HT32F67595
Datasheet

32-Bit Arm® Cortex®-M33/M0+ Dual Core BLE Microcontroller, up to 1024 KB Flash, 256 KB SRAM and 256 KB ROM with BLEC, 2P4GC, DMAC, STIM, GPTM, WDT, RTC, SPI, DSPI, QSPI, UART, I²C, SCI, IrDA, I²S, PCM, AES128, TRNG, QEI, ADC, TSEN

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1 General Description

The Holtek HT32F67595 device is a high performance, low power consumption 32-bit microcontroller based around an Arm® Cortex®-M33 processor core and with an Arm® Cortex®-M0+ co-processor core which runs the lower layer of the BLE and 2.4G protocol stack. The Cortex®-M33 is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer, and including advanced debug support.

The device operates at a frequency of up to 64 MHz with a Flash accelerator to obtain maximum efficiency. It provides up to 1024 KB encryptable in-system Flash memory with 16 KB cache controller for code/data storage, up to 256 KB of embedded SRAM memory for system operation and application program usage and up to 256 KB of embedded ROM memory for preprogrammed embedded RTX-RTOS kernel, driver library, and BLE lower layer protocol stack software. A variety of peripherals, such as BLEC, 2P4GC, DMAC, STIM, GPTM, WDT, RTC, SPI, DSPI, QSPI, UART, I^2C, SCI, IrDA, I^2S, PCM, AES128, TRNG, QEI, ADC, TSEN and SW-DP (Serial Wire Debug Port), etc., are also implemented in the device. Several power saving modes provide the flexibility for maximum optimization between wake-up latency and power consumption, an especially important consideration in low power applications.

The above features ensure that the device is suitable for use in a wide range of BLE products such as handheld products, health care products, home appliances, smart device information beacons, data loggers, human interface device service, etc.

2 Features

Main-Processor – MP

- 32-bit Arm® Cortex®-M33 main processor core
- Up to 64 MHz operating frequency
- 1.5 DMIPS/MHz
- Architecture optimized for small-footprint embedded applications
- Outstanding processing performance combined with fast interrupt handling
- Fast code execution permits slower processor clock or increases sleep mode time
- Efficient processor core, system, and memories
- Low-power consumption with integrated sleep modes
- Serial wire trace reduces the number of pins required for debugging and tracing

The Cortex®-M33 processor provides a high-performance of 1.5 DMIPS/MHz and low-power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

The CPU executes code from flash using a 16 KB cache controller. Code in flash might be encrypted, so, decryption will happen while in progress without extra wait states.

Co-Processor – CP

- 32-bit Arm® Cortex®-M0+ processor core
- 16 MHz operating frequency
- 0.93 DMIPS/MHz

The Cortex®-M0+ processor executes code from a dependent 64K Bytes SRAM memory. The code and data can be encrypted and stored in other non-volatile memory such as Flash memory and be dynamically uploaded by software when the device is powered on, which runs the lower layer of the BLE and 2.4G protocol stack.

On-Chip Memory

- Up to 1024 KB in-system Flash memory with 16 KB cache controller for code/data and options storage
- Up to 256 KB of embedded SRAM memory for system operation and application program usage
- Up to 256 KB of embedded ROM memory for preprogrammed embedded RTX-RTOS kernel, driver library, and BLEC lower layer protocol stack software.

The in-system flash memory provides non-volatile storage for code and data.

The ROM provides preprogrammed embedded RTX-RTOS kernel, driver library, and BLEC lower layer protocol stack software. It also contains a boot loader that can be used to reprogram the device using SPI or UART. Since ROM contains BLE host and controller software libraries, leaving more of the flash memory available for the customer applications.

Up to 256K Bytes SRAM used for both store the Cortex®-M33 code & data and Cortex®-M0+ code. It is split into 4 × 64K Bytes blocks, each block should be enabled or disabled individually by software to minimize power consumption when system in low power mode. In additional it contains a 16K bytes flash cache. When it is not used, the cache can be used as a general-purpose SRAM.

Debug Support

- 2-Wire SWD debugging
- Supports over-the-air (OTA) upgrade

Bluetooth Low Energy Controller – BLEC

- 2.4 GHz RF transceiver compatible with Bluetooth Low Energy (BLE) 5.3 specification
- Operating clock 16 MHz
- Low power modes supporting 32.768 kHz
- Four operating modes: Active, Sleep, Deep-Sleep and Hibernation
- GFSK modulation, Frequency-Hopping Spread Spectrum (FHSS)
- Support LE 1 Mbps, 2 Mbps and coded 500 Kbps, 125 Kbps for long-range
- Support AoA/AoD for direction finding
- Receiver supports programmable gain control of over 70 dB
- Excellent receiver sensitivity of -96 dBm @ 1 Mbps
- Programmable transmitter output power up to +10 dBm
- All device classes support: Broadcaster, Central, Observer, Peripheral
- Simultaneous Master and Slave operation
- Frequency Hopping
- All packet types: Advertising, Data, Control
- Encryption: AES, CCM
- Bit stream processing: CRC, Whitening

The BLE core is a qualified Bluetooth baseband controller compatible with the Bluetooth Smart specification and it is in charge of packet encoding/decoding and frame scheduling. It performs Link Layer Control management supporting the main BLE states, including advertising and connection.

2.4G RF Private Protocol Controller – 2P4GC

- 2.4 GHz RF transceiver
- FSK/GFSK modulation
- Programmable 8/16/80-bit preamble
- Wake-on Radio
- Auto CRC-16

Reset Control Unit – RSTCU

- System Resets
  - Power On Reset – POR
  - Brown Out Detector – BOD
  - Low Voltage Detector – LVD
- Watchdog Time-out reset
- Software-initiate reset of digital peripherals

There are several sources of reset, some are triggered due to errors or unexpected behavior, while others are user initiated.

Clock Control Unit – CKCU

- External 16 MHz crystal (±20 ppm) oscillator
- External 32.768 kHz crystal (±50 ppm) oscillator
- Internal 16 MHz / 48 MHz RC oscillator
- Internal 32 kHz RC oscillator
- Integrated system clock PLL
- Independent clock divider and gating bits for peripheral clock sources

The CKCU support two external and two internal clock sources. A 16 MHz crystal is required as the frequency for the radio. This signal is doubled internally to create a 64 MHz clock by PLL. Bluetooth low energy requires a slow-speed clock with better than ±50 ppm accuracy if the device is to enter any low power mode while maintaining a connection. The internal 32 kHz RC oscillator can in some use cases be compensated to meet the requirement. The low-speed crystal oscillator is designed for use with a 32.768 kHz crystal. The internal high speed PLL (64 MHz) can be used as a clock source for the main processor, Arm® Cortex®-M33, subsystem. The 32 kHz clock source can be used as external clocking referenced through GPIO.

Power Management Control Unit – PMU

- Single V_{DD} power supply: 1.8 V to 3.6 V
- On-Chip internal SISO DC/DC
- To minimize power consumption, PMU supports a number of software configurable power mode and power management features

Power Mode / Function Block	Active (ACT)	Sleep (SLP)	Deep-Sleep (DSLP)	Hibernation (HIB)
CPU	Active	Off	Off	Off
FLASH	On	Available	Off	Off
SRAM	On	On	Off	Off
RADIO	On	Off	Off	Off
SRAM Retention	Full	Partial	No	No
16M RC / Crystal	On	Off	Off	Off
32K RC / Crystal	On	On	On	Off

Power Mode / Function Block	Active (ACT)	Sleep (SLP)	Deep-Sleep (DSLP)	Hibernation (HIB)
Peripheral	Available	Available	Off	Off
Wake up on RTC	Available	Available	Available	Off
Wake up on GPIO	Available	Available	Available	Available

In the Active mode, the application Cortex®-M33 or Cortex®-M0+ CPU is actively executing code. The Active mode provides normal operation of the processor and all of the peripherals that are currently enabled. The system clock can be any available clock source.

In the Sleep mode, all active peripherals can be clocked. But the application CPU core and memory are not clocked, and no code is executed. Any interrupt event will bring the processor back into active mode.

In the Deep-Sleep mode, only the always-on domain is active. An external wake-up event RTC event is required to bring the device back to active mode.

In the Hibernation mode, the device is turned off entirely, including the always-on domain. The I/O are latched with the value they had before entering hibernation mode. A change of state on any I/O pin defined as a wake-up from hibernation pin wakes up the device and functions as a reset trigger.

DMA Controller – DMAC

- Support memory to memory, memory to peripheral, peripheral to memory and peripheral to peripheral transmission
- Support UART, SPI, I²C, SCI, I²S, ADC interface
- 4 independent DMA channels
- Configurable 2 level priority
- Independent source and destination transfer size (8-bit, 16-bit, 32-bit)
- Support circular mode
- Up to 65535 programmable number of data to be transferred
- Source and destination address increment or no increment

The DMA controller provides a way to offload data transfer tasks from the CPU, allowing for more efficient use of the processor and the available bus bandwidth. The DMA controller can perform transfers between memory and peripherals. The controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory as the peripheral is ready to transfer more data.

I/O Ports – GPIO

- Up to 16 GPIOs
- Programmable driver strength up to 10 mA
- Fully flexible digital pin multiplexing allows use as GPIO or any of several peripherals functions
- Pin state can be retained during all sleep modes
- Pins configured as digital inputs are Schmitt-triggered

- Programmable control for GPIO pad configuration
  - Weak pull-up or pull-down resistors
  - Digital input enables
- Programmable control for interrupts
  - POR Interrupt generation masking per pin
  - Edge-triggered on rising or falling

There are up to 16 general purpose I/O pins, GPIO, for the implementation of logic input/output functions. Each of the GPIO ports can be multiplexed to any digital peripheral through the I/O controller which has a series of related control and configuration registers to maximize flexibility and to meet the requirements of a wide range of applications.

System Tick Timer – STIM

- 32-bit compare match count-up counter – no I/O control features
- One shot mode – counting stops after a match condition
- Repetitive mode – restarts counter after a match condition

There are two dependent system tick timers (STIM), which provide a 48-bit incrementing wrap-on-zero counter with a flexible control mechanism. The system tick timer can be used in several different ways.

General-Purpose Timer – GPTM

- 16-bit or 32-bit operating modes
  - 16-bit or 32-bit programmable one-shot timer
  - 16-bit or 32-bit programmable periodic timer
  - 16-bit general-purpose timer with a 4-bit prescaler
  - 16-bit input-edge count or time-capture mode with 4-bit prescaler
  - 16-bit PWM mode with 4-bit prescaler and software configurable output inversion
- Count Mode
  - Power On Reset – POR
  - Count Up Mode
  - Continue Count Up Mode
  - Count Up-Down Mode
  - Continue Up-Down Mode
- Four 32-bit counter or up to eight 16-bit counters
- Up to eight PWM pins
- Efficient transfers using the DMA controller
- Two 32-bit Timers support IR output to specific pins
- Capture Mode
- IR decode function with capture mode

The general-purpose timers can be used to count or time external events that drive the timer-input pins. Each 16 or 32-bit GPTM block provides two 16-bit timers or counters that can be configured to operate independently as timers or event counters or configured to operate as on 32-bit timer.

Watchdog Timer – WDT

- Two 32-bit counter up with 30.52 μs step for a maximum 36.41 hr time-out
- Non-Maskable Interrupt (NMI) or WDT reset
- NMI interrupt can be selected masked 16 × 30.52 μs ahead before WDT reset

The watchdog timer is used to regain control when system fails because of a software error, or an external device failed to respond properly.

There are two dependent watchdog timers, which can generate a reset when a predefined timer-out value is reached. Two internal 32K RC oscillators provide dependent clock source for two watchdog timers.

Real Time Clock – RTC

- 48-bit incrementing counter with support for programmable increment to support ppm-adjustment
- Four match registers supporting the generation of events
- Software and hardware reset of events

The Real Time Clock implements a second and sub-second counter with support for soft-compensation for ppm-offsets, with four match registers.

Serial Peripheral Interface – SPI

- SPI clock frequency up to 16 MHz and programmable output frequencies in master mode
- 8 bytes transmit and receive FIFO
- SPI mode 0, 1, 2, 3 support (clock edge and phase)
- Support both master and slave modes
- Support Multi-master and multi-slave operation
- Support RX timeout interrupt
- Programmable TX only / RX only / TRX mode
- Programmable SPI_DO idle byte

This interface supports a subset of the Serial Peripheral Interface SPI. The serial interface can transmit and receive 8, 16, 32 bits or as long as data in master/slave mode. Data is written from a master (CPU/DMA) over the APB bus to the SPI.

Universal Asynchronous Receiver Transmitter – UART

- Programmable serial data baud rate
- Hardware flow control support (CTS/RTS)
- Functionality based on the 16550 industry standard
- Programmable character properties, such as number of data bits per character (5~8), optional
- Parity bit (with odd/even/stick/no select) and number of stop bits (1, 1.5 or 2)

- 8 bytes transmit and receive FIFOs
- Support line break generation and detection
- Support RX timeout interrupt

The UART is compliant to the industry-standard 16550 and is used for serial communication with a peripheral data set. Data is written from a master (CPU/DMA) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU/DMA) to read back. Both UARTs support hardware flow control signals (RTS, CTS).

Inter-Integrated Circuit – I²C

- Two-wire I²C serial interface consists of a serial data line (SDA) and a serial clock (SCL)
- Support three speed modes:
  - Standard mode: 0 ~ 100K bit/s
  - Fast mode: ≤ 400K bit/s
  - High-speed mode: ≤ 3M bit/s
- Support 8 bytes transmit/receive FIFOs
- Configurable master or slave, transmit/receive operation
- Support 7-bit or 10-bit addressing mode
- Support configurable slave address and target address
- Interrupt operation

The I²C interface is a programmable control bus that provides support for the communications link between Integrated Circuits in a system. It is a simple two-wire bus with a software-defined protocol for system control, which is used in temperature sensors and voltage level translators to EEPROMs, general-purpose I/O, A/D and D/A converters.

Smart Card Interface – SCI

- Support the asynchronous protocols T=0 in accordance with ISO 7816-3
- Flexible output clock 1/2/4 MHz
- Error management at character level for T=0 that parity error counter in reception mode and in transmission mode with auto-repetition
- 32-bit counting by ETU clock for time-out counter
- Power-down mode for reducing current consumption when no activity

The smart card interface is compatible with the ISO 7816-3 and EMV 4.2 related standards. As a master device, it can transmit data controlled by CPU/DMA to destination card, and also it can receive data stored in SRAM.

Inter-IC Sound – I²S

- Master and Slave mode
- I²S-justified, Left-justified and DSP (PCM A&B) formats
- 16-bit, 20-bit, 24-bit operation
- Programmable MCLK output: 16/8/4/2 MHz
- Programmable sample rate f_S: 8/16/32 kHz

The I²S is a synchronous communication interface that can be used as a master or slave to exchange data with other audio peripherals, such as ADCs or DACs.

Cryptography

Advanced Encryption Standard – AES128

- Supports AES Encrypt / Decrypt functions
- Supports AES ECB/CBC/CTR modes
- Supports Key Size of 128 bits
- Supports 4 words Initial Vector for CBC and CTR modes
- 4 × 32-bit AES data buffer
- DMA support
- Supports Word Data Swap function

The AES core supports both encryption and decryption functions and supports 128-bit input data. It should be noted that hardware does not pad out any input data bits, therefore users need to do pad action by software at first.

True Random Number Generator – TRNG

- TRNG used to provide the seed for encryption processes, its output can be used as entropy input for a Crypto engine

The crypto engine could work in bypass mode and aims to accelerate the algorithm calculations that are needed in order to implement the AES and CBC crypto.

Security

- Supports 32-bit Unique ID for each chip
- Supports automatic hardware decoding

The security module used to protect the code saved in the flash memory, it supports encrypted storage of code for each chip. A 32-bit unique ID is used as the encryption key and each chip can perform the same function but store different code. The user can also use the security module to encrypt the BOOT program.

Quadrature Encoder Interface – QEI

- Support 2-channel incremental encode

A quadrature encoder, also known as a 2-channel incremental encoder, converts linear displacement into a pulse signal. By monitoring both the number of pulses and the relative phase of the two signals, you can track the position, direction of rotation, and speed. In addition, a third channel, or index signal, can be used to reset the position counter. The quadrature encoder interface (QEI) interprets the code produced by a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, it can capture a running estimate of the velocity of the encoder wheel.

Analog to Digital Converter – ADC

- Up to 14-bit dynamic SAR ADC engine
- Conversion time and dynamic range can be changed
  - 14-bit dynamic with 125 ksps for audio application
  - 12-bit dynamic with 500 ksps for general application
- Up to 5 single-ended channels
- One channel for battery monitoring
- DMA support

The low power general purpose 14-bit ADC has up to 5 channels and operates in the single ended mode.

Temperature Sensor – TSEN

- Detection range: -40 °C ~ 125 °C
- Accuracy: ±8 °C
- Resolution: 0.3 °C

A BJT based temperature sensor is integrated, which can be used for performance tuning over temperatures. The sensed voltage is converted to 12-bit digital code by general purpose ADC. Accuracy compensation could be implemented by customer if required.

Package and Operation Temperature

- 28-pin LGA package
- Operation temperature range: -40 °C to 85 °C

3 Overview

Device Information

Table 1. Features and Peripheral List

Peripherals		HT32F67595
In-System Flash (KB)		1024
ROM (KB)		256
SRAM (KB)		256
Timers	STIM (System Tick Timer)	2
	GPTM	4
	WDT	2
	RTC	1
Communication	QSPI (SPI/DPI/QPI)	2
	UART	3
	I^2C	2
	SCI (ISO7816-3)	1
	IrDA	1
	I^2S/LJF/PCM	1
AES-128		1
TRNG		1
QEI (Quadrature Encoder I/F)		1
14-bit ADC	Number of ADCs	2
	Number of channels	5
TSEN (Temperature sensor)		1
GPIO		Up to 16
CPU frequency		Up to 64 MHz
Operating voltage		1.8 V ~ 3.6 V
Operating temperature		-40 °C ~ 85 °C
Package		28-pin LGA

Block Diagram

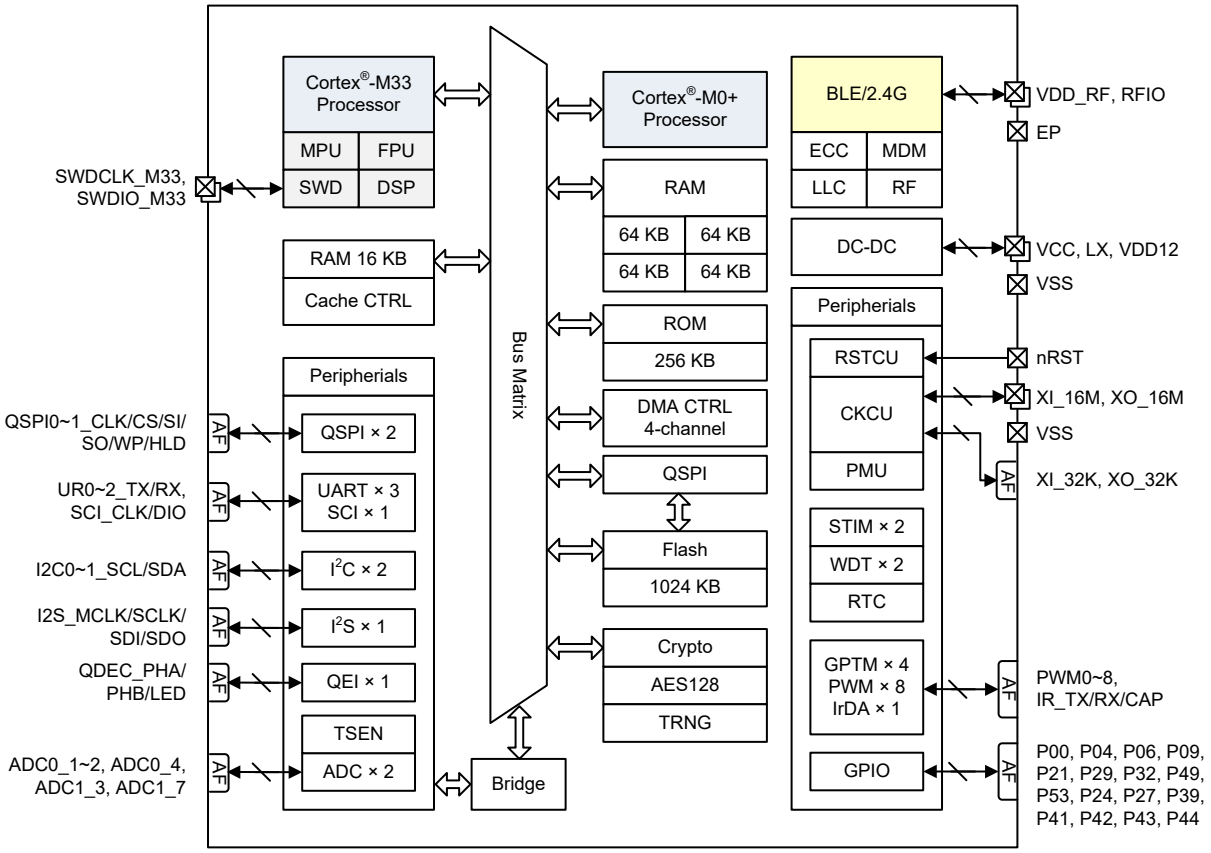


Figure 1. Block Diagram

4 Pin Assignment

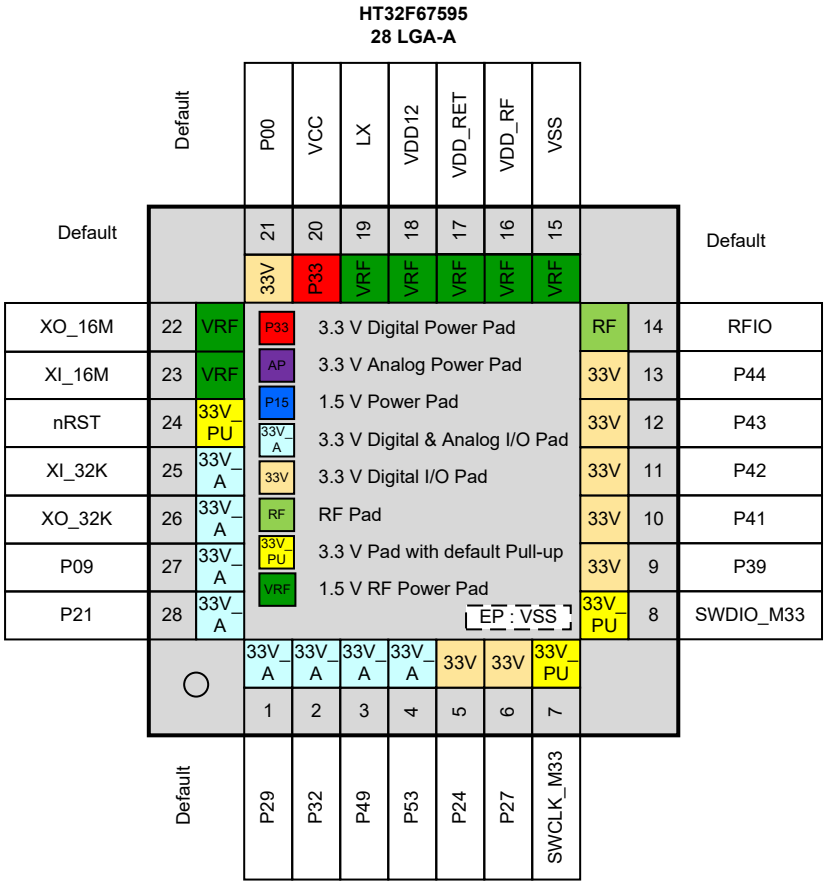


Figure 2. 28-pin LGA Pin Assignment

Table 2. Pin Assignment

Package	HT32F67595 Alternate Function Mapping										
28 LGA	Default	GPIO	ADC×2	IrDA×1	CLKOUT	SPI/DPI/ QPI×2	I²C ×3	UART×3	PWM×8	QEI ×1	I²S/ PCM×1
28	P21		ADC0_2			V	V	V	V	V	V
1	P29				16MOUT	V	V	V	V	V	V
2	P32		ADC0_4			V	V	V	V	V	V
3	P49		ADC1_3			V	V	V	V	V	V
4	P53		ADC1_7			V	V	V	V	V	V
5	P24					V	V	V	V	V	V
6	P27					V	V	V	V	V	V
7	SWCLK_M33										
8	SWDIO_M33										
9	P39				32KOUT	V	V	V	V	V	V
10	P41					V	V	V	V	V	V
11	P42				32KOUT	V	V	V	V	V	V
12	P43					V	V	V	V	V	V
13	P44					V	V	V	V	V	V
14	RFIO										
15	VSS										
16	VDD_RF										
17	VDD_RET										
18	VDD12										
19	LX										
20	VCC										
22	XO_16M										
23	XI_16M										
24	nRST										
21	P00			IR_TX		V	V	V	V	V	V
25	XI_32K	P04									
26	XO_32K	P06									
27	P09		ADC0_1			V	V	V	V	V	V

Note: Alternate Function “V”: Programmable

Table 3. Alternate Function Mapping

PID	Function	PID	Function	PID	Function	PID	Function	PID	Function
0	GPIO	16	SPI1_CLK	32	I2S0_ODATA	48	GPTM1_CAP1	64	GPTM3_B_DECODE
1	UART0_CTS	17	SPI1_MISO	33	I2S0_BCLK	49	GPTM1_A_PWM	109	CLKOUT
2	UART0_RXD	18	SPI1_CS	34	I2S0_WCLK	50	GPTM1_B_PWM	113	ADC0_TRIG
3	UART0_RTS	19	SPI1_MOSI	35	I2S0_SDATA	51	GPTM1_A_DECODE	117	ADC1_TRIG
4	UART0_TXD	20	SPI0_CLK	36	I2S0_MCLK	52	GPTM1_B_DECODE		
5	UART1_CTS	21	SPI0_MISO	37	QDEC_PHA	53	GPTM2_CAP0		
6	UART1_RXD	22	SPI0_CS	38	QDEC_PHB	54	GPTM2_CAP1		
7	UART1_RTS	23	SPI0_MOSI	39	QDEC_LED	55	GPTM2_A_PWM		
8	UART1_TXD	24	—	40	GPTM0_CAP0	56	GPTM2_B_PWM		
9	UART2_CTS	25	—	41	GPTM0_CAP1	57	GPTM2_A_DECODE		
10	UART2_RXD	26	I2C0_SCL	42	GPTM0_A_PWM	58	GPTM2_B_DECODE		
11	UART2_RTS	27	I2C0_SDA	43	GPTM0_B_PWM	59	GPTM3_CAP0		
12	UART2_TXD	28	I2C1_SCL	44	GPTM0_A_DECODE	60	GPTM3_CAP1		
13	7816_UAM_CLK	29	I2C1_SDA	45	GPTM0_B_DECODE	61	GPTM3_A_PWM		
14	7816_UAM_DAT	30	I2C2_SCL	46	GPTM_IR_OUT	62	GPTM3_B_PWM		
15	7816_UAM_RST_N	31	I2C2_SDA	47	GPTM1_CAP0	63	GPTM3_A_DECODE		

Table 4. Pin Description

Pin Number	Pin Name	Type(1)	I/O Structure(2)	Output Driving	Description	
28 LGA					Default Function	Common Function
28	P21	AI/O	33V	2/4/8/10 mA	P21	ADC0_2
1	P29	AI/O	33V	2/4/8/10 mA	P29	—
2	P32	AI/O	33V	2/4/8/10 mA	P32	ADC0_4
3	P49	AI/O	33V	2/4/8/10 mA	P49	ADC1_3
4	P53	AI/O	33V	2/4/8/10 mA	P53	ADC1_7
5	P24	I/O	33V	2/4/8/10 mA	P24	QSPI1_CS
6	P27	I/O	33V	2/4/8/10 mA	P27	QSPI1_HLD
7	SWCLK_M33	I	33V_PU	—	SWCLK_M33	—
8	SWDIO_M33	I/O	33V_PU	—	SWDIO_M33	—
9	P39	I/O	33V	2/4/8/10 mA	P39	32KOUT
10	P41	I/O	33V	2/4/8/10 mA	P41	—
11	P42	I/O	33V	2/4/8/10 mA	P42	32KOUT
12	P43	I/O	33V	2/4/8/10 mA	P43	—
13	P44	I/O	33V	2/4/8/10 mA	P44	16MOUT
14	RFIO	AI/O	12V	—	RF I/O	—
15	VSS	P	—	—	RF power ground	—
17	VDD_RF	P	—	—	VDD for RF Block	—
16	VDD_RET	P	—	—	VDD for Retention	—
18	VDD12	P	—	—	DC-DC Output (1.2 V)	—
19	LX	AO	12V	—	DC-DC switching output	—
20	VCC	P	33V	—	Power Supply (1.8~3.6 V)	—
22	XO_16M	AO	12V	—	External 16 MHz DCXO XO	—
23	XI_16M	AI	12V	—	External 16 MHz DCXO XI	—
24	nRST	I	33V_PU	—	External reset pin	—
21	P00	I/O	33V	2/4/8/10 mA	P00	IR_TX
25	XI_32K	I/O	33V	2/4/8/10 mA	XI_32K	P04
26	XO_32K	I/O	33V	2/4/8/10 mA	XO_32K	P06
27	P09	AI/O	33V	2/4/8/10 mA	P09	ADC0_1

Note: 1. I = Input, O = Output, A = Analog Port, P = Power Supply
2. 33V = 3.3 V tolerant, PU = Pull-up, 12V = 1.2 V, 50V = 5.0V tolerant
3. The EP means the exposed pad on the packages. It must be connected to ground.

5 Electrical Characteristics

Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	External Main Supply Voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{IN}	Input Voltage on I/O	V_{SS} - 0.3	V_{DD} + 0.3	V
T_A	Ambient Operating Temperature Range	-40	85	°C
T_{STG}	Storage Temperature Range	-65	150	°C
T_J	Maximum Junction Temperature	—	125	°C
V_{ESD}	Electrostatic Discharge Voltage – Human Body Mode	-2500	2500	V

Recommended Operating Conditions

Table 6. Recommended Operating Conditions

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Main Operating Voltage	—	1.8	3.3	3.6	V
V_{ADC}	ADC Input Voltage	—	0.0	—	1.1	V
V_{OSC}	Crystal Oscillator Input Voltage	—	0.5	—	1.2	V

Power Consumption

Table 7. Power Consumption Characteristics

T_A = 25 °C, V_{CC} = 3.0 V and V_{DD_RET} = 1.1 V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
LDO Mode						
I_{ACT}	Cortex®-M33 per MHz	Internal RC	59	62	65	μA
		External 16 MHz Crystal	70	75	80	μA
	Radio RX	@ 1 Mbps PHY	—	10.3	11.1	mA
		@ 2 Mbps PHY	—	10.4	11.1	mA
	Radio TX	@ 0 dBm	—	10.4	11.1	mA
		@ 10 dBm	—	32.1	35.3	mA
I_{SLP}	Sleep	256K SRAM Retention	4.9	5.4	5.9	μA
		64K SRAM Retention	3.0	3.2	3.8	μA
I_{DSLP}	Deep-Sleep	RTC On, External 32K Crystal	—	2.5	2.6	μA
I_{HIB}	Hibernation	RTC Off	—	1.9	2.4	μA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC/DC Mode(Note)						
I_{ACT}	Cortex®-M33 per MHz	Internal RC	—	53.5	—	μA
		External 16 MHz Crystal	—	55.1	—	μA
	Radio RX	@ 1 Mbps PHY	—	4.0	4.4	mA
		@ 2 Mbps PHY	—	3.8	4.4	mA
	Radio TX	@ 0 dBm	—	3.8	4.5	mA
		@ 10 dBm	—	18	24	mA
I_{SLP}	Sleep	256K SRAM Retention	2.6	2.9	3.1	μA
		64K SRAM Retention	2.3	2.5	2.75	μA
I_{DSLP}	Deep-Sleep	RTC On, External 32K Crystal	—	2.65	2.9	μA
I_{HIB}	Hibernation	RTC Off	—	1.85	2.05	μA

Note: Please note that the real current in the DC/DC mode depends on the inductor component selection.

Reset Characteristics

Table 8. V_{CC} Power Reset Characteristics

T_A = 25 °C & V_{CC} = 3.0 V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
R_{PU}	Weak Internal Pull-up Equivalent Resistor	V_{CC} = 3.3 V	100	110	120	kΩ
		V_{CC} = 3.0 V	110	125	140	
		V_{CC} = 2.5 V	130	160	190	
		V_{CC} = 1.8 V	260	290	320	
t_{PUS}	Reset Input Pulse	1.8 V < V_{CC} < 3.6 V	—	—	100	ns

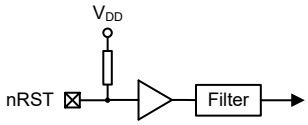


Figure 3. nRST Pin Block Diagram

External Clock Characteristics

Table 9. 16 MHz External Crystal Oscillator Characteristics

T_A = 25 °C & V_{CC} = 3.0 V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
ESR	Equivalent Series Resistance	6 pF < C_L < 9 pF	—	20	120	Ω
C_L	Crystal Load Capacitance	—	3	—	27	pF
f_{HSE}	Crystal Frequency	—	—	16	—	MHz
FT_{HSE}	Crystal Frequency Tolerance	—	-20	—	20	ppm
t_{HSESU}	Start-up Time	—	1.3	1.5	2.3	ms
TOL_{HSE}	Crystal Tolerance	T_A = 25 ± 3 °C	—	—	±10	ppm
		T_A = -20 ~ 75 °C	—	—	±10	ppm

Table 10. 32.768 kHz External Crystal Oscillator Characteristics

T_A = 25 °C & V_{CC} = 3.0V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
ESR	Equivalent Series Resistance	6 pF < C_L < 9 pF	—	30	100	Ω
C_L	Crystal Load Capacitance	—	3	—	27	pF
f_{LSE}	Crystal Frequency	—	—	32.768	—	kHz
FT_{LSE}	Crystal Frequency Tolerance	—	-50	—	50	ppm
t_{LSESU}	Start-up Time	—	—	3	—	ms

Internal Clock Characteristics

Table 11. 32 kHz Internal RC Oscillator Characteristics

T_A = 25 °C & V_{CC} = 3.0V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{IRC32K}	Internal 32 kHz RC Oscillation Frequency	Calibrate Frequency	32.62	32.81	32.90	kHz
TC_{IRC32K}	Temperature Coefficient	—	—	80	—	ppm/°C

Table 12. 16 MHz Internal RC Oscillator Characteristics

T_A = 25 °C & V_{CC} = 3.0V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{IRC16M}	Internal 16 MHz RC Oscillation Frequency	Calibrate Frequency	15.68	16.0	16.32	MHz
TC_{IRC16M}	Temperature Coefficient	—	70	80	90	ppm/°C

Table 13. 48 MHz Internal RC Oscillator Characteristics

T_A = 25 °C & V_{CC} = 3.0V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{IRC48M}	Internal 48 MHz RC Oscillation Frequency	Calibrate Frequency	45.68	48.0	48.30	MHz
TC_{IRC48M}	Temperature Coefficient	—	70	80	90	ppm/°C
$t_{IRC48MSU}$	Start-up Time	—	—	8	10	μs

RF Characteristics

Table 14. Radio RX Characteristics

T_A = 25 °C, V_{CC} = 3.0V & LDO Mode, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit
P_{MIN}	Sensitivity	-94.5	-96	-97	dBm
In-Band Blocking					
C_{I0}	Co-channel Interference	—	-3	—	dB
C_{I1}	Interferer at f_{OFFS} = +1/-1 MHz	—	9/5	—	dB
C_{I2}	Interferer at f_{OFFS} = +2/-2 MHz	—	43/42	—	dB
C_{I3}	Interferer at f_{OFFS} = +3/-3 MHz	—	47/42	—	dB
C_{I4}	Interferer at Image Channel (f_{IMAGE})	—	32	—	dB
C_{I5}	Interferer at Image Channel (f_{IMAGE} +1/-1 MHz)	—	5/12	—	dB
Out-of-Band Blocking					
	f = 30 ~ 2,000 MHz	—	-40	—	dBm
	f = 2,000 ~ 2,399 MHz	—	-19	—	dBm
	f = 2,484 ~ 3,000 MHz	—	-22	—	dBm
	f = 3,000 ~ 12,750 MHz	—	-42	—	dBm

Symbol	Parameter	Min.	Typ.	Max.	Unit
Intermodulation Performance for Wanted Signal					
	at -64 dBm and 1 Mbps BLE, 3rd, 4th and 5th Offset Channel	—	-37	—	dBm
P_{ISSI}	Upper Limit of Monotonous Range	—	-94	—	dBm

Table 15. Radio TX Characteristics

T_A = 25 °C, V_{CC} = 3.0V & LDO Mode, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit
P_{TX}	Output Power	-45	0	10	dBm
	Output Power Step	—	3	—	dBm
Δ_{F2AVG}	Average Frequency Deviation for 10101010 Pattern	185	249	—	kHz
Δ_{F1AVG}	Average Frequency Deviation for 11110000 Pattern	225	247	275	kHz
	Δ_{F2AVG} / Δ_{F1AVG}	0.8	1	—	—
Carrier	Frequency Accuracy	-150	0	150	kHz
	Maximum Frequency Drift	-20	0	20	kHz
	Initial Frequency Drift	-23	0	23	kHz
	Maximum Drift Rate (per 50 μs)	-20	0	20	kHz
Spurious Emissions					
	f < 1 GHz	—	-21	—	dBm
	f > 1 GHz including harmonics	—	-43	—	dBm
In-Band Emissions (at 0 dBm, f = 2400 ~ 2483.5 MHz)					
	< f ± 2 MHz	-48	-44	-40	dBm

I/O Port Characteristics

Table 16. I/O Port Characteristics

T_A = 25 °C & V_{CC} = 3.0V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
R_{PU}	Pull-up Equivalent Resistor	V_{CC} = 3.3 V	105	115	125	kΩ
		V_{CC} = 3.0 V	110	125	135	kΩ
		V_{CC} = 2.5 V	150	160	170	kΩ
		V_{CC} = 1.8 V	270	290	310	kΩ
R_{PD}	Pull-down Equivalent Resistor	V_{CC} = 3.3 V	65	85	95	kΩ
		V_{CC} = 3.0 V	80	90	100	kΩ
		V_{CC} = 2.5 V	105	115	125	kΩ
		V_{CC} = 1.8 V	185	205	220	kΩ
I_{DRV0}	Level-0	V_{CC} = 3.3 V	4.8	5.0	5.2	mA
		V_{CC} = 3.0 V	3.8	4.0	4.2	mA
		V_{CC} = 2.5 V	3.0	3.2	3.4	mA
		V_{CC} = 1.8 V	1.8	2.0	2.2	mA
I_{DRV1}	Level-1	V_{CC} = 3.3 V	7.3	7.5	7.7	mA
		V_{CC} = 3.0 V	6.6	6.8	7.0	mA
		V_{CC} = 2.5 V	4.8	5.0	5.2	mA
		V_{CC} = 1.8 V	3.1	3.3	3.5	mA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{DRV2}	Level-2	V_{CC} = 3.3 V	9.6	9.8	10	mA
		V_{CC} = 3.0 V	8.8	9.0	9.2	mA
		V_{CC} = 2.5 V	6.6	6.8	7.0	mA
		V_{CC} = 1.8 V	4.0	4.2	4.4	mA
I_{DRV3}	Level-3	V_{CC} = 3.3 V	10.8	11.0	11.2	mA
		V_{CC} = 3.0 V	9.6	9.8	10.0	mA
		V_{CC} = 2.5 V	7.5	7.7	7.9	mA
		V_{CC} = 1.8 V	5.2	5.4	5.6	mA

ADC Characteristics

Table 17. ADC Characteristics

T_A = 25 °C & V_{CC} = 3.0V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{REF}	Reference Voltage(1)	—	—	1.1	—	V
f_{ADC}	Clock Frequency	—	—	4	8	MHz
f_S	Sampling Rate	14-bit	—	125	—	ksps
		12-bit	—	500	—	ksps
t_{TRIG}	External Trigger Period	—	—	—	10	$1/f_{ADC}$
V_{AIN}	Conversion Voltage Range	—	0	—	V_{REFT+}	V
R_{AIN}	External Input Impedance	—	—	—	10	MΩ
C_{ADC}	Internal S/H Capacitor Impedance	—	—	5	—	pF
t_{PU}	Power-up Time	—	—	1	—	CC(2)
t_S	Sampling Time	—	1.5	—	1000	$1/f_{ADC}$
t_{CONV}	Total Conversion Time (Resolution = N bits)	—	t_S+0.5+N/2	—	—	$1/f_{ADC}$
ACC	Accuracy	V_{AIN} < 50 mV	—	±10	—	LSB
		50 mV < V_{AIN} < 50 mV	—	±2	±3	LSB
ENOB	Effective Number of Bits	Single Ended	—	11.8	—	Bits
		Differential	—	13.2	—	Bits

Note: 1. When V_{AIN} > V_{REFT+}, the ADC convert result is 0xFFF.
2. CC: Conversion Cycle.

I²C Characteristics

Table 18. I²C Characteristics

T_A = 25 °C, V_{CC} = 3.0 V & SCL = 1 MHz, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{SCL}	SCL Clock Frequency	—	—	—	1	MHz
t_{LOW}	SCL Low Level Duration	—	0.6	—	—	µs
t_{HIGH}	SCL High Level Duration	—	0.3	—	—	µs
t_{RISE}	SCL, SDA Rise Time	—	—	—	0.2	µs
t_{FALL}	SCL, SDA Fall Time	—	—	—	0.2	µs
$t_{SU:DAT}$	SDA Setup Time	—	0.1	—	—	µs
$t_{HD:DAT}$	SDA Hold Time	—	10	—	—	µs

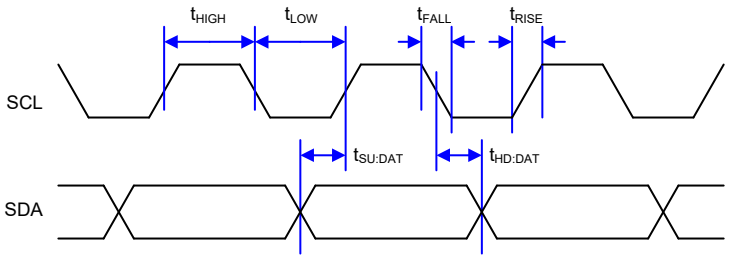


Figure 4. I²C Timing Diagram

SPI Characteristics

Table 19. SPI Characteristics

T_A = 25 °C & V_{CC} = 3.0 V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$1/t_{CK}$	Clock Frequency	2.5 V < V_{CC} < 3.6 V	—	—	32	MHz
		1.8 V < V_{CC} < 2.5 V	—	—	20	MHz
$t_{W(CKH)}$	Clock High Time	—	t_{CK}/2-0.5	—	t_{CK}/2	ns
$t_{W(CKL)}$	Clock Low Time	—	t_{CK}/2	—	t_{CK}/2+0.5	ns
$t_{S(IN)}$	Data Input Setup Time	—	1	—	—	ns
$t_{H(IN)}$	Data Input Hold Time	—	3.5	—	—	ns
$t_{V(OUT)}$	Data Output Valid Time	—	—	1	2	ns
$t_{H(OUT)}$	Data Output Hold Time	—	0	—	—	ns

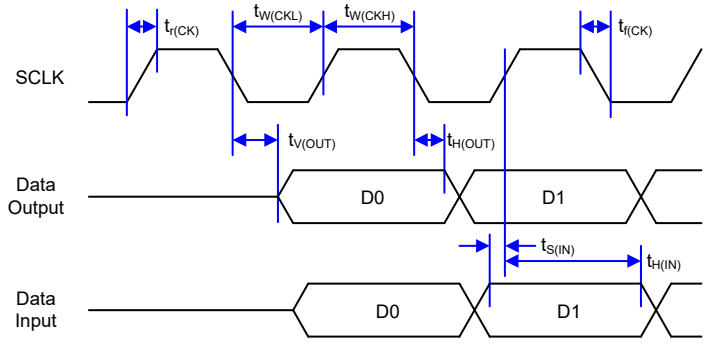


Figure 5. SPI Timing Diagram

TSEN Characteristics

Table 20. TSEN Characteristics

T_A = 25 °C & V_{CC} = 3.0V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
TC	Sensor Temperature Coefficient	—	—	2	—	mV/°C
T_{RNG}	Temperature Sensor Range	—	-40	—	125	°C
T_{ACC}	Temperature Sensor Accuracy	—	-8	—	8	°C
T_{RES}	Temperature Sensor Resolution	—	—	0.3	—	°C
$t_{V(OUT)}$	Data Output Valid Time	—	—	0.3	—	ns
I_{TSEN}	Temperature Sensor Current	—	—	20	—	μA

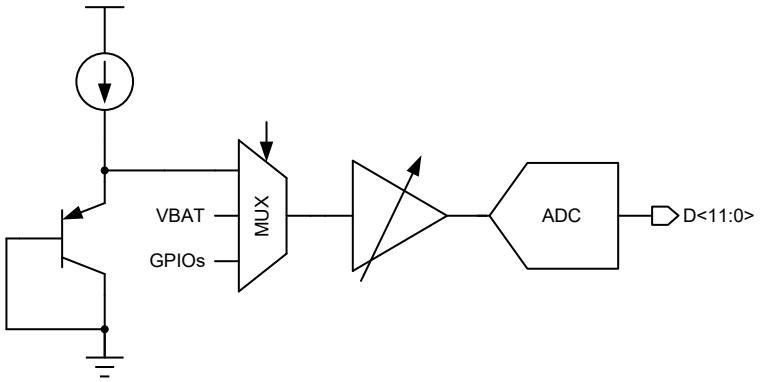


Figure 6. TSEN Operation Diagram

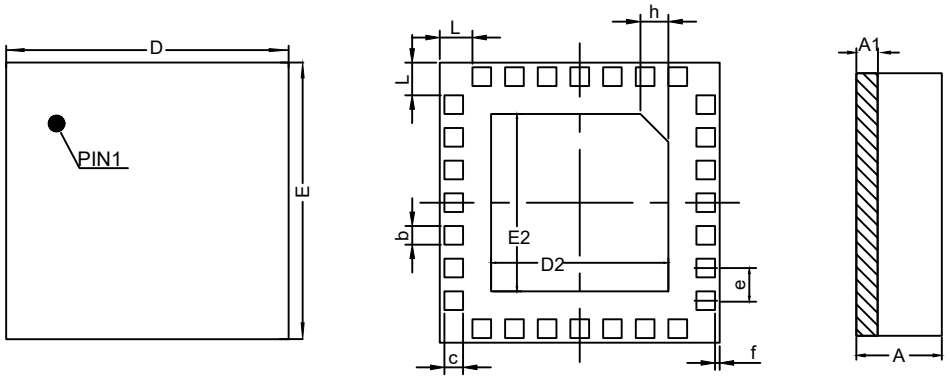
6 Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

28-pin LGA (3mm × 3mm × 0.75mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.024	0.026	0.028
A1	0.006	0.007	0.008
b	0.007	0.008	0.009
c	0.007	0.008	0.009
D	0.114	0.118	0.122
D2	0.071	0.075	0.079
e	0.013	0.014	0.015
E	0.114	0.118	0.122
E2	0.071	0.075	0.079
L	0.013	0.014	0.015
f	0.002	0.002	0.002
h	0.011	0.012	0.013

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.62	0.67	0.72
A1	0.14	0.17	0.20
b	0.17	0.20	0.23
c	0.17	0.20	0.23
D	2.90	3.00	3.10
D2	1.80	1.90	2.00
e	0.33	0.35	0.37
E	2.90	3.00	3.10
E2	1.80	1.90	2.00
L	0.33	0.35	0.37
f	0.045	0.05	0.055
h	0.28	0.30	0.32