# HT32F61041
# Datasheet

**32-Bit Arm® Cortex®-M0+ Power Delivery Microcontroller, 64 KB Flash and 8 KB SRAM with PD3.1, 1 Msps ADC, DIV, USART, UART, SPI, I²C, MCTM, GPTM, BFTM, PWM, CRC, RTC and WDT**

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# 1 General Description

The Holtek HT32F61041 device is a high performance, low power consumption 32-bit microcontroller based around an Arm® Cortex®-M0+ processor core. The Cortex®-M0+ is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer, and including advanced debug support.

The device operates at a frequency of up to 20 MHz to obtain maximum efficiency. It provides 64 KB of embedded Flash memory for code/data storage and 8 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as Hardware Divider DIV, ADC, $I^2C$, USART, UART, SPI, MCTM, GPTM, PWM, BFTM, CRC-16/32, RTC, WDT, SW-DP (Serial Wire Debug Port), etc., are also implemented in the device. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The device integrates USB Power Delivery (PD) PHY communication protocols and are compliant with USB PD 3.1/PPS specification.

The above features ensure that the device is suitable for use in a wide range of PD applications, especially in areas such as power bank, car charger and various products powered by PD protocol.

# 2 Features



## Core

- 32-bit Arm® Cortex®-M0+ processor core
- Up to 20 MHz operating frequency
- Single-cycle multiplication
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized, low-power processor. The processor is based on the ARMv6-M architecture and supports Thumb® instruction sets, single-cycle I/O ports, hardware multiplier and low latency interrupt respond time.

## On-Chip Memory

- 64 KB on-chip Flash memory for instruction/data and option byte storage
- 8 KB on-chip SRAM
- Supports multiple boot modes

The Arm® Cortex®-M0+ processor access and debug access share the single external interface to external AHB peripherals. The processor access takes priority over debug access. The maximum address range of the Cortex®-M0+ is 4 GB since it has a 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex®-M0+ processor to reduce the software complexity of repeated implementation by different device vendors. However, some regions are used by the Arm® Cortex®-M0+ system peripherals. Refer to the Arm® Cortex®-M0+ Technical Reference Manual for more information. Figure 2 in the Overview chapter shows the memory map of the device, including code, SRAM, peripheral and other pre-defined regions.

## Flash Memory Controller – FMC

- 32-bit word programming with In System Programming (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions for the embedded on-chip Flash Memory. The word program/page erase functions are also provided.

## Reset Control Unit – RSTCU

- Supply supervisor
  - Power on Reset / Power down Reset – POR / PDR
  - Brown-out Detector – BOD
  - Programmable Low Voltage Detector – LVD

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by external signals, internal events and the reset generators.

## Clock Control Unit – CKCU

- External 4 to 20 MHz crystal oscillator
- External 32.768 kHz crystal oscillator
- Internal 20 MHz RC oscillator trimmed to ±2 % accuracy at 25 °C operating temperature
- Internal 32 kHz RC oscillator
- Independent clock divider and gating bits for peripheral clock sources

The Clock Control Unit, CKCU, provides a range of oscillator and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), an HSE clock monitor, clock pre-scalers, clock multiplexers, APB clock divider and gating circuitry. The AHB, APB and Cortex®-M0+ clocks are derived from the system clock (CK_SYS) which can come from the HSI, HSE, LSI or LSE. The Watchdog Timer and Real-Time Clock (RTC) use either the LSI or LSE as their clock source.

## Power Management Control Unit – PWRCU

- Flexible power supply: $V_{DD}$ power supply (2.5 V ~ 5.5 V), $V_{DDIO}$ for I/Os (1.8 V ~ 5.5 V)
- Integrated 1.5 V LDO regulator for MCU core, peripherals and memories power supply
- $V_{DD}$, $V_{DDIO}$ and $V_{CORE}$ power domains
- Three power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in this device provides many types of power saving modes such as Sleep, Deep-Sleep1 and Deep-Sleep2 modes. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.

## Power Delivery

- Compliant with USB PD 3.1/PPS specification
- Supports Dual Role Port – DRP
- Supports Fast Role Swap – FRS
- Integrated VCONN Switch
- Integrated HVO switch output

Power Delivery has an integrated USB BMC encoding/decoding circuit, it can support Dual Role Port operation, PD 3.1 for allowing up to 240 W power supply and Programmable Power Supply, PPS. The CC1 and CC2 pins is used for Type-C identification and PD communication transmission, providing VCONN power for E-Mark cable. These two pins contain an over voltage protection circuit, which will disconnect the channel to protect the internal circuit when the voltage is too high. There are two HVO output pins used for the external MOS component on/off control.

## Real-Time Clock – RTC

- 24-bit up-counter with a programmable prescaler
- Alarm function
- Interrupt and Wake-up event

The Real-Time Clock, RTC, includes an APB interface, a 24-bit count-up counter, a control register, a prescaler, a compare register and a status register. The RTC circuits are located in the $V_{CORE}$ power domain. When the device enters the power-saving mode, the RTC counter is used as a wakeup timer to let the system resume from the power saving mode.

## External Interrupt/Event Controller – EXTI

- Up to 16 EXTI lines with configurable trigger source and type
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge or both edges
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

The External Interrupt/Event Controller, EXTI, comprises 16 edge detectors which can generate a wake-up event or interrupt requests independently. Each EXTI line can also be masked independently.

## Hardware Divider – DIV

- Signed/unsigned 32-bit divider
- Operation in 8 clock cycles, load in 1 clock cycle
- Division by zero error Flag

The divider is the truncated division and needs a software triggered start signal by controlling the "START" bit in the control register. The divider calculation complete flag will be set to 1 after 8 clock cycles, however, if the divisor register data is zero during the calculation, the divide by zero error flag will be set to 1.

## Analog to Digital Converter – ADC

- 12-bit SAR ADC engine
- Up to 1 Msps conversion rate
- Up to 9 external analog input channels

A 12-bit multi-channel Analog to Digital Converter is integrated in this device. There are multiplexed channels, which include 9 external analog signal channels and 2 internal channels which can be measured. If the input voltage is required to remain within a specific threshold window, an Analog Watchdog function will monitor and detect these signals. An interrupt will then be generated to inform the device that the input voltage is not within the preset thresholds. There are three conversion modes to convert an analog signal to digital data. The ADC can be operated in one shot, continuous and discontinuous conversion modes.

## I/O Ports – GPIO

- Up to 28 GPIOs
- Port A, B, C are mapped as 16 external interrupts – EXTI
- Almost all I/O pins have configurable output driving current

There are up to 28 General Purpose I/O pins, GPIO, for the implementation of logic input/output functions. Each of the GPIO ports has a series of related control and configuration registers to maximize flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

## Basic Function Timer – BFTM

- 32-bit compare match count-up counter – no I/O control
- One shot mode – counter stops counting when compare match occurs
- Repetitive mode – counter restarts when compare match occurs

The Basic Function Timer Module, BFTM, is a simple 32-bit up-counting counter designed to measure time intervals and generate a one shot or repetitive interrupts. The BFTM can operate in two modes, repetitive and one shot modes. In the repetitive mode, the counter will restart at each compare match event. The BFTM also supports a one shot mode which will force the counter to stop counting when a compare match event occurs.

## Motor Control Timer – MCTM

- 16-bit up, down, up/down auto-reload counter
- Up to 4 independent channels
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting
- Single Pulse Mode Output
- Complementary Outputs with programmable dead-time insertion
- Break input to force the timer's output signals into a reset or fixed condition

The Motor Control Timer Module, MCTM, consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR), one 8-bit repetition counter and several control/status registers. It can be used for a variety of purposes including measuring the pulse width of input signals or generating output waveforms such as compare match outputs, PWM outputs or complementary PWM outputs with dead-time insertion. The MCTM is capable of offering full functional support for motor control, hall sensor interfacing and break input.

## General-Purpose Timer – GPTM

- 16-bit up, down, up/down auto-reload counter
- Up to 4 independent channels
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting
- Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder

The General Purpose Timer Module, GPTM, consists of one 16-bit up/down-counter, four 16-bit Capture / Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR) and several control / status registers. It can be used for a variety of purposes including general time measurement, input signal pulse width measurement, output waveform generation such as single pulse generation or PWM output generation. The GPTM supports an Encoder Interface using a quadrature decoder with two inputs.

## Pulse-Width-Modulation Timer – PWM

- 16-bit up, down, up/down auto-reload counter
- Up to 4 independent channels for each timer
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting
- Single Pulse Mode Output

The Pulse-Width-Modulation Timer, PWM, consists of one 16-bit up/down-counter, four 16-bit Compare Registers (CRs), one 16-bit Counter-Reload Register (CRR) and several control / status registers. It can be used for a variety of purposes including general timer and output waveform generation such as single pulse generation or PWM output.

## Watchdog Timer – WDT

- 12-bit down counter with 3-bit prescaler
- Provides reset to the system
- Programmable watchdog timer window function
- Register write protection function

The Watchdog Timer is a hardware timing circuit that can be used to detect a system lock-up due to software trapped in a deadlock. It includes a 12-bit count-down counter, a prescaler, a WDT delta value register, WDT operation control circuitry and a WDT protection mechanism. If the software does not reload the counter value before a Watchdog Timer underflow occurs, a reset will be generated when the counter underflows. In addition, a reset is also generated if the software reloads the counter when it reaches a delta value. This means the counter must be reloaded within a limited timing window using a specific method. The Watchdog Timer counter can be stopped while the processor is in the debug mode. The register write protect function which can be enabled to prevent an unexpected change in the Watchdog timer configuration.

## Inter-integrated Circuit – $I^2C$

- Supports both master and slave modes with a frequency of up to 1 MHz
- Provides an arbitration function and clock synchronization
- Supports 7-bit and 10-bit addressing modes and general call addressing
- Supports slave multi-addressing mode with address mask function

The $I^2C$ is an internal circuit allowing communication with an external $I^2C$ interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The $I^2C$ module provides three data transfer rates: 100 kHz in the Standard mode, 400 kHz in the Fast mode and 1 MHz in the Fast plus mode. The SCL period generation register is used to setup different kinds of duty cycle implementations for the SCL pulse.

The SDA line which is connected directly to the $I^2C$ bus is a bi-directional data line between the master and slave devices and is used for data transmission and reception. The $I^2C$ also has an arbitration detect function and clock synchronization to prevent situations where more than one master attempts to transmit data to the $I^2C$ bus at the same time.

## Serial Peripheral Interface – SPI

- Supports both master and slave modes
- Frequency of up to ($f_{PCLK}$/2) MHz for the master mode and ($f_{PCLK}$/3) MHz for the slave mode
- FIFO Depth: 8 levels
- Multi-master and multi-slave operation

The Serial Peripheral Interface, SPI, provides a SPI protocol data transmit and receive function in both master and slave modes. The SPI interface uses 4 pins, which are the serial data input and output lines MISO and MOSI, the clock line, SCK, and the slave select line, SEL. One SPI device acts as a master device which controls the data flow using the SEL and SCK signals to indicate the start of data communication and the data sampling rate. To receive a data byte, the streamed data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but in a reverse sequence. The mode fault detection provides a capability for multi-master applications.

## Universal Synchronous Asynchronous Receiver Transmitter – USART

- Supports both asynchronous and clocked synchronous serial communication modes
- Programmable baud rate clock frequency up to ($f_{PCLK}$/16) MHz for Asynchronous mode and ($f_{PCLK}$/8) MHz for synchronous mode
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bits generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error
- Auto hardware flow control mode – RTS, CTS
- IrDA SIR encoder and decoder
- RS485 mode with output enable control
- FIFO Depth: 8-level for both receiver and transmitter

The Universal Synchronous Asynchronous Receiver Transceiver, USART, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. The USART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The USART peripheral function supports four types of interrupt including Line Status Interrupt, Transmitter FIFO Empty Interrupt, Receiver Threshold Level Reaching Interrupt and Time Out Interrupt. The USART module includes a transmitter FIFO (TX_FIFO) and receiver FIFO (RX_FIFO). The software can detect a USART error status by reading the USART Status & Interrupt Flag Register, USRSIFR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

## Universal Asynchronous Receiver Transmitter – UART

- Asynchronous serial communication operating baud-rate clock frequency up to ($f_{PCLK}$/16) MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bits generation
  - Bit order: LSB-first or MSB-first transfer

- Error detection: Parity, overrun and frame error

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports Line Status Interrupt. The software can detect a UART error status by reading the UART Status & Interrupt Flag Register, URSIFR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

## Cyclic Redundancy Check – CRC

- Supports CRC16 polynomial: 0x8005,
  $X^{16}+X^{15}+X^{2}+1$
- Supports CCITT CRC16 polynomial: 0x1021,
  $X^{16}+X^{12}+X^{5}+1$
- Supports IEEE-802.3 CRC32 polynomial: 0x04C11DB7,
  $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^{8}+X^{7}+X^{5}+X^{4}+X^{2}+X+1$
- Supports 1's complement, byte reverse & bit reverse operation on data and checksum
- Supports byte, half-word & word data size
- Programmable CRC initial seed value
- CRC computation executed in 1 AHB clock cycle for 8-bit data and 4 AHB clock cycles for 32-bit data

The CRC calculation unit is an error detection technique test algorithm which is used to verify data transmission or storage data correctness. A CRC calculation takes a data stream or a block of data as its input and generates a 16-bit or 32-bit output remainder. Ordinarily, a data stream is suffixed by a CRC code and used as a checksum when being sent or stored. Therefore, the received or restored data stream is calculated by the same generator polynomial as described above. If the new CRC code result does not match the one calculated earlier, that means the data stream contains a data error.

## Debug Support

- Serial Wire Debug Port – SW-DP
- 4 comparators for hardware breakpoint or code / literal patch
- 2 comparators for hardware watch points

## Package and Operation Temperature

- 46-pin QFN package
- Operation temperature range: -40 °C to 85 °C

# 3 Overview

## Device Information

**Table 1. Features and Peripheral List**

| Peripherals | | HT32F61041 |
|---|---|---|
| Main Flash (KB) | | 63 |
| Option Bytes Flash (KB) | | 1 |
| SRAM (KB) | | 8 |
| Timers | MCTM | 1 |
| | GPTM | 1 |
| | PWM | 2 |
| | BFTM | 2 |
| | WDT | 1 |
| | RTC | 1 |
| Communication | SPI | 2 |
| | USART | 1 |
| | UART | 2 |
| | $I^2C$ | 2 |
| Hardware Divider | | 1 |
| CRC-16/32 | | 1 |
| EXTI | | 16 |
| 12-bit ADC | | 1 |
| Number of channels | | 9 Channels |
| Power Delivery | | 1 |
| GPIO | | Up to 28 |
| CPU frequency | | Up to 20 MHz |
| Operating voltage | | 2.5 V ~ 5.5 V |
| Operating temperature | | -40 °C ~ 85 °C |
| Package | | 46-pin QFN |

Note: The functions listed here, except the Power Delivery, are compatible with the HT32F50241 device. Refer to the HT32F50231/HT32F50241 user manual for detailed functional description.

# Block Diagram

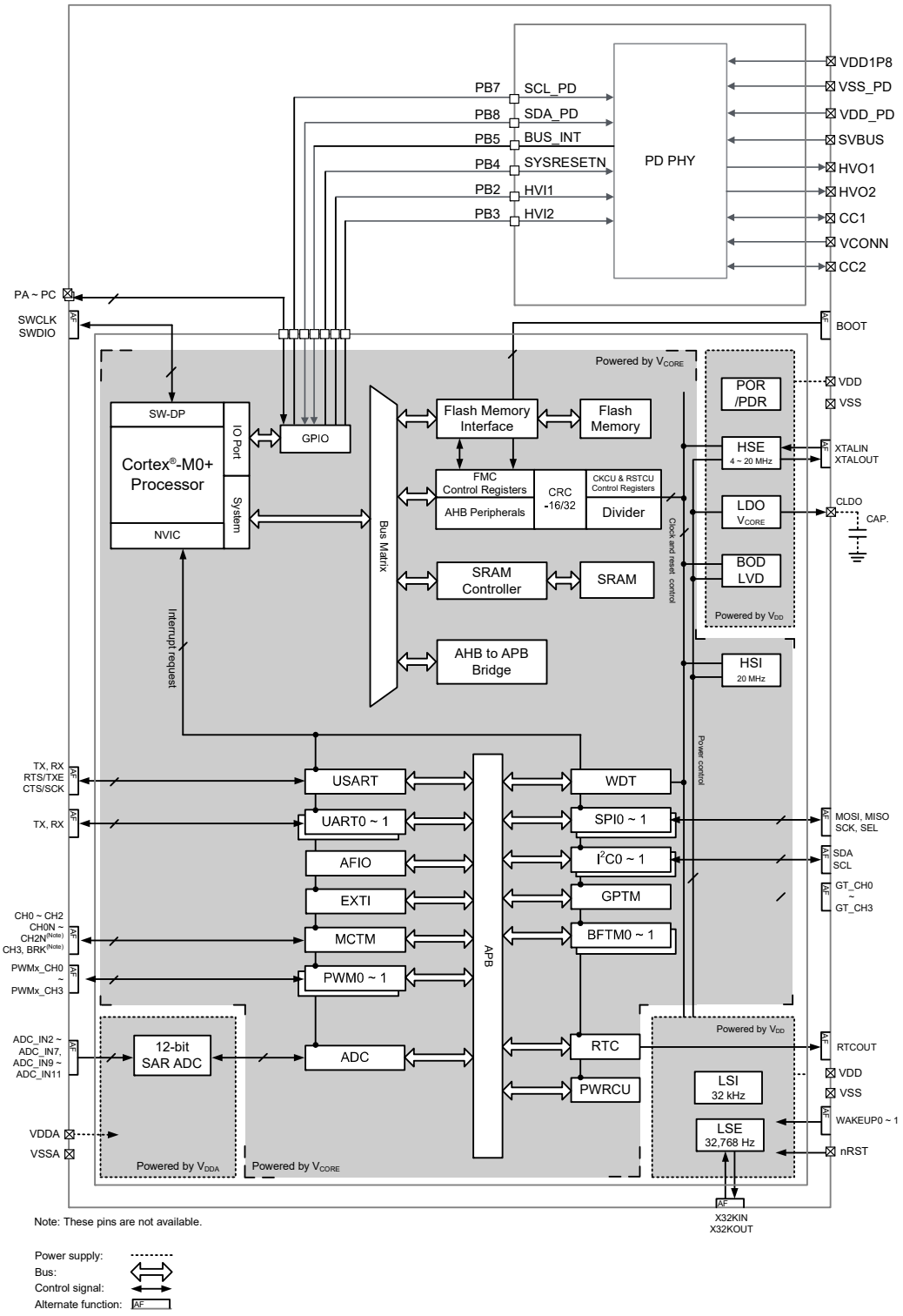



**Figure 1. Block Diagram**

## Memory Map

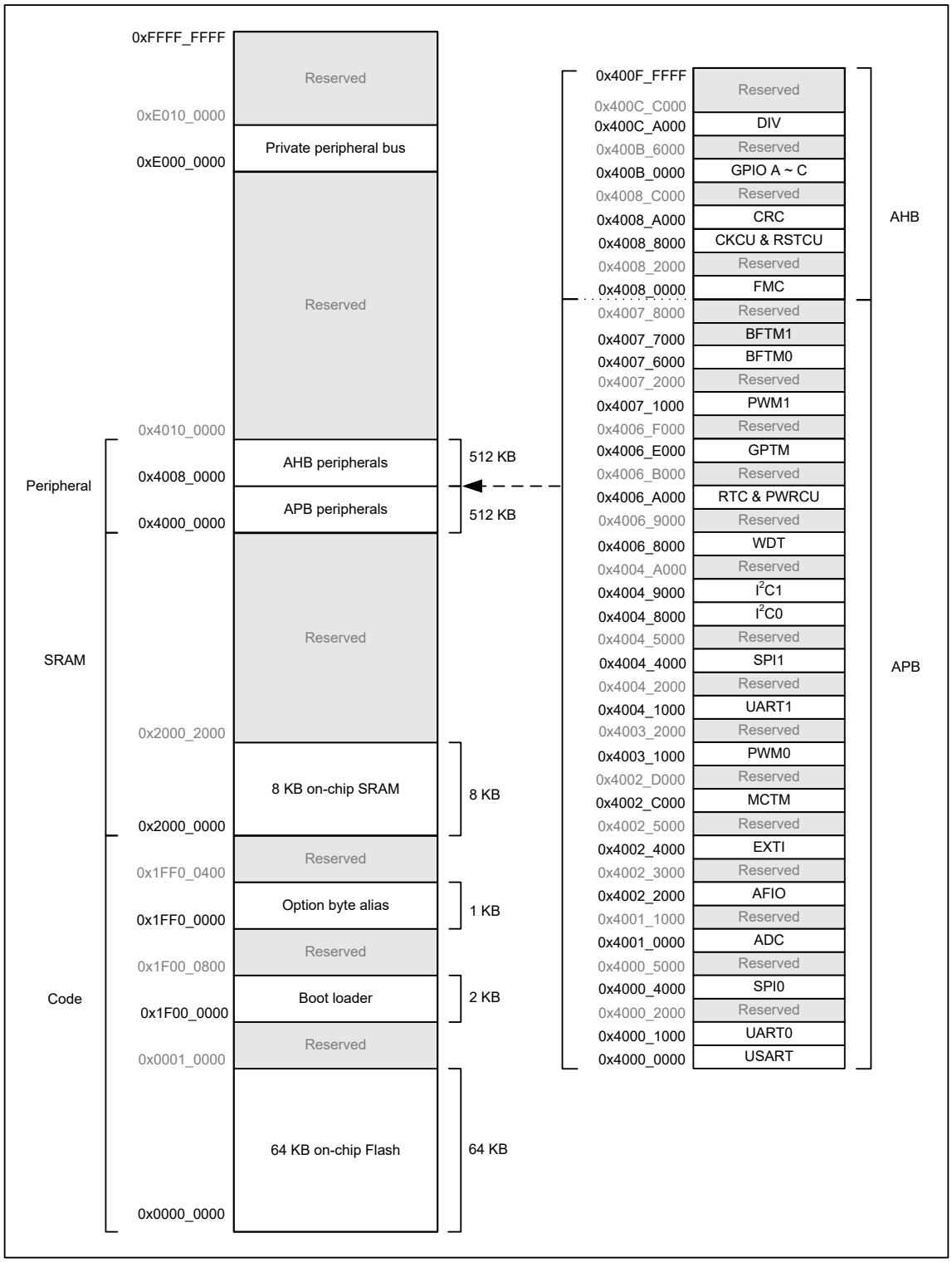



**Figure 2. Memory Map**

**Table 2. Register Map**

| Start Address | End Address | Peripheral | Bus |
|---|---|---|---|
| 0x4000_0000 | 0x4000_0FFF | USART | |
| 0x4000_1000 | 0x4000_1FFF | UART0 | |
| 0x4000_2000 | 0x4000_3FFF | Reserved | |
| 0x4000_4000 | 0x4000_4FFF | SPI0 | |
| 0x4000_5000 | 0x4000_FFFF | Reserved | |
| 0x4001_0000 | 0x4001_0FFF | ADC | |
| 0x4001_1000 | 0x4002_1FFF | Reserved | |
| 0x4002_2000 | 0x4002_2FFF | AFIO | |
| 0x4002_3000 | 0x4002_3FFF | Reserved | |
| 0x4002_4000 | 0x4002_4FFF | EXTI | |
| 0x4002_5000 | 0x4002_BFFF | Reserved | |
| 0x4002_C000 | 0x4002_CFFF | MCTM | |
| 0x4002_D000 | 0x4003_0FFF | Reserved | |
| 0x4003_1000 | 0x4003_1FFF | PWM0 | |
| 0x4003_2000 | 0x4004_0FFF | Reserved | |
| 0x4004_1000 | 0x4004_1FFF | UART1 | |
| 0x4004_2000 | 0x4004_3FFF | Reserved | APB |
| 0x4004_4000 | 0x4004_4FFF | SPI1 | |
| 0x4004_5000 | 0x4004_7FFF | Reserved | |
| 0x4004_8000 | 0x4004_8FFF | $I^2C0$ | |
| 0x4004_9000 | 0x4004_9FFF | $I^2C1$ | |
| 0x4004_A000 | 0x4006_7FFF | Reserved | |
| 0x4006_8000 | 0x4006_8FFF | WDT | |
| 0x4006_9000 | 0x4006_9FFF | Reserved | |
| 0x4006_A000 | 0x4006_AFFF | RTC & PWRCU | |
| 0x4006_B000 | 0x4006_DFFF | Reserved | |
| 0x4006_E000 | 0x4006_EFFF | GPTM | |
| 0x4006_F000 | 0x4007_0FFF | Reserved | |
| 0x4007_1000 | 0x4007_1FFF | PWM1 | |
| 0x4007_2000 | 0x4007_5FFF | Reserved | |
| 0x4007_6000 | 0x4007_6FFF | BFTM0 | |
| 0x4007_7000 | 0x4007_7FFF | BFTM1 | |
| 0x4007_8000 | 0x4007_FFFF | Reserved | |

| Start Address | End Address | Peripheral | Bus |
|---|---|---|---|
| 0x4008_0000 | 0x4008_1FFF | FMC | AHB |
| 0x4008_2000 | 0x4008_7FFF | Reserved | |
| 0x4008_8000 | 0x4008_9FFF | CKCU & RSTCU | |
| 0x4008_A000 | 0x4008_BFFF | CRC | |
| 0x4008_C000 | 0x400A_FFFF | Reserved | |
| 0x400B_0000 | 0x400B_1FFF | GPIOA | |
| 0x400B_2000 | 0x400B_3FFF | GPIOB | |
| 0x400B_4000 | 0x400B_5FFF | GPIOC | |
| 0x400B_6000 | 0x400C_9FFF | Reserved | |
| 0x400C_A000 | 0x400C_BFFF | DIV | |
| 0x400C_C000 | 0x400F_FFFF | Reserved | |

## Clock Structure

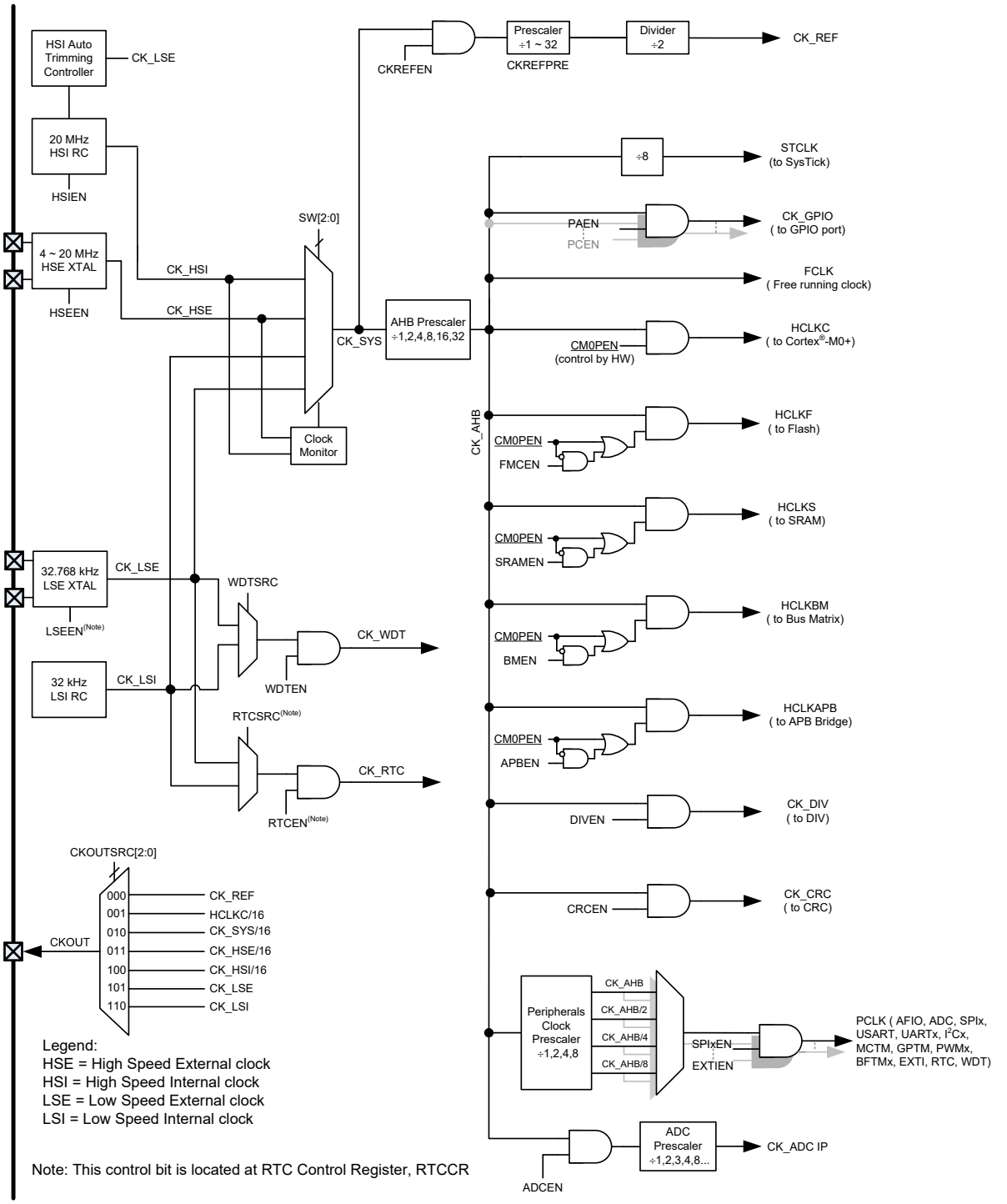



**Figure 3. Clock Structure**

# 4 PD PHY

Power Delivery, known as PD, is a USB charging standard and technology released by the USB-IF. It uses Type-C interface to implement PD fast charging. With a power output of up to 240 W, it can charge mobile phones, tablet and notebook computers. The high wattage output can even provide power for monitors, televisions, etc., and the Type-C interface can support two-way charging, making it more flexible in use.

The device contains a transceiver control circuit compliant with PD standard. With integrated USB BMC encoding/decoding circuit, it can support Dual Role Port operation, PD 3.1 for allowing up to 240 W power supply and Programmable Power Supply, PPS. The CC1 and CC2 pins is used for Type-C identification and PD communication transmission, providing VCONN power for E-Mark cable. These two pins contain an over voltage protection circuit, which will disconnect the channel to protect the internal circuit when the voltage is too high. There are two HVO output pins used for the external MOS component on/off control. The PD transceiver control circuit contains an independent control register space. The device writes or reads PD register data using the $I^2C$ interface (master mode) to implement USB Type-C PD communication transmission.

The device has six PD modes. Users can select a PD mode according to their requirements and turn on Type-C detection to start PD communication. When an external PD device is connected, the Type-C identification will automatically be executed. After the identification is completed, an interrupt signal will be generated to inform the device. The device will read data from PD registers using the $I^2C$ interface and then determine to carry out PD charging or discharging transmission according to the identification result. The PD charge/discharge communication is transmitted and received by MCU writing or reading PD register TX/RX buffer data via the $I^2C$ interface. The PD protocol communication process is implemented in accordance with PD specification content stipulated by the USB-IF.

## PD PHY Registers Type

**Table 3. PD PHY Register Type**

| Bit Type | Definition |
|---|---|
| RO | Read only |
| WC | Write with 1 which in automatically cleared by hardware |
| RW | Readable and writeable |
| RWH | Readable and writable which can be overwritten by hardware |
| RC | Readable interrupt bits, cleared on read |

## PD PHY Registers

Overall operation of the PD PHY is controlled using a series of registers.

**Table 4. PD PHY Register List**

| Register Name | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VERSION | INT_RES | — | — | — | — | — | — | — |
| USB_C_CTL1 | DRP_TOG-GL7 | DRP_TOG-GL6 | DRP_TOG-GL5 | CURR_SRC4 | CURR_SRC3 | MODES2 | MODES1 | MODES0 |
| USB_C_CTL2 | UNSUP_ACC | TRY_SRC | ATT_SRC | ATT_SNK | ERR_REC | DIS_ST | UNATT_SRC | UNATT_SNK |

| Register Name | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| USB_C_CTL3 | — | — | VBUS_IG-NORE | — | — | RESETPHY | — | DET_DIS |
| CC1_CON-TROL | VBUSOK | — | — | — | PDWN1 | TXE1 | VCONN1 | PU1 |
| CC2_CON-TROL | VBUSOK | — | — | — | PDWN2 | TXE2 | VCONN2 | PU2 |
| CC_SEL | — | — | — | — | VCONN_ SWAP_OFF | VCONN_ SWAP_ON | CC_SEL1 | CC_SEL0 |
| USB_C_STA-TUS1 | TYPE_C_ DET7 | TYPE_C_ DET6 | CC_ORI-ENT5 | CC_ORI-ENT4 | TYPE_C_ RSLT3 | TYPE_C_ RSLT2 | TYPE_C_ RSLT1 | TYPE_C_ RSLT0 |
| USB_C_STA-TUS2 | — | — | VBUS_REQ | PD_NOT_ ALLOWED | — | — | OVRTEMP | SHORT |
| USB_C_STA-TUS3 | TYPEC_AC-TIVE | — | — | — | — | — | — | — |
| CC1_CMP | — | — | — | DET_3A | DET_1P5A | DET_DEF | DET_RD | DET_RA |
| CC2_CMP | — | — | — | DET_3A | DET_1P5A | DET_DEF | DET_RD | DET_RA |
| CC1_STATUS | — | SRC_RX16 | SRC_RX15 | SRC_RP1 | PWR3A_ SNK1 | PWR1P5A_ SNK1 | PWRDEF_ SNK1 | SNK_RP1 |
| CC2_STATUS | — | SRC_RX26 | SRC_RX25 | SRC_RP2 | PWR3A_ SNK2 | PWR1P5A_ SNK2 | PWRDEF_ SNK2 | SNK_RP2 |
| VBUS_MON | VBUS_ MON_EN | COMP | DAC5 | DAC4 | DAC3 | DAC2 | DAC1 | DAC0 |
| AFE_TRIM2 | — | — | — | — | — | — | TRIM_ CCDRV1 | TRIM_ CCDRV0 |
| AFE_TRIM3 | — | TRIM_ SLICE2 | TRIM_ SLICE1 | TRIM_ SLICE0 | — | — | — | — |
| POWER | VCONN_ CTRL_EXT | — | — | — | PWR3 | PWR2 | PWR1 | PWR0 |
| IRQ1 | — | — | — | — | I_VBUS_ DROP | — | I_OVRTEMP | I_SHORT |
| IRQ2 | I_CC_ CHANGE | I_PD_RX | I_PD_HR_ RX | I_PD_CR_ RX | I_PD_TX_ OK | I_PD_TX_ FAIL | I_FAST_ SWAP | I_TX_DIS-CARD |
| IRQ_MSK1 | — | — | — | — | M_VBUS_ DROP | — | M_OVR-TEMP | M_SHORT |
| IRQ_MSK2 | M_CC_ CHANGE | M_PD_RX | M_PD_HR_ RX | M_PD_CR_ RX | M_PD_TX_ OK | M_PD_TX_ FAIL | M_FAST_ SWAP | — |
| PD_CFG1 | ID_INSERT | VBUS_ HIGH_VOLT | GUIDE_ TRY_SNK | — | RESET_ MSG_ID | SOP_TO_ RESET2 | SOP_TO_ RESET1 | SOP_TO_ RESET0 |
| PD_CFG2 | FAST_ SWAP_SNK | FAST_ SWAP_SRC | CDR_SE-LECT | SOP_RCV4 | SOP_RCV3 | SOP_RCV2 | SOP_RCV1 | SOP_RCV0 |
| PD_CFG3 | — | — | P_DATA_ ROLE_DP | P_PWR_ ROLE_DP | P_DATA_ ROLE_PR | P_PWR_ ROLE_PR | P_DATA_ ROLE_SOP | P_PWR_ ROLE_SOP |
| SHORT_PRO-TECT | SHORT_ RESET | SHORT_ TIME6 | SHORT_ TIME5 | SHORT_ TIME4 | SHORT_ TIME3 | SHORT_ TIME2 | SHORT_ TIME1 | SHORT_ TIME0 |
| PD_STATUS | FAST_ SWAP | — | RX_RE-SULT5 | RX_RE-SULT4 | RX_RE-SULT3 | TX_RE-SULT2 | TX_RE-SULT1 | TX_RE-SULT0 |
| RX_STATUS | RX_DATA | RX_OVER-RUN | — | — | — | — | — | RX_CLEAR |
| RX_INFO | RX_BYTES7 | RX_BYTES6 | RX_BYTES5 | RX_BYTES4 | RX_BYTES3 | RX_SOP2 | RX_SOP1 | RX_SOP0 |
| TX_COM-MAND | TX_CMD7 | TX_CMD6 | TX_CMD5 | — | — | TX_WAIT_ RP | TX_START | TXBUF_ READY |
| TX_INFO | — | — | TX_RE-TRIES5 | TX_RE-TRIES4 | TX_RE-TRIES3 | TX_SOP2 | TX_SOP1 | TX_SOP0 |

| Register Name | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RX_PACKET_DATA61 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RX_PACKET_DATA62 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RX_PACKET_DATA63 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RX_PACKET_DATA64 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RX_PACKET_DATA65 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RX_PACKET_DATA66 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RX_PACKET_DATA67 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RX_PACKET_DATA68 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RX_PACKET_DATA69 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RX_PACKET_DATA70 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RX_PACKET_DATA71 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RX_PACKET_DATA72 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RX_PACKET_DATA73 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RX_PACKET_DATA74 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RX_PACKET_DATA75 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RX_PACKET_DATA76 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RX_PACKET_DATA77 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RX_PACKET_DATA78 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RX_PACKET_DATA79 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RX_PACKET_DATA80 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RX_PACKET_DATA81 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RX_PACKET_DATA82 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RX_PACKET_DATA83 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RX_PACKET_DATA84 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RX_PACKET_DATA85 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RX_PACKET_DATA86 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RX_PACKET_DATA87 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| Register Name | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RX_PACKET_DATA88 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RX_PACKET_DATA89 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RX_PACKET_DATA90 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TX_PACKET_DATA91 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TX_PACKET_DATA92 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TX_PACKET_DATA93 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TX_PACKET_DATA94 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TX_PACKET_DATA95 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TX_PACKET_DATA96 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TX_PACKET_DATA97 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TX_PACKET_DATA98 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TX_PACKET_DATA99 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TX_PACKET_DATA100 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TX_PACKET_DATA101 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TX_PACKET_DATA102 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TX_PACKET_DATA103 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TX_PACKET_DATA104 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TX_PACKET_DATA105 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TX_PACKET_DATA106 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TX_PACKET_DATA107 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TX_PACKET_DATA108 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TX_PACKET_DATA109 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TX_PACKET_DATA110 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TX_PACKET_DATA111 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TX_PACKET_DATA112 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TX_PACKET_DATA113 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TX_PACKET_DATA114 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| Register Name | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TX_PACKET_DATA115 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TX_PACKET_DATA116 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TX_PACKET_DATA117 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TX_PACKET_DATA118 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TX_PACKET_DATA119 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TX_PACKET_DATA120 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| C_OVP | — | — | — | — | ENP2 | ENP1 | STP2 | STP1 |



The following table indicates the way in which the PD PHY internal registers are affected after a power-on reset occurs.

**Table 5. PD PHY Register Reset List**

| Address | Register | Power On Reset |
|---|---|---|
| 00H | VERSION | 0--- ---- |
| 01H | USB_C_CTL1 | 0000 1000 |
| 02H | USB_C_CTL2 | 0000 0000 |
| 03H | USB_C_CTL3 | --0- -0-0 |
| 04H | CC1_CONTROL | 1--- 1000 |
| 05H | CC2_CONTROL | 1--- 1000 |
| 06H | CC_SEL | ---- 0000 |
| 07H | USB_C_STATUS1 | 0000 0000 |
| 08H | USB_C_STATUS2 | --00 --00 |
| 09H | USB_C_STATUS3 | 1--- ---- |
| 0AH | CC1_CMP | ---0 0000 |
| 0BH | CC2_CMP | ---0 0000 |
| 0CH | CC1_STATUS | -000 0000 |
| 0DH | CC2_STATUS | -000 0000 |
| 0FH | VBUS_MON | 0000 0000 |
| 11H | AFE_TRIM2 | ---- --10 |
| 12H | AFE_TRIM3 | -000 ---- |
| 14H | POWER | 0--- 1111 |
| 16H | IRQ1 | ---- 0-00 |
| 17H | IRQ2 | 1000 0000 |
| 18H | IRQ_MSK1 | ---- 0-00 |
| 19H | IRQ_MSK2 | 0000 000- |
| 1AH | PD_CFG1 | 000- 0000 |
| 1BH | PD_CFG2 | 0000 0000 |
| 1CH | PD_CFG3 | --00 0000 |
| 1DH | SHORT_PROTECT | 0010 1001 |
| 1EH | PD_STATUS | 0-00 0000 |
| 1FH | RX_STATUS | 00-- ---0 |
| 20H | RX_INFO | 0000 0000 |

| Address | Register | Power On Reset |
|---|---|---|
| 21H | TX_COMMAND | 000- -001 |
| 22H | TX_INFO | --01 1000 |
| 3DH | RX_PACKET_DATA61 | 0000 0000 |
| 3EH | RX_PACKET_DATA62 | 0000 0000 |
| 3FH | RX_PACKET_DATA63 | 0000 0000 |
| 40H | RX_PACKET_DATA64 | 0000 0000 |
| 41H | RX_PACKET_DATA65 | 0000 0000 |
| 42H | RX_PACKET_DATA66 | 0000 0000 |
| 43H | RX_PACKET_DATA67 | 0000 0000 |
| 44H | RX_PACKET_DATA68 | 0000 0000 |
| 45H | RX_PACKET_DATA69 | 0000 0000 |
| 46H | RX_PACKET_DATA70 | 0000 0000 |
| 47H | RX_PACKET_DATA71 | 0000 0000 |
| 48H | RX_PACKET_DATA72 | 0000 0000 |
| 49H | RX_PACKET_DATA73 | 0000 0000 |
| 4AH | RX_PACKET_DATA74 | 0000 0000 |
| 4BH | RX_PACKET_DATA75 | 0000 0000 |
| 4CH | RX_PACKET_DATA76 | 0000 0000 |
| 4DH | RX_PACKET_DATA77 | 0000 0000 |
| 4EH | RX_PACKET_DATA78 | 0000 0000 |
| 4FH | RX_PACKET_DATA79 | 0000 0000 |
| 50H | RX_PACKET_DATA80 | 0000 0000 |
| 51H | RX_PACKET_DATA81 | 0000 0000 |
| 52H | RX_PACKET_DATA82 | 0000 0000 |
| 53H | RX_PACKET_DATA83 | 0000 0000 |
| 54H | RX_PACKET_DATA84 | 0000 0000 |
| 55H | RX_PACKET_DATA85 | 0000 0000 |
| 56H | RX_PACKET_DATA86 | 0000 0000 |
| 57H | RX_PACKET_DATA87 | 0000 0000 |
| 58H | RX_PACKET_DATA88 | 0000 0000 |
| 59H | RX_PACKET_DATA89 | 0000 0000 |
| 5AH | RX_PACKET_DATA90 | 0000 0000 |
| 5BH | TX_PACKET_DATA91 | 0000 0000 |
| 5CH | TX_PACKET_DATA92 | 0000 0000 |
| 5DH | TX_PACKET_DATA93 | 0000 0000 |
| 5EH | TX_PACKET_DATA94 | 0000 0000 |
| 5FH | TX_PACKET_DATA95 | 0000 0000 |
| 60H | TX_PACKET_DATA96 | 0000 0000 |
| 61H | TX_PACKET_DATA97 | 0000 0000 |
| 62H | TX_PACKET_DATA98 | 0000 0000 |
| 63H | TX_PACKET_DATA99 | 0000 0000 |
| 64H | TX_PACKET_DATA100 | 0000 0000 |
| 65H | TX_PACKET_DATA101 | 0000 0000 |
| 66H | TX_PACKET_DATA102 | 0000 0000 |
| 67H | TX_PACKET_DATA103 | 0000 0000 |
| 68H | TX_PACKET_DATA104 | 0000 0000 |

| Address | Register | Power On Reset |
|---|---|---|
| 69H | TX_PACKET_DATA105 | 0000 0000 |
| 6AH | TX_PACKET_DATA106 | 0000 0000 |
| 6BH | TX_PACKET_DATA107 | 0000 0000 |
| 6CH | TX_PACKET_DATA108 | 0000 0000 |
| 6DH | TX_PACKET_DATA109 | 0000 0000 |
| 6EH | TX_PACKET_DATA110 | 0000 0000 |
| 6FH | TX_PACKET_DATA111 | 0000 0000 |
| 70H | TX_PACKET_DATA112 | 0000 0000 |
| 71H | TX_PACKET_DATA113 | 0000 0000 |
| 72H | TX_PACKET_DATA114 | 0000 0000 |
| 73H | TX_PACKET_DATA115 | 0000 0000 |
| 74H | TX_PACKET_DATA116 | 0000 0000 |
| 75H | TX_PACKET_DATA117 | 0000 0000 |
| 76H | TX_PACKET_DATA118 | 0000 0000 |
| 77H | TX_PACKET_DATA119 | 0000 0000 |
| 78H | TX_PACKET_DATA120 | 0000 0000 |
| 7DH | C_OVP | ---- 0000 |

- **VERSION Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | INT_RES | — | — | — | — | — | — | — |
| R/W | R/W | RO | RO | RO | RO | RO | RO | RO |
| POR | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

Bit 7 **INT_RES**: Interrupts Reset control
0: Reset interrupts by reading
1: Reset interrupts by writing "1" to the bits to be cleared

Bit 6~0 Unimplemented, read as "0"

- **USB_C_CTL1 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DRP_ TOGGL7 | DRP_ TOGGL6 | DRP_ TOGGL5 | CURR_ SRC4 | CURR_ SRC3 | MODES2 | MODES1 | MODES0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

Bit 7~5 **DRP_TOGGL7~DRP_TOGGL5**: Type-C State Machine configuration
000: 50 % in Unattached.SNK State and 50 % in Unattached.SRC
001: 40 % in Unattached.SNK State and 60 % in Unattached.SRC
010: 30 % in Unattached.SNK State and 70 % in Unattached.SRC
011: Reserved
100: Reserved
101: 60 % in Unattached.SNK State and 40 % in Unattached.SRC
110: 70 % in Unattached.SNK State and 30 % in Unattached.SRC
111: Pseudo randomly change the ratio between Unattached.SNK and Unattached.SRC between 34 % and 66 %

Bit 4~3 **CURR_SRC4~CURR_SRC3**: $R_P$ pull-up current selection
00: No current
01: 80 μA – Default current capability
10: 180 μA – 1.5 A current capability
11: 330 μA – 3 A current capability

Bit 2~0 **MODES2~MODE0**: PD mode selection
000: SNK (start in sink mode. No Accessory support.)
001: SNK + Accessory Support
010: SRC (start in source mode. No Accessory support.)
011: SRC + Accessory Support
100: DRP (dual role port – will toggle (refer to the DRP_TOGGL[7:5] bits)
101: DRP + Accessory Support
110: Reserved
111: Reserved
Note: This bit field selects which State Machine is used. The ATT_SRC and ATT_SNK bits can be used to switch state machines between source and sink during PR-swap (refer to the USB_C_CTL2 register).

- **USB_C_CTL2 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | UNSUP_ACC | TRY_SRC | ATT_SRC | ATT_SNK | ERR_REC | DIS_ST | UNATT_SRC | UNATT_SNK |
| R/W | WC | R/W | WC | WC | WC | WC | WC | WC |
| POR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7 **UNSUP_ACC**: Unsupported Accessory control
0: No effect
1: Unsupported Accessory – use if software does not know how to support this accessory
When this bit is set high, go to the Unsupported Accessory state if the software does not support this powered accessory.

Bit 6 **TRY_SRC**: TRY.SRC mode control
0: No effect
1: TRY.SRC mode enabled

Bit 5 **ATT_SRC**: Attached.SRC control
0: No effect
1: Set Type-C circuit in Attached.SRC State
When this bit is set high, go to Attached.SRC state, done with a Power Role Swap and valid only from Attached.SNK state.

Bit 4 **ATT_SNK**: Attached.SNK control
0: No effect
1: Set Type-C circuit in Attached.SNK State
When this bit is set high, go to Attached.SNK state, done with a Power Role Swap and valid only from Attached.SRC state.

Bit 3 **ERR_REC**: Type-C circuit ErrorRecovery State control
0: No effect
1: Set Type-C circuit in ErrorRecovery State
When this bit is set high, go to ErrorRecovery state, valid from any state.

Bit 2 **DIS_ST**: Type-C circuit Disabled State control
0: No effect
1: Set Type-C circuit in Disabled State
When this bit is set high, go to Disabled state, valid from any state.

Bit 1 **UNATT_SRC**: Type-C circuit Unattached.SRC State control
0: No effect
1: Set Type-C circuit in Unattached.SRC State – provided the FSM is in an appropriate state

Bit 0 **UNATT_SNK**: Type-C circuit Unattached.SNK State control
0: No effect
1: Set Type-C circuit in Unattached.SNK State – provided the FSM is in an appropriate state

- **USB_C_CTL3 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | VBUS_IGNORE | — | — | RESETPHY | — | DET_DIS |
| R/W | — | — | R/W | — | — | WC | — | R/W |
| POR | — | — | 0 | — | — | 0 | — | 0 |

Bit 7~6 Unimplemented, read as "0"

Bit 5 **VBUS_IGNORE**: VBUS ignore selection
0: Use VBUS for state change
1: Ignore VBUS during PR-swap

Bit 4~3 Unimplemented, read as "0"

Bit 2 **RESETPHY**: PD PHY logic reset control
0: Normal operation
1: Force reset of PD logic – Does not reset registers

Bit 1 Unimplemented, read as "0"

Bit 0 **DET_DIS**: Type-C detection control
0: Type-C detection enabled
1: Type-C detection disabled – Control only by software, ignore FSM

- **CC1_CONTROL Registe**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VBUSOK | — | — | — | PDWN1 | TXE1 | VCONN1 | PU1 |
| R/W | RO | — | — | — | RWH | RWH | RWH | RWH |
| POR | 1 | — | — | — | 1 | 0 | 0 | 0 |

Bit 7 **VBUSOK**: VBUS active status
0: VBUS is not active
1: VBUS is active

Bit 6~4 Unimplemented, read as "0"

Bit 3 **PDWN1**: 5.1 kΩ pull down resistor to CC1 control
0: Disable
1: Enable

Bit 2 **TXE1**: CC1 PD driver control
0: Disable
1: Enable

Bit 1 **VCONN1**: VCONN power to CC1 control
0: Disable
1: Enable

Bit 0 **PU1**: Pull up current to CC1 control
0: Disable
1: Enable

- **CC2_CONTROL Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VBUSOK | — | — | — | PDWN2 | TXE2 | VCONN2 | PU2 |
| R/W | RO | — | — | — | RWH | RWH | RWH | RWH |
| POR | 1 | — | — | — | 1 | 0 | 0 | 0 |

Bit 7 **VBUSOK**: VBUS active status
0: VBUS is not active
1: VBUS is active

Bit 6~4 Unimplemented, read as "0"

Bit 3 **PDWN2**: 5.1 kΩ pull down resistor to CC2 control
0: Disable
1: Enable

Bit 2 **TXE2**: CC2 PD driver control
0: Disable
1: Enable

Bit 1 **VCONN2**: VCONN power to CC2 control
0: Disable
1: Enable

Bit 0 **PU2**: Pull up current to CC2 control
0: Disable
1: Enable

- **CC_SEL Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | VCONN_SWAP_OFF | VCONN_SWAP_ON | CC_SEL1 | CC_SEL0 |
| R/W | — | — | — | — | WC | WC | RWH | RWH |
| POR | — | — | — | — | 0 | 0 | 0 | 0 |

Bit 7~4 Unimplemented, read as "0"

Bit 3 **VCONN_SWAP_OFF**: VCONN via Type-C FSM control
0: Reserved
1: Turn off

Bit 2 **VCONN_SWAP_ON**: VCONN via Type-C FSM control
0: Reserved
1: Turn on

Bit 1~0 **CC_SEL1~CC_SEL0**: CC2 PD driver control
00: Reserved
01: CC1 select
10: CC2 select
11: Reserved

### • USB_C_STATUS1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TYPE_C_DET7 | TYPE_C_DET6 | CC_ORIENT5 | CC_ORIENT4 | TYPE_C_RSLT3 | TYPE_C_RSLT2 | TYPE_C_RSLT1 | TYPE_C_RSLT0 |
| R/W | RO | RO | RO | RO | RO | RO | RO | RO |
| POR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7~6 **TYPE_C_DET7~TYPE_C_DET6**: Type-C detection status
00: Type-C detection has not started
01: Type-C detection is ongoing
10: Type-C detection is completed (Type-C result may be read)
11: Reserved

Bit 5~4 **CC_ORIENT5~CC_ORIENT4**: CC1/CC2 connection status
00: No or unresolved connection is detected
01: Position 1 (Normal Orientation – CC1)
10: Position 2 (Normal Orientation – CC2)
11: A fault has occurred during detection

Bit 3~0 **TYPE_C_RSLT3~TYPE_C_RSLT0**: Type-C detection result status
0000: Nothing is attached
0001: SRC with Default current capability is attached
0010: SRC with 1.5 A current capability is attached
0011: SRC with 3 A current capability is attached
0100: SNK is attached
0101: Debug Accessory is attached
0110: Audio Accessory is attached
0111: Powered Accessory is attached
1000~1110: Reserved
1111: Undetermined

### • USB_C_STATUS2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | VBUS_REQ | PD_NOT_ALLOWED | — | — | OVRTEMP | SHORT |
| R/W | — | — | RO | RO | — | — | RO | RO |
| POR | — | — | 0 | 0 | — | — | 0 | 0 |

Bit 7~6 Unimplemented, read as "0"

Bit 5 **VBUS_REQ**: Indicates the state the VBUS switch should be on
0: VBUS is not required
1: VBUS is now required

Bit 4 **PD_NOT_ALLOWED**: PD allowed status
0: PD is allowed
1: PD is not allowed

Bit 3~2 Unimplemented, read as "0"

Bit 1 **OVRTEMP**: Over temperature status
0: Not over temperature
1: Over temperature

Bit 0 **SHORT**: Reflect short logic input
This indicates that the VCONN output voltage switch is on and there is an unsafe voltage across it. This signal will typically glitch when VCONN is turned on, and remain high during an overcurrent situation. A sustained short signal will cause an I_SHORT interrupt. Hence this bit is normally used only for debug.

- **USB_C_STATUS3 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TYPEC_ACTIVE | — | — | — | — | — | — | — |
| R/W | RO | — | — | — | — | — | — | — |
| POR | 1 | — | — | — | — | — | — | — |

Bit 7 **TYPEC_ACTIVE**: FSM active status
0: FSM is note active
1: FSM is active

Bit 6~0 Unimplemented, read as "0"

- **CC1_CMP Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | DET_3A | DET_1P5A | DET_DEF | DET_RD | DET_RA |
| R/W | — | — | — | RO | RO | RO | RO | RO |
| POR | — | — | — | 0 | 0 | 0 | 0 | 0 |

Bit 7~5 Unimplemented, read as "0"

Bit 4 **DET_3A**: CC1 3 A detection status
0: 3 A is not detected
1: 3 A is detected

Bit 3 **DET_1P5A**: CC1 1.5 A detection status
0: 1.5 A is not detected
1: 1.5 A is detected

Bit 2 **DET_DEF**: CC1 default current detection status
0: Default current is not detected
1: Default current is detected

Bit 1 **DET_RD**: CC1 $R_D$ detection status
0: $R_D$ is not detected
1: $R_D$ is detected

Bit 0 **DET_RA**: CC1 $R_A$ detection status
0: $R_A$ is not detected
1: $R_A$ is detected

- **CC2_CMP Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | DET_3A | DET_1P5A | DET_DEF | DET_RD | DET_RA |
| R/W | — | — | — | RO | RO | RO | RO | RO |
| POR | — | — | — | 0 | 0 | 0 | 0 | 0 |

Bit 7~5 Unimplemented, read as "0"

Bit 4 **DET_3A**: CC2 3 A detection status
0: 3 A is not detected
1: 3 A is detected

Bit 3 **DET_1P5A**: CC2 1.5 A detection status
0: 1.5 A is not detected
1: 1.5 A is detected

Bit 2 **DET_DEF**: CC2 default current detection status
0: Default current is not detected
1: Default current is detected

Bit 1 **DET_RD**: CC2 $R_D$ detection status
0: $R_D$ is not detected
1: $R_D$ is detected

Bit 0 **DET_RA**: CC2 $R_A$ detection status
0: $R_A$ is not detected
1: $R_A$ is detected

- **CC1_STATUS Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | SRC_RX16 | SRC_RX15 | SRC_RP1 | PWR3A_SNK1 | PWR1P5A_SNK1 | PWRDEF_SNK1 | SNK_RP1 |
| R/W | — | RO | RO | RO | RO | RO | RO | RO |
| POR | — | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7 Unimplemented, read as "0"

Bit 6~5 **SRC_RX16~SRC_RX15**: CC1 SRC detection status
00: Nothing is detected after $t_{CCDebounce}$ (SRC.open)
01: $R_D$ is detected after $t_{CCDebounce}$ (SRC.$R_D$)
10: $R_A$ is detected after $t_{CCDebounce}$ (SRC.$R_A$)
11: Reserved

Bit 4 **SRC_RP1**: CC1 SRC detection status
0: Nothing is detected (CC1 above maximum $V_{RD}$)
1: $R_D$ or $R_A$ pull-down is detected (CC1 below maximum $V_{RD}$)

Bit 3 **PWR3A_SNK1**: CC1 SNK 3 A detection status
0: Nothing is detected
1: SRC with 3 A current capability is detected

Bit 2 **PWR1P5A_SNK1**: CC1 SNK 1.5 A detection status
0: Nothing is detected
1: SRC with 1.5 A current capability is detected

Bit 1 **PWRDEF_SNK1**: CC1 SNK default current detection status
0: Nothing is detected
1: SRC with default current capability is detected

Bit 0 **SNK_RP1**: CC1 SNK $R_P$ detection status
0: Nothing is detected (CC1 below maximum $V_{RA}$) (SNK.open)
1: $R_P$ pull-up is detected (CC1 above minimum $V_{RD}$) (SNK.$R_P$)

### • CC2_STATUS Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | SRC_RX26 | SRC_RX25 | SRC_RP2 | PWR3A_SNK2 | PWR3A_SNK2 | PWRDEF_SNK2 | SNK_RP2 |
| R/W | — | RO | RO | RO | RO | RO | RO | RO |
| POR | — | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7 Unimplemented, read as "0"

Bit 6~5 **SRC_RX26~SRC_RX25**: CC2 SRC detection status
00: Nothing is detected after $t_{CCDebounce}$ (SRC.open)
01: $R_D$ is detected after $t_{CCDebounce}$ (SRC.$R_D$)
10: $R_A$ is detected after $t_{CCDebounce}$ (SRC.$R_A$)
11: Reserved

Bit 4 **SRC_RP2**: CC2 SRC detection status
0: Nothing is detected (CC2 above maximum $V_{RD}$)
1: $R_D$ or $R_A$ pull-down is detected (CC2 below maximum $V_{RD}$)

Bit 3 **PWR3A_SNK2**: CC2 SNK 3 A detection status
0: Nothing is detected
1: SRC with 3 A current capability is detected

Bit 2 **PWR1P5A_SNK2**: CC2 SNK 1.5 A detection status
0: Nothing is detected
1: SRC with 1.5 A current capability is detected

Bit 1 **PWRDEF_SNK2**: CC2 SNK default current detection status
0: Nothing is detected
1: SRC with default current capability is detected

Bit 0 **SNK_RP2**: CC2 SNK $R_P$ detection status
0: Nothing is detected (CC2 below maximum $V_{RA}$) (SNK.open)
1: $R_P$ pull-up is detected (CC2 above minimum $V_{RD}$) (SNK.$R_P$)

### • VBUS_MON Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VBUS_MON_EN | COMP | DAC5 | DAC4 | DAC3 | DAC2 | DAC1 | DAC0 |
| R/W | R/W | RO | RWH | RWH | RWH | RWH | RWH | RWH |
| POR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7 **VBUS_MON_EN**: VBUS monitor comparator control
0: Disable
1: Enable

Bit 6 **COMP**: VBUS higher than DAC set threshold
0: VBUS is not higher
1: VBUS is higher

Bit 5~0 **DAC5~DAC0**: Scaled VBUS threshold value
For 48 V EPR configuration, a 6-bit DAC is used to detect voltage drop. With recommended external divider, the following method is used to set the VBUS voltage when voltage drop detection is required:
DAC = 1.5 × (VBUS - 6)

- **AFE_TRIM2 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | — | — | TRIM_CCDRV1 | TRIM_CCDRV0 |
| R/W | — | — | — | — | — | — | R/W | R/W |
| POR | — | — | — | — | — | — | 1 | 0 |

Bit 7~2 Unimplemented, read as "0"

Bit 1~0 **TRIM_CCDRV1~TRIM_CCDRV0**: CC driver rise/fall trim
00: Slowest
01~10: Mid-point
11: Fastest

- **AFE_TRIM3 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | TRIM_SLICE2 | TRIM_SLICE1 | TRIM_SLICE0 | — | — | — | — |
| R/W | — | R/W | R/W | R/W | — | — | — | — |
| POR | — | 0 | 0 | 0 | — | — | — | — |

Bit 7 Unimplemented, read as "0"

Bit 6~4 **TRIM_SLICE2~TRIM_SLICE0**: Trim for the slicer when CDR_SELECT=1
The valid values are 3'h4 : 3'h0, with 3'h2 being the mid position of the trim. It is likely that after characterization these bits can be fixed, and always set to the same value on boot. Use a default value of 3'h7.

Bit 3~0 Unimplemented, read as "0"

- **POWER Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VCONN_CTRL_EXT | — | — | — | PWR3 | PWR2 | PWR1 | PWR0 |
| R/W | R/W | — | — | — | R/W | R/W | R/W | R/W |
| POR | 0 | — | — | — | 1 | 1 | 1 | 1 |

Bit 7 **VCONN_CTRL_EXT**: External VCONN generator enable control
0: Use internal VCONN generator
1: Use external VCONN generator

Bit 6~4 Unimplemented, read as "0"

Bit 3~0 **PWR3~PWR0**: Power enable control
0000: All Disable
0001: AFE Power Enable
0010: Wake Power Enable
0100: Bandgap and LDO Power Enable
1000: Oscillator Enable
1101: AFE Power, Bandgap and LDO Power, Oscillator Enable
1111: AFE Power, Wake Power, Bandgap and LDO Power, Oscillator Enable
Others: Reserved

- **IRQ1 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | I_VBUS_DROP | — | I_OVRTEMP | I_SHORT |
| R/W | — | — | — | — | RC | — | RC | RC |
| POR | — | — | — | — | 0 | — | 0 | 0 |

Bit 7~4 Unimplemented, read as "0"

Bit 3 **I_VBUS_DROP**: Indicates VBUS has dropped below threshold set by DAC[5:0]
0: VBUS is not dropped below threshold
1: VBUS is dropped below threshold

Bit 2 Unimplemented, read as "0"

Bit 1 **I_OVRTEMP**: OTP interrupt
0: OTP is not interrupt
1: OTP is interrupt

Bit 0 **I_SHORT**: Short interrupt
0: Short is not interrupt
1: Short is interrupt

- **IRQ2 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | I_CC_CHANGE | I_PD_RX | I_PD_HR_RX | I_PD_CR_RX | I_PD_TX_OK | I_PD_TX_FAIL | I_FAST_SWAP | I_TX_DISCARD |
| R/W | RC | RC | RC | RC | RC | RC | RC | RC |
| POR | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7 **I_CC_CHANGE**: Type-C status changed
0: Type-C status is not changed
1: Type-C status is changed

Bit 6 **I_PD_RX**: PD-message received
0: PD-message is not received
1: PD-message is received

Bit 5 **I_PD_HR_RX**: PD-HardReset received
0: PD-HardReset is not received
1: PD-HardReset is received

Bit 4 **I_PD_CR_RX**: PD-CableReset received
0: PD-CableReset is not received
1: PD-CableReset is received

Bit 3 **I_PD_TX_OK**: PD-Transmit success
0: PD-Transmit is not success
1: PD-Transmit is success

Bit 2 **I_PD_TX_FAIL**: PD-Transmit failure
0: PD-Transmit is not failure
1: PD-Transmit is failure

Bit 1 **I_FAST_SWAP**: Fast Role Swap occurred
0: Fast Role Swap is not occurred
1: Fast Role Swap is occurred

Bit 0 **I_TX_DISCARD**: PD transmit discarded due to incoming message
0: PD transmit was not discarded
1: PD transmit was discarded
Refer to the TX_RESULT[2:0] bits in the PD_STATUS register.

- **IRQ_MSK1 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | M_VBUS_DROP | — | M_OVRTEMP | M_SHORT |
| R/W | — | — | — | — | R/W | — | R/W | R/W |
| POR | — | — | — | — | 0 | — | 0 | 0 |

Bit 7~4 Unimplemented, read as "0"

Bit 3 **M_VBUS_DROP**: VBUS_DROP interrupt control
0: Disable
1: Enable

Bit 2 Unimplemented, read as "0"

Bit 1 **M_OVRTEMP**: OTP interrupt control
0: Disable
1: Enable

Bit 0 **M_SHORT**: Short interrupt control
0: Disable
1: Enable

- **IRQ_MSK2 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | M_CC_CHANGE | M_PD_RX | M_PD_HR_RX | M_PD_CR_RX | M_PD_TX_OK | M_PD_TX_FAIL | M_FAST_SWAP | — |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | — |
| POR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — |

Bit 7 **M_CC_CHANGE**: Type-C status changed interrupt control
0: Disable
1: Enable

Bit 6 **M_PD_RX**: PD-message received interrupt control
0: Disable
1: Enable

Bit 5 **M_PD_CR_RX**: PD-HardReset received interrupt control
0: Disable
1: Enable

Bit 4 **M_PD_TX_OK**: PD-CableReset received interrupt control
0: Disable
1: Enable

Bit 3 **M_VBUS_DROP**: PD-Transmit success interrupt control
0: Disable
1: Enable

Bit 2 **M_PD_TX_FAIL**: PD-Transmit failure interrupt control
0: Disable
1: Enable

Bit 1 **M_FAST_SWAP**: Fast Role Swap interrupt control
0: Disable
1: Enable

Bit 0 Unimplemented, read as "0"

• **PD_CFG1 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ID_IN-SERT | VBUS_ HIGH_VOLT | GUIDE_ TRY_SNK | — | RESET_ MSG_ID | SOP_TO_ RESET2 | SOP_TO_ RESET1 | SOP_TO_ RESET0 |
| R/W | R/W | R/W | R/W | — | WC | R/W | R/W | R/W |
| POR | 0 | 0 | 0 | — | 0 | 0 | 0 | 0 |

Bit 7 **ID_INSERT**: PD-FSM status control
0: PD-FSM will not change outgoing message – In this case software is responsible for providing the ID bits in the header
1: PD-FSM will keep track of Transmitted IDs for all SOP* and insert the correct value into the header at bit 11 ~ bit 9, no other bits are touched

Bit 6 **VBUS_HIGH_VOLT**: PD-FSM BIST Mode 2 control
0: PD-FSM will respond to request for BIST Mode 2 for compliance
1: PD-FSM will not respond to request for BIST Mode 2 for compliance
Note: The software must keep this bit updated according to VBUS voltage. Set to 1 if VBUS is above vSafe5V. This is required by the specification. Note that the original purpose of this was to prevent malicious use of BIST to force a port to high voltage which continues even after disconnect. However, the specification now limits the BIST length to 60 ms.

Bit 5 **GUIDE_TRY_SNK**: Use the TRY_SINK modified Type-C FSM
0: Not use
1: Use

Bit 4 Unimplemented, read as "0"

Bit 3 **RESET_MSG_ID**: Write 1 to clear the MessageID for SOP_TO_RESET type messages control
0: Reserved
1: Clear the MessageID

Bit 2~0 **SOP_TO_RESET2~SOP_TO_RESET0**: Which SOP to reset MessageID for Typically used to reset ID during a swap operation
001: SOP
010: SOP'
010: SOP''
100: Debug_SOP
101: Debug_SOP''
110~111: Reserved

• **PD_CFG2 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FAST_ SWAP_SNK | FAST_ SWAP_SRC | CDR_ SELECT | SOP_ RCV4 | SOP_ RCV3 | SOP_ RCV2 | SOP_ RCV1 | SOP_ RCV0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7 **FAST_SWAP_SNK**: Fast Role Swap sink function enable control
0: Disable
1: Enable

Bit 6 **FAST_SWAP_SRC**: Fast Role Swap source function enable control
0: Disable
1: Enable

Bit 5 **CDR_SELECT**: Select between versions of the CC CDR
0: 3-level slicer
1: AC coupled
Note that this bit also controls rxMode signals to the AFE.

Bit 4~0 **SOP_RCV4~SOP_RCV0**: Select which SOP to receive
00000: No SOP is received
xxxx1: SOP is received
xxx1x: SOP' is received
xx1xx: SOP'' is received
x1xxx: SOP_debug' is received
1xxxx: SOP_debug'' is received
Note that multiple SOP types can be received at the same time.

- **PD_CFG3 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | P_DATA_ROLE_DP | P_PWR_ROLE_DP | P_DATA_ROLE_PR | P_PWR_ROLE_PR | P_DATA_ROLE_SOP | P_PWR_ROLE_SOP |
| R/W | — | — | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | — | — | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7~6 Unimplemented, read as "0"

Bit 5 **P_DATA_ROLE_DP**: SOP''. Current Port Data Role. Transmit header bit 5
0: Bit is cleared to 0
1: Bit is set to 1
Cable communication to the remote end of the cable (future use).

Bit 4 **P_PWR_ROLE_DP**: SOP''. Current Port Power Role. Transmit header bit 8
Cable communication to the remote end of the cable (future use).
0: Bit is cleared to 0
1: Bit is set to 1

Bit 3 **P_DATA_ROLE_PR**: SOP'. Current Port Data Role. Transmit header bit 5
0: Bit is cleared to 0
1: Bit is set to 1
Cable communication to the near end of the cable.

Bit 2 **P_PWR_ROLE_PR**: SOP'. Current Port Power Role. Transmit header bit 8
0: Bit is cleared to 0
1: Bit is set to 1
Cable communication to the near end of the cable.

Bit 1 **P_DATA_ROLE_SOP**: SOP. Current Port Data Role. Transmit header bit 5
0: Bit is cleared to 0
1: Bit is set to 1

Bit 0 **P_PWR_ROLE_SOP**: SOP. Current Port Power Role. Transmit header bit 8
0: Bit is cleared to 0
1: Bit is set to 1

- **SHORT_PROTECT Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SHORT_RESET | SHORT_TIME6 | SHORT_TIME5 | SHORT_TIME4 | SHORT_TIME3 | SHORT_TIME2 | SHORT_TIME1 | SHORT_TIME0 |
| R/W | WC | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |

Bit 7~6 **SHORT_RESET**: Short reset control
0: Reserved
1: Reset
Note: 1. Write 1 to reset VCONN power after maximum short time has been reached.
2. To prevent over-temperature, protect should not be reset more than once per second.

Bit 6~0 **SHORT_TIME6~SHORT_TIME0**: Maximum short time before VCONN is shut off – One LSB is 0.488 ms

- **PD_STATUS Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FAST_SWAP | — | RX_RESULT5 | RX_RESULT4 | RX_RESULT3 | TX_RESULT2 | TX_RESULT1 | TX_RESULT0 |
| R/W | RO | — | RO | RO | RO | RO | RO | RO |
| POR | 0 | — | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7 **FAST_SWAP**: Indicates Fast Role Swap has happened
0: Fast Role Swap has not happened
1: Fast Role Swap has happened

Bit 6 Unimplemented, read as "0"

Bit 5~3 **RX_RESULT5~RX_RESULT3**: Received status
000: No operation
001: Message Received - Read buffer
010: Hard reset from remote
011: Cable reset from remote
100~111: Reserved

Bit 2~0 **TX_RESULT2~TX_RESULT0**: Transmitter status
000: No operation
001: Message sent with success
010: Transmission error
011: Transmitter busy
100: Transmit discarded due to incoming message
101~111: Reserved

- **RX_STATUS Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RX_DATA | RX_OVERRUN | — | — | — | — | — | RX_CLEAR |
| R/W | RO | RO | — | — | — | — | — | WC |
| POR | 0 | 0 | — | — | — | — | — | 0 |

Bit 7 **RX_DATA**: Indicates buffer data is available
0: Buffer data is not available
1: Buffer data is available

Bit 6 **RX_OVERRUN**: New data has arrived without the previous data having been read
0: Read
1: Not read
Cleared by writing a "1" to RX_CLEAR.

Bit 5~1 Unimplemented, read as "0"

Bit 0 **RX_CLEAR**: Write a "1" to this bit to indicate data has been read
0: Reserved
1: Indicates data has been read
If there is another packet in buffer, RX_DATA will remain 1.

- **RX_INFO Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RX_ BYTES7 | RX_ BYTES6 | RX_ BYTES5 | RX_ BYTES4 | RX_ BYTES3 | RX_ SOP2 | RX_ SOP1 | RX_ SOP0 |
| R/W | RO | RO | RO | RO | RO | RO | RO | RO |
| POR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7~3 **RX_BYTES7~RX_BYTES3**: Actual number of bytes received

Bit 2~0 **RX_SOP2~RX_SOP0**: SOP type of the received message
000: No Message
001: SOP
010: SOP'
011: SOP''
100: Debug SOP'
101: Debug SOP''
110~111: Reserved

- **TX_COMMAND Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TX_CMD7 | TX_CMD6 | TX_CMD5 | — | — | TX_WAIT_RP | TX_START | TXBUF_READY |
| R/W | R/W | R/W | R/W | — | — | R/W | WC | RO |
| POR | 0 | 0 | 0 | — | — | 0 | 0 | 1 |

Bit 7~5 **TX_CMD7~TX_CMD5**: Transmit Commands control
000: NOP
001: Send the message in buffer
010: Send CableReset
011: Send HardReset
100: Start BIST Mode 2 for 45 ms
101~111: Unused

Bit 4~3 Unimplemented, read as "0"

Bit 2 **TX_WAIT_RP**: TX Wait $R_P$ control
0: TX does not wait
1: TX will hold until $R_P$ = 3 A

Bit 1 **TX_START**: A write to this bit starts transmission of what is in the TX buffer
0: Not transmission
1: Starts transmission

Bit 0 **TXBUF_READY**: Transmission status
0: Transmission ongoing
1: Transmission complete
The software should check whether this bit is 1 before filling the transmit buffer.

- **TX_INFO Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | TX_RETRIES5 | TX_RETRIES4 | TX_RETRIES3 | TX_SOP2 | TX_SOP1 | TX_SOP0 |
| R/W | — | — | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | — | — | 0 | 1 | 1 | 0 | 0 | 0 |

Bit 7~6 Unimplemented, read as "0"

Bit 5~3 **TX_RETRIES5~TX_RETRIES3**: Number of retries to be attempted for this message

Bit 2~0 **TX_SOP2~TX_SOP0**: SOP type of the transmitted message
000: Not Valid
001: SOP
010: SOP'
011: SOP''
100: Debug SOP'
101: Debug SOP''
110~111: Reserved

### • RX_PACKET_DATAm Register (m=61~90)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7~0 **D7~D0**: Receive packet data

The SOP and EOP symbols are not included in the receive data. The first byte of the data is the 8 LSB's of the packet header, and is ordered consistently with the power delivery specification. Also:

- The GoodCRC packets are consumed by the logic and do not appear in the receive buffer.
- The packet's CRC is not included in the byte count. However, when space in the buffer is available, the CRC field appears after the data in the buffer.

### • TX_PACKET_DATAn Register (n=91~120)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7~0 **D7~D0**: Transmit packet data

The SOP and EOP symbols are not included in the transmit data. The first byte of the data is the 8 LSB's of the packet header, and is ordered consistently with the power delivery specification.

### • C_OVP Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | ENP2 | ENP1 | STP2 | STP1 |
| R/W | — | — | — | — | R/W | R/W | R/W | R/W |
| POR | — | — | — | — | 0 | 0 | 0 | 0 |

Bit 7~4 Unimplemented, read as "0"

Bit 3~2 **ENP2~ENP1**: Associated Protect blocks enable control
00: Disable
01: CC1 Protect blocks enable
10: CC2 Protect blocks enable
11: CC1 and CC2 Protect blocks enable

The Protect blocks must be enabled before they are started.

Bit 1~0 **STP2~STP1**: Protect blocks for the associated CC1/CC2 Start control
00: Disable
01: CC1 OVP Start enable
10: CC2 OVP Start enable
11: CC1 and CC2 OVP Start enable

These can be started at boot time, or to save power only started when needed. The protect blocks must be first enabled with CC1/CC2 pin.

## PD PHY Reset

When the system is powered on for the first time, the SYSRESETN line needs to be sent a signal from low to high with a width of 30 μs to complete the reset action. After this, send the I²C command to set the relevant registers.

## SVBUS External Divider Resistor Configuration

**Table 6. External Divider for 48 V EPR Scaled VBUS (SVBUS Input)**

| Component | Connection | Note |
|---|---|---|
| 220 kΩ + 680 Ω 1 % resistors | VBUS to SVBUS pin | — |
| 12 kΩ + 1 kΩ 1 % resistors | SVBUS pin to ground | Good analog ground connection |
| 10nF capacitor | SVBUS pin to ground | Good analog ground connection |

## PD PHY I²C Function

The I²C serial interface is a two line interface, a serial data line, SDA_PD, and serial clock line, SCL_PD. As many devices may be connected together on the same bus, their outputs are both open drain types. For this reason it is necessary that external pull-high resistors are connected to these outputs. Note that no chip select line exists, as each device on the I²C bus is identified by a unique address which will be transmitted and received on the I²C bus. When two devices communicate with each other on the bidirectional I²C bus, one is known as the master device and one as the slave device. Both master and slave can transmit and receive data, however, it is the master device that has overall control of the bus. For the device, which only operates in slave mode, there are two methods of transferring data on the I²C bus, the slave transmit mode and the slave receive mode.

Communication on the I²C bus requires four separate steps, a START signal, a slave device address transmission, a data transmission and finally a STOP signal. When a START signal is placed on the I²C bus, all devices on the bus will receive this signal and be notified of the imminent arrival of data on the bus. The first seven bits of the data will be the slave address, the 8th bit is the read/write bit whose value will be placed in the SRW bit. This bit will be checked by the slave device to determine whether to go into transmit or receive mode. The transmitted data is 8-bit wide and is transmitted after the slave device has acknowledged receipt of its slave address. The order of serial bit transmission is the MSB first and the LSB last. After receipt of 8 bits of data, the receiver must transmit an acknowledge signal, level “0”, before it can receive the next data byte. If the slave transmitter does not receive an acknowledge bit signal from the master receiver, then the slave transmitter will release the SDA_PD line to allow the master to send a STOP signal to release the I²C Bus.

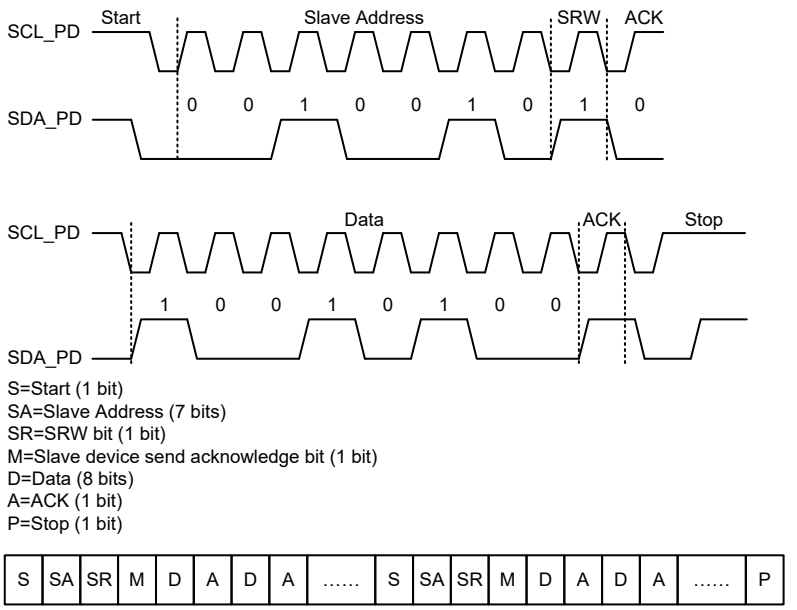



**Figure 4. PD PHY I²C Communication Timing Diagram**

## Device Addressing

The slave address byte is the first byte received following the START condition from the master device. The first seven bits of the first byte make up the slave address. The eighth bit defines whether a read or write operation is to be performed. When the R/$\overline{W}$ bit is "1", then a read operation is selected. A "0" selects a write operation. The device address bits are "0010010". When an address byte is sent, the device compares the first seven bits after the START condition. If they match, the device outputs an acknowledge on the SDA_PD line.

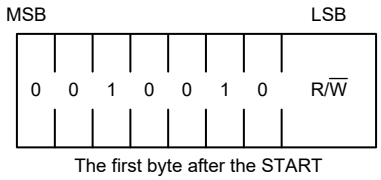



**Figure 5. Device Addressing**

## Write/Read Timing

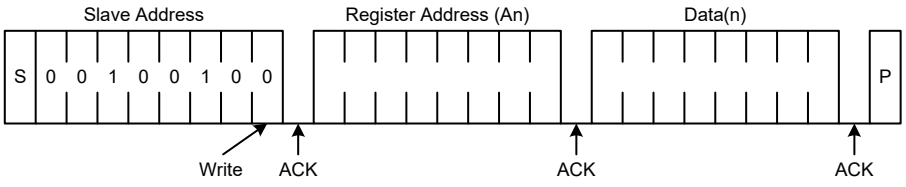



**Figure 6. Byte Write Timing**

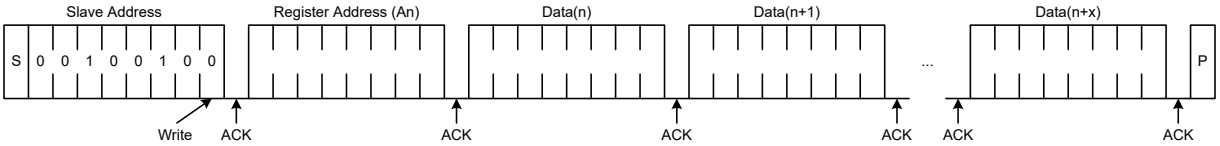



**Figure 7. Page Write Timing**

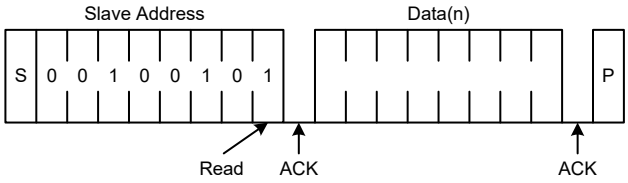



**Figure 8. Read Timing**

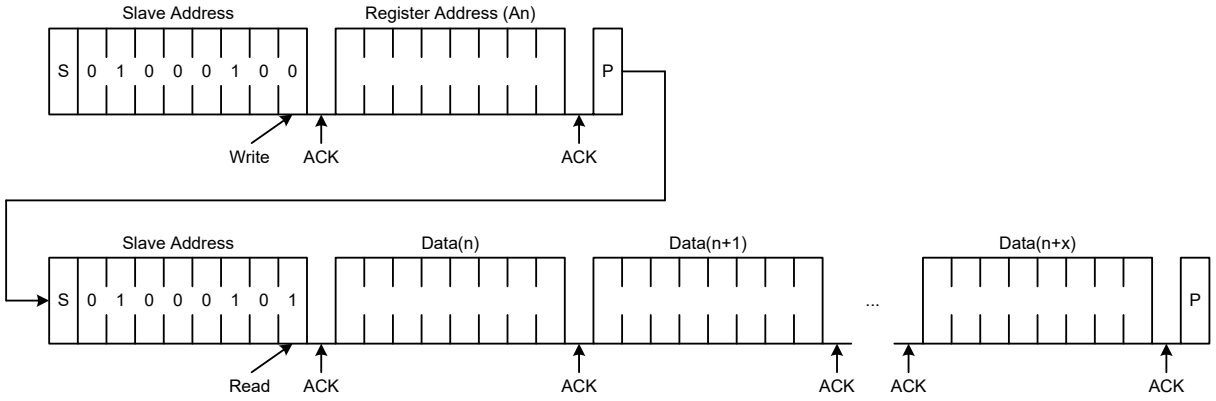



**Figure 9. Random Read Timing**

# 5 Pin Assignment

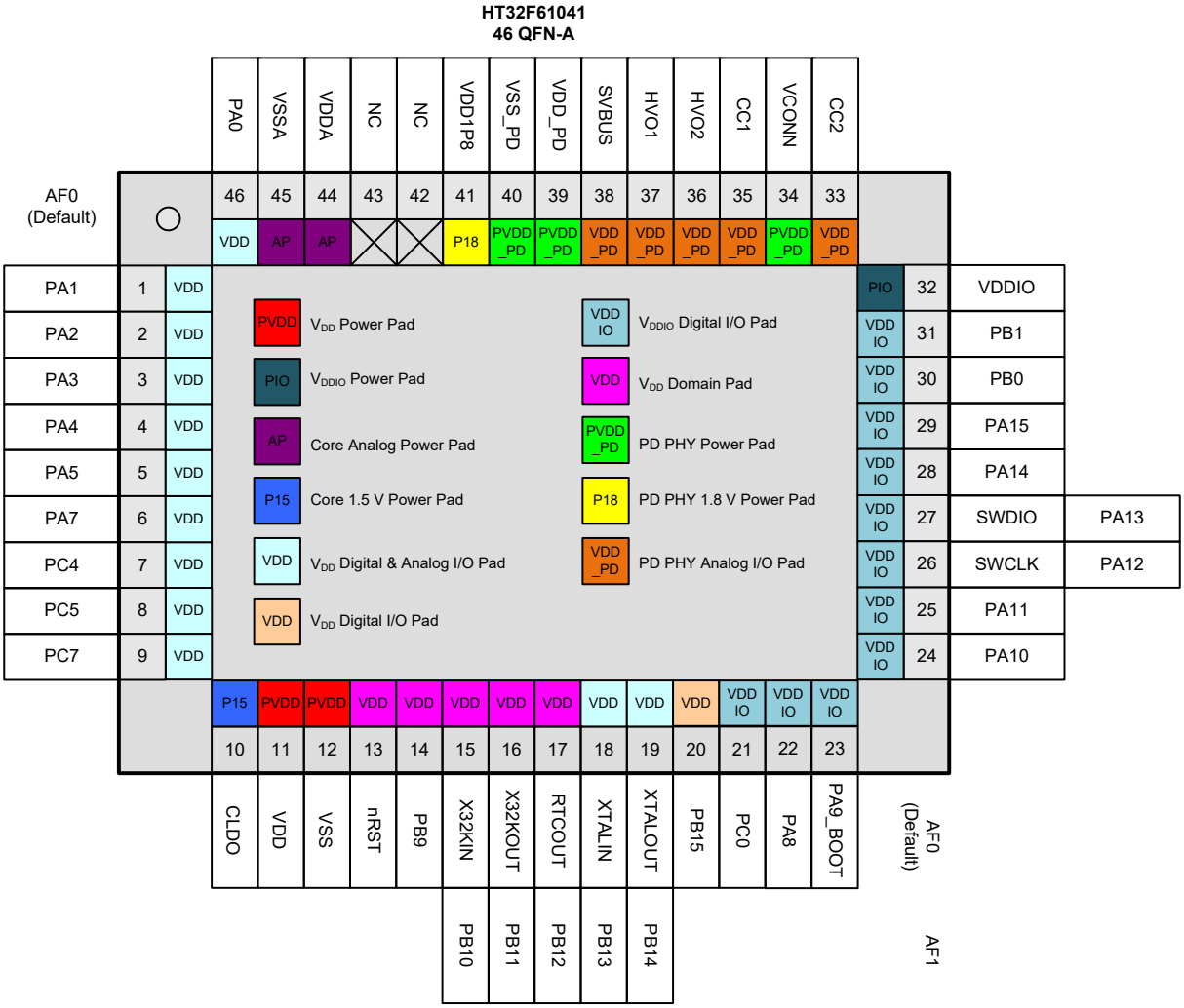



**Figure 10. 46-pin QFN Pin Assignment**

## Table 7. Pin Assignment

| Package | Alternate Function Mapping | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
| 46 QFN | System Default | GPIO | ADC | N/A | MCTM /GPTM | SPI | USART /UART | I²C | N/A | N/A | N/A | N/A | N/A | PWM | N/A | System Other |
| 46 | PA0 | | ADC_IN2 | | GT_CH0 | SPI1_SCK | USR_RTS | I2C1_SCL | | | | | | | | |
| 1 | PA1 | | ADC_IN3 | | GT_CH1 | SPI1_MOSI | USR_CTS | I2C1_SDA | | | | | | | | |
| 2 | PA2 | | ADC_IN4 | | GT_CH2 | SPI1_MISO | USR_TX | | | | | | | | | |
| 3 | PA3 | | ADC_IN5 | | GT_CH3 | SPI1_SEL | USR_RX | | | | | | | | | |
| 4 | PA4 | | ADC_IN6 | | GT_CH0 | SPI0_SCK | UR1_TX | I2C0_SCL | | | | | | | | |
| 5 | PA5 | | ADC_IN7 | | GT_CH1 | SPI0_MOSI | UR1_RX | I2C0_SDA | | | | | | | | |
| 6 | PA7 | | ADC_IN9 | | GT_CH3 | SPI0_SEL | | | | | | | | | | |
| 7 | PC4 | | ADC_IN10 | | | | USR_TX | | | | | | | PWM1_CH0 | | |
| 8 | PC5 | | ADC_IN11 | | | | USR_RX | | | | | | | PWM1_CH1 | | |
| 9 | PC7 | | | | MT_CH2N | | UR0_RX | I2C0_SDA | | | | | | | | |
| 10 | CLDO | | | | | | | | | | | | | | | |
| 11 | VDD | | | | | | | | | | | | | | | |
| 12 | VSS | | | | | | | | | | | | | | | |
| 13 | nRST | | | | | | | | | | | | | | | |
| 14 | PB9 | | | | MT_CH3 | | | | | | | | | PWM1_CH2 | | WAKEUP1 |
| 15 | X32KIN | PB10 | | | GT_CH0 | SPI1_SEL | USR_TX | | | | | | | PWM1_CH3 | | |
| 16 | X32KOUT | PB11 | | | GT_CH1 | SPI1_SCK | USR_RX | | | | | | | PWM0_CH3 | | |
| 17 | RTCOUT | PB12 | | | | SPI0_MISO | UR0_RX | | | | | | | PWM0_CH0 | | WAKEUP0 |
| 18 | XTALIN | PB13 | | | | | UR0_TX | I2C0_SCL | | | | | | | | |
| 19 | XTALOUT | PB14 | | | | | UR0_RX | I2C0_SDA | | | | | | | | |
| 20 | PB15 | | | | MT_CH0 | SPI0_SEL | | I2C1_SCL | | | | | | PWM0_CH1 | | |
| 21 | PC0 | | | | MT_CH0N | SPI0_SCK | | I2C1_SDA | | | | | | PWM0_CH2 | | |
| 22 | PA8 | | | | | | USR_TX | | | | | | | PWM1_CH3 | | |
| 23 | PA9_BOOT | | | | | SPI0_MOSI | | | | | | | | PWM1_CH0 | | CKOUT |
| 24 | PA10 | | | | MT_CH1 | SPI0_MOSI | USR_RX | | | | | | | PWM0_CH1 | | |
| 25 | PA11 | | | | MT_CH1N | SPI0_MISO | | | | | | | | PWM0_CH2 | | |
| 26 | SWCLK | PA12 | | | | | | | | | | | | | | |
| 27 | SWDIO | PA13 | | | | | | | | | | | | | | |
| 28 | PA14 | | | | MT_CH0 | SPI1_SEL | UR1_TX | I2C1_SCL | | | | | | PWM0_CH0 | | |
| 29 | PA15 | | | | MT_CH0N | SPI1_SCK | UR1_RX | I2C1_SDA | | | | | | PWM1_CH2 | | |
| 30 | PB0 | | | | MT_CH1 | SPI1_MOSI | USR_TX | I2C0_SCL | | | | | | PWM0_CH1 | | |
| 31 | PB1 | | | | MT_CH1N | SPI1_MISO | USR_RX | I2C0_SDA | | | | | | PWM1_CH1 | | |

| Package | Alternate Function Mapping | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
| 46 QFN | System Default | GPIO | ADC | N/A | MCTM /GPTM | SPI | USART /UART | I²C | N/A | N/A | N/A | N/A | N/A | PWM | N/A | System Other |
| 32 | VDDIO | | | | | | | | | | | | | | | |
| 33 | CC2 | | | | | | | | | | | | | | | |
| 34 | VCONN | | | | | | | | | | | | | | | |
| 35 | CC1 | | | | | | | | | | | | | | | |
| 36 | HVO2 | | | | | | | | | | | | | | | |
| 37 | HVO1 | | | | | | | | | | | | | | | |
| 38 | SVBUS | | | | | | | | | | | | | | | |
| 39 | VDD_PD | | | | | | | | | | | | | | | |
| 40 | VSS_PD | | | | | | | | | | | | | | | |
| 41 | VDD1P8 | | | | | | | | | | | | | | | |
| 42, 43 | NC | | | | | | | | | | | | | | | |
| 44 | VDDA | | | | | | | | | | | | | | | |
| 45 | VSSA | | | | | | | | | | | | | | | |



## Table 8. Pin Description

| Pin Number | Pin Name | Type(1) | I/O Structure(2) | Output Driving | Description |
|---|---|---|---|---|---|
| 46 QFN | | | | | Default Function (AF0) |
| 46 | PA0 | AI/O | 5V | 4/8/12/16 mA | PA0 |
| 1 | PA1 | AI/O | 5V | 4/8/12/16 mA | PA1 |
| 2 | PA2 | AI/O | 5V | 4/8/12/16 mA | PA2 |
| 3 | PA3 | AI/O | 5V | 4/8/12/16 mA | PA3 |
| 4 | PA4 | AI/O | 5V | 4/8/12/16 mA | PA4, this pin provides a UART_TX function in the Boot loader mode. |
| 5 | PA5 | AI/O | 5V | 4/8/12/16 mA | PA5, this pin provides a UART_RX function in the Boot loader mode |
| 6 | PA7 | AI/O | 5V | 4/8/12/16 mA | PA7 |
| 7 | PC4 | AI/O | 5V | 4/8/12/16 mA | PC4 |
| 8 | PC5 | AI/O | 5V | 4/8/12/16 mA | PC5 |
| 9 | PC7 | I/O | 5V | 4/8/12/16 mA | PC7 |
| 10 | CLDO | P | — | — | Core power LDO $V_{CORE}$ output<br>It must be connected a 2.2 μF capacitor as close as possible between this pin and VSS. |
| 11 | VDD | P | — | — | Voltage for digital I/O |
| 12 | VSS | P | — | — | Ground reference for digital I/O |
| 13 | nRST(3) | I | 5V_PU | — | External reset pin |
| 14 | PB9(3) | I/O ($V_{DD}$) | 5V | 4/8/12/16 mA | PB9 |
| 15 | PB10(3) | AI/O ($V_{DD}$) | 5V | 4/8/12/16 mA | X32KIN |
| 16 | PB11(3) | AI/O ($V_{DD}$) | 5V | 4/8/12/16 mA | X32KOUT |
| 17 | PB12(3) | I/O ($V_{DD}$) | 5V | 4/8/12/16 mA | RTCOUT |

| Pin Number | Pin Name | Type(1) | I/O Structure(2) | Output Driving | Description |
|---|---|---|---|---|---|
| 46 QFN | | | | | Default Function (AF0) |
| 18 | PB13 | AI/O | 5V | 4/8/12/16 mA | XTALIN |
| 19 | PB14 | AI/O | 5V | 4/8/12/16 mA | XTALOUT |
| 20 | PB15 | I/O | 5V | 4/8/12/16 mA | PB15 |
| 21 | PC0 | I/O ($V_{DDIO}$) | 5V | 4/8/12/16 mA | PC0 |
| 22 | PA8 | I/O ($V_{DDIO}$) | 5V | 4/8/12/16 mA | PA8 |
| 23 | PA9 | I/O ($V_{DDIO}$) | 5V_PU | 4/8/12/16 mA | PA9_BOOT |
| 24 | PA10 | I/O ($V_{DDIO}$) | 5V | 4/8/12/16 mA | PA10 |
| 25 | PA11 | I/O ($V_{DDIO}$) | 5V | 4/8/12/16 mA | PA11 |
| 26 | PA12 | I/O ($V_{DDIO}$) | 5V_PU | 4/8/12/16 mA | SWCLK |
| 27 | PA13 | I/O ($V_{DDIO}$) | 5V_PU | 4/8/12/16 mA | SWDIO |
| 28 | PA14 | I/O ($V_{DDIO}$) | 5V | 4/8/12/16 mA | PA14 |
| 29 | PA15 | I/O ($V_{DDIO}$) | 5V | 4/8/12/16 mA | PA15 |
| 30 | PB0 | I/O ($V_{DDIO}$) | 5V | 4/8/12/16 mA | PB0 |
| 31 | PB1 | I/O ($V_{DDIO}$) | 5V | 4/8/12/16 mA | PB1 |
| 32 | VDDIO | P | — | — | Voltage for digital I/O |
| 33 | CC2 | AI/O | — | — | USB Type-C PD configuration channel 2 |
| 34 | VCONN | P | — | — | VCONN power 3 V ~ 5.5 V input |
| 35 | CC1 | AI/O | — | — | USB Type-C PD configuration channel 1 |
| 36 | HVO2 | OD | — | — | Open drain output 2 |
| 37 | HVO1 | OD | — | — | Open drain output 1 |
| 38 | SVBUS | AI | — | — | USB VBUS connector |
| 39 | VDD_PD | PWR | — | — | PD PHY Positive power supply |
| 40 | VSS_PD | PWR | — | — | PD PHY Negative power supply, ground |
| 41 | VDD1P8 | PWR | — | — | PD PHY Regulator output pin and 1.8 V Digital positive power supply |
| 42, 43 | NC | — | — | — | No connected |
| 44 | VDDA | P | — | — | Analog voltage for ADC |
| 45 | VSSA | P | — | — | Ground reference for the ADC |

Note: 1. I = input, O = output, A = Analog port, OD = Open-Drain output, P = power supply, $V_{DD}$ = $V_{DD}$ Power.
2. 5V = 5 V operation I/O type, PU = Pull-up.
3. These pins are located at the $V_{DD}$ power domain.
4. In the Boot loader mode, only the UART interface can be used for communication.

## Internal Connection Signal Lines

The MCU generated signals such as the I2C1_SCL have been internally connected to the power delivery for control purpose. The connections are listed in the following table and the related control registers should be configured correctly using application program.

**Table 9. Internal Connection Signal Lines**

| MCU Signal Name | Connected PD PHY Signal Name | Description |
|---|---|---|
| PB7 / I2C1_SCL ($I^2C$) | SCL_PD | PD PHY $I^2C$ Clock line. The MCU AFIO setting should be AF7 to select the $I^2C$ pin function. |
| PB8 / I2C1_SDA ($I^2C$) | SDA_PD | PD PHY $I^2C$ data line. The MCU AFIO setting should be AF7 to select the $I^2C$ pin function. |
| PB2 | HVI1 | Open drain control logic 1. The MCU AFIO setting should be AF0 to select the General Purpose Input/Output pin function. |
| PB3 | HVI2 | Open drain control logic 2. The MCU AFIO setting should be AF0 to select the General Purpose Input/Output pin function. |
| PB4 | SYSRESETN | PD PHY reset input signal. The MCU AFIO setting should be AF0 to select the General Purpose Input/Output pin function. |
| PB5 | BUS_INT | BUS interrupt output signal. The MCU AFIO setting should be AF0 to select the General Purpose Input/Output pin function. |

# 6 Application Circuits

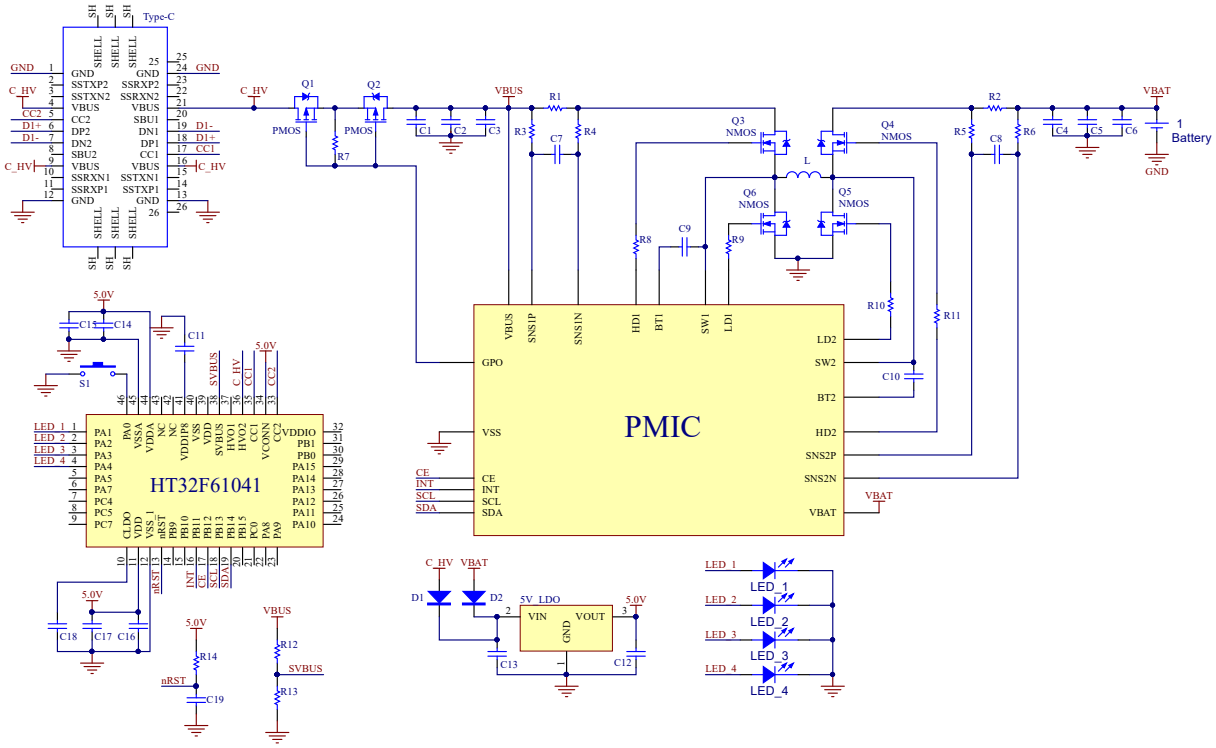



**Figure 11. Application Circuit**

# 7 Electrical Characteristics

## Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**Table 10. Absolute Maximum Ratings**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | External Main Supply Voltage | $V_{SS}$ - 0.3 | $V_{SS}$ + 5.5 | V |
| $V_{DDIO}$ | External I/O Supply Voltage | $V_{SS}$ - 0.3 | $V_{SS}$ + 5.5 | V |
| $V_{DDA}$ | External Analog Supply Voltage | $V_{SSA}$ - 0.3 | $V_{SSA}$ + 5.5 | V |
| $V_{IN}$ | Input Voltage on I/O | $V_{SS}$ - 0.3 | $V_{DD}$ + 0.3 | V |
| $T_A$ | Ambient Operating Temperature Range | -40 | 85 | °C |
| $T_{STG}$ | Storage Temperature Range | -60 | 150 | °C |
| $T_J$ | Maximum Junction Temperature | — | 125 | °C |
| $P_D$ | Total Power Dissipation | — | 500 | mW |

## Recommended DC Operating Conditions

**Table 11. Recommended DC Operating Conditions**

$T_A$ = 25 °C, unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operating Voltage | — | 2.5 | 5.0 | 5.5 | V |
| $V_{DDIO}$ | I/O Operating Voltage | — | 1.8 | 5.0 | 5.5 | V |
| $V_{DDA}$ | Analog Operating Voltage | — | 2.5 | 5.0 | 5.5 | V |

## On-Chip LDO Voltage Regulator Characteristics

**Table 12. LDO Characteristics**

$T_A$ = 25 °C, unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{LDO}$ | Internal Regulator Output Voltage | $V_{DD}$ ≥ 2.5 V Regulator input @ $I_{LDO}$ = 35 mA and voltage variant = ±5 %, After trimming | 1.425 | 1.5 | 1.57 | V |
| $I_{LDO}$ | Output Current | $V_{DD}$ = 2.5 V Regulator input @ $V_{LDO}$ = 1.5 V | — | 30 | 35 | mA |
| $C_{LDO}$ | External Filter Capacitor Value for Internal Core Power Supply | The capacitor value is dependent on the core power current consumption | 1 | 2.2 | — | μF |

## Power Consumption

### Table 13. Power Consumption Characteristics

$T_A$ = 25 °C, unless otherwise specified.

| Symbol | Parameter | Conditions | Typ. | Max. @ $T_A$ | | Unit |
|---|---|---|---|---|---|---|
| | | | | 25 °C | 85 °C | |
| $I_{DD}$ | Supply Current (Run Mode) | $V_{DD}$ = 5.0 V, HSI = 20 MHz, $f_{CPU}$ = 20 MHz, $f_{BUS}$ = 20 MHz, all peripherals enabled | 6.5 | 7.2 | — | mA |
| | | $V_{DD}$ = 5.0 V, HSI = 20 MHz, $f_{CPU}$ = 20 MHz, $f_{BUS}$ = 20 MHz, all peripherals disabled | 4 | 4.5 | — | |
| | | $V_{DD}$ = 5.0 V, HSI = 20 MHz, $f_{CPU}$ = 10 MHz, $f_{BUS}$ = 10 MHz, all peripherals enabled | 3.5 | 3.9 | — | |
| | | $V_{DD}$ = 5.0 V, HSI = 20 MHz, $f_{CPU}$ = 10 MHz, $f_{BUS}$ = 10 MHz, all peripherals disabled | 2.25 | 2.5 | — | |
| | | $V_{DD}$ = 5.0 V, HSI off, LSI on, $f_{CPU}$ = 32 kHz, $f_{BUS}$ = 32 kHz, all peripherals enabled | 32 | 41 | — | µA |
| | | $V_{DD}$ = 5.0 V, HSI off, LSI on, $f_{CPU}$ = 32 kHz, $f_{BUS}$ = 32 kHz, all peripherals disabled | 28 | 37 | — | |
| | Supply Current (Sleep Mode) | $V_{DD}$ = 5.0 V, HSI = 20 MHz, $f_{CPU}$ = 0 MHz, $f_{BUS}$ = 20 MHz, all peripherals enabled | 3.5 | 3.9 | — | mA |
| | | $V_{DD}$ = 5.0 V, HSI = 20 MHz, $f_{CPU}$ = 0 MHz, $f_{BUS}$ = 20 MHz, all peripherals disabled | 0.8 | 0.92 | — | |
| | | $V_{DD}$ = 5.0 V, HSI = 20 MHz, $f_{CPU}$ = 0 MHz, $f_{BUS}$ = 10 MHz, all peripherals enabled | 2 | 2.25 | — | |
| | | $V_{DD}$ = 5.0 V, HSI = 20 MHz, $f_{CPU}$ = 0 MHz, $f_{BUS}$ = 10 MHz, all peripherals disabled | 0.65 | 0.75 | — | |
| | Supply Current (Deep-Sleep1 Mode) | $V_{DD}$ = 5.0 V, All clock off (HSE/HSI/LSE), LDO in low power mode, LSI on, RTC on | 23 | 29 | — | µA |
| | Supply Current (Deep-Sleep2 Mode) | $V_{DD}$ = 5.0 V, All clock off (HSE/HSI/LSE), LDO off, DMOS on, LSI on, RTC on | 6.5 | 10 | — | |

Note: 1. HSE means high speed external oscillator. HSI means 20 MHz high speed internal oscillator.
2. LSE means 32.768 kHz low speed external oscillator. LSI means 32 kHz low speed internal oscillator.
3. RTC means Real-Time clock.
4. Code = while (1) {208 NOP} executed in Flash.
5. $f_{BUS}$ means $f_{HCLK}$ and $f_{PCLK}$.

# Reset and Supply Monitor Characteristics

## Table 14. $V_{DD}$ Power Reset Characteristics

$T_A$ = 25 °C, unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{POR}$ | Power On Reset Threshold (Rising Voltage on $V_{DD}$) | $T_A$ = -40 °C ~ 85 °C | 2.22 | 2.35 | 2.48 | V |
| $V_{PDR}$ | Power Down Reset Threshold (Falling Voltage on $V_{DD}$) | | 2.12 | 2.2 | 2.33 | V |
| $V_{PORHYST}$ | POR Hysteresis | — | — | 150 | — | mV |
| $t_{POR}$ | Reset Delay Time | $V_{DD}$ = 5.0 V | — | 0.1 | 0.2 | ms |

Note: 1. Data based on characterization results only, not tested in production.
2. If the LDO is turned on, the $V_{DD}$ POR has to be in the de-assertion condition. When the $V_{DD}$ POR is in the assertion state then the LDO will be turned off.

## Table 15. LVD/BOD Characteristics

$T_A$ = 25 °C, unless otherwise specified.

| Symbol | Parameter | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{BOD}$ | Voltage of Brown Out Detection | After factory-trimmed, $V_{DD}$ Falling edge | | 2.37 | 2.45 | 2.53 | V |
| $V_{LVD}$ | Voltage of Low Voltage Detection | $V_{DD}$ Falling edge | LVDS = 000 | 2.57 | 2.65 | 2.73 | V |
| | | | LVDS = 001 | 2.77 | 2.85 | 2.93 | V |
| | | | LVDS = 010 | 2.97 | 3.05 | 3.13 | V |
| | | | LVDS = 011 | 3.17 | 3.25 | 3.33 | V |
| | | | LVDS = 100 | 3.37 | 3.45 | 3,53 | V |
| | | | LVDS = 101 | 4.15 | 4.25 | 4.35 | V |
| | | | LVDS = 110 | 4.35 | 4.45 | 4.55 | V |
| | | | LVDS = 111 | 4.55 | 4.65 | 4.75 | V |
| $V_{LVDHTST}$ | LVD Hysteresis | $V_{DD}$ = 5.0 V | — | — | 100 | — | mV |
| $t_{suLVD}$ | LVD Setup Time | $V_{DD}$ = 5.0 V | — | — | — | 5 | μs |
| $t_{atLVD}$ | LVD Active Delay Time | $V_{DD}$ = 5.0 V | — | — | — | — | ms |
| $I_{DDLVD}$ | Operation Current (2) | $V_{DD}$ = 5.0 V | — | — | 10 | 20 | μA |

Note: 1. Data based on characterization results only, not tested in production.
2. Bandgap current is not included.
3. LVDS field is in the PWRCU LVDCSR register.

## External Clock Characteristics

### Table 16. High Speed External Clock (HSE) Characteristics

$T_A$ = 25 °C, unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operation Range | $T_A$ = -40 °C ~ 85 °C | 2.5 | — | 5.5 | V |
| $f_{HSE}$ | High Speed External Oscillator Frequency (HSE) | $V_{DD}$ = 2.5 V ~ 5.0 V | 4 | — | 20 | MHz |
| $C_L$ | Load Capacitance | $V_{DD}$ = 5.0 V, $R_{ESR}$ = 100 Ω @ 20 MHz | — | — | 12 | pF |
| $R_{FHSE}$ | Internal Feedback Resistor between XTALIN and XTALOUT Pins | $V_{DD}$ = 5.0 V | — | 0.5 | — | MΩ |
| $R_{ESR}$ | Equivalent Series Resistance | $V_{DD}$ = 5.0 V, $C_L$ = 12 pF @ 20 MHz, HSEGAIN = 0 | — | — | 110 | Ω |
| | | $V_{DD}$ = 2.5 V, $C_L$ = 12 pF @ 20 MHz, HSEGAIN = 1 | | | | |
| $D_{HSE}$ | HSE Oscillator Duty Cycle | — | 40 | — | 60 | % |
| $I_{DDHSE}$ | HSE Oscillator Current Consumption | $V_{DD}$ = 5.0 V, $R_{ESR}$ = 100 Ω, $C_L$ = 12 pF @ 8 MHz, HSEGAIN = 0 | — | 0.85 | — | mA |
| | | $V_{DD}$ = 5.0 V, $R_{ESR}$ = 25 Ω, $C_L$ = 12 pF @ 20 MHz, HSEGAIN = 1 | — | 3.0 | — | |
| $I_{PWDHSE}$ | HSE Oscillator Power Down Current | $V_{DD}$ = 5.0 V | — | — | 0.01 | μA |
| $t_{SUHSE}$ | HSE Oscillator Startup Time | $V_{DD}$ = 5.0 V | — | — | 4 | ms |

### Table 17. Low Speed External Clock (LSE) Characteristics

$T_A$ = 25 °C, unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operation Range | $T_A$ = -40 °C ~ 85 °C | 2.5 | — | 5.5 | V |
| $f_{CK\_LSE}$ | LSE Frequency | $V_{DD}$ = 2.5 V ~ 5.5 V | — | 32.768 | — | kHz |
| $R_F$ | Internal Feedback Resistor | — | — | 10 | — | MΩ |
| $R_{ESR}$ | Equivalent Series Resistance | $V_{DD}$ = 5.0 V | 30 | — | TBD | kΩ |
| $C_L$ | Recommended Load Capacitances | $V_{DD}$ = 5.0 V | 6 | — | TBD | pF |
| $I_{DDLSE}$ | Oscillator Supply Current (High current mode) | $f_{CK\_LSE}$ = 32.768 kHz, $R_{ESR}$ = 50 kΩ, $C_L \geq 7$ pF, $V_{DD}$ = 2.5 V ~ 5.5 V, $T_A$ = -40 °C ~ 85 °C | — | 4.0 | 5.6 | μA |
| | Oscillator Supply Current (Low Current Mode) | $f_{CK\_LSE}$ = 32.768 kHz, $R_{ESR}$ = 50 kΩ, $C_L < 7$ pF, $V_{DD}$ = 2.5 V ~ 5.5 V, $T_A$ = -40 °C ~ 85 °C | — | 3.6 | 4.5 | μA |
| | Power Down Current | — | — | — | 0.01 | μA |
| $t_{SULSE}$ | Startup Time (Low Current Mode) | $f_{CK\_LSI}$ = 32.768 kHz, $V_{DD}$ = 2.5 V ~ 5.5 V | 500 | — | — | ms |

Note: The following guidelines are recommended to increase the stability of the crystal circuit of the HSE / LSE clock in the PCB layout:

1. The crystal oscillator should be located as close as possible to the MCU to keep the trace lengths as short as possible to reduce any parasitic capacitance.
2. Shield lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
3. Keep any high frequency signal lines away from the crystal area to prevent any crosstalk adverse effects.

## Internal Clock Characteristics

### Table 18. High Speed Internal Clock (HSI) Characteristics

$T_A$ = 25 °C, unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operation Range | $T_A$ = -40 °C ~ 85 °C | 2.5 | — | 5.5 | V |
| $f_{HSI}$ | HSI Frequency | $V_{DD}$ = 5 V @ 25 °C | — | 20 | — | MHz |
| $ACC_{HSI}$ | Factory Calibrated HSI Oscillator Frequency Accuracy | $V_{DD}$ = 5.0 V, $T_A$ = 25 °C | -2 | — | 2 | % |
| | | $V_{DD}$ = 2.5 V ~ 5.5 V<br>$T_A$ = -40 °C ~ 85 °C | -3 | — | 3 | % |
| Duty | Duty Cycle | $f_{HSI}$ = 20 MHz | 35 | — | 65 | % |
| $I_{DDHSI}$ | Oscillator Supply Current | $f_{HSI}$ = 20 MHz @<br>$V_{DD}$ = 2.5 V ~ 5.5 V | — | — | 140 | μA |
| | Power Down Current | | — | — | 0.01 | μA |
| $T_{SUHSI}$ | HSI Oscillator Startup time | $f_{HSI}$ = 20 MHz | — | — | 20 | μs |

### Table 19. Low Speed Internal Clock (LSI) Characteristics

$T_A$ = 25 °C, unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operation Range | $T_A$ = -40 °C ~ 85 °C | 2.5 | — | 5.5 | V |
| $f_{LSI}$ | Low Speed Internal Oscillator Frequency (LSI) | $V_{DD}$ = 5.0 V,<br>$T_A$ = -40 °C ~ 85 °C | 21 | 32 | 43 | kHz |
| $ACC_{LSI}$ | LSI Frequency Accuracy | $V_{DD}$ = 5.0 V,<br>with factory-trimmed | -10 | — | +10 | % |
| $I_{DDLSI}$ | LSI Oscillator Operating Current | $V_{DD}$ = 5.0 V | — | 0.5 | 0.8 | μA |
| $t_{SULSI}$ | LSI Oscillator Startup Time | $V_{DD}$ = 5.0 V | — | — | 100 | μs |

## Memory Characteristics

### Table 20. Flash Memory Characteristics

$T_A$ = 25 °C, unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $N_{ENDU}$ | Number of Guaranteed Program / Erase Cycles before failure (Endurance) | $T_A$ = -40 °C ~ 85 °C | 20 | — | — | K cycles |
| $t_{RET}$ | Data Retention Time | $T_A$ = -40 °C ~ 85 °C | 10 | — | — | Years |
| $t_{PROG}$ | Word Programming Time | $T_A$ = -40 °C ~ 85 °C | 20 | — | — | μs |
| $t_{ERASE}$ | Page Erase Time | $T_A$ = -40 °C ~ 85 °C | 2 | — | — | ms |
| $t_{MERASE}$ | Mass Erase Time | $T_A$ = -40 °C ~ 85 °C | 10 | — | — | ms |

## I/O Port Characteristics

### Table 21. I/O Port Characteristics

$T_A$ = 25 °C, unless otherwise specified.

| Symbol | Parameter | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{IL}$ | Low Level Input Current | 5.0 V I/O | $V_I$ = $V_{SS}$, On-chip pull-up resister disabled | — | — | 3 | μA |
| | | Reset pin | | — | — | 3 | μA |
| $I_{IH}$ | High Level Input Current | 5.0 V I/O | $V_I$ = $V_{DD}$, On-chip pull-down resister disabled | — | — | 3 | μA |
| | | Reset pin | | — | — | 3 | μA |
| $V_{IL}$ | Low Level Input Voltage | 5.0 V I/O | | -0.5 | — | $V_{DD}$ × 0.35 | V |
| | | Reset pin | | -0.5 | — | $V_{DD}$ × 0.35 | V |
| $V_{IH}$ | High Level Input Voltage | 5.0 V I/O | | $V_{DD}$ × 0.65 | — | $V_{DD}$ + 0.5 | V |
| | | Reset pin | | $V_{DD}$ × 0.65 | — | $V_{DD}$ + 0.5 | V |
| $V_{HYS}$ | Schmitt Trigger Input Voltage Hysteresis | 5.0 V I/O | | — | 0.12 × $V_{DD}$ | — | mV |
| | | Reset pin | | — | 0.12 × $V_{DD}$ | — | mV |
| $I_{OL}$ | Low Level Output Current (GPIO Sink Current) | 5.0 V I/O 4 mA drive, $V_{OL}$ = 0.6 V | | 4 | — | — | mA |
| | | 5.0 V I/O 8 mA drive, $V_{OL}$ = 0.6 V | | 8 | — | — | mA |
| | | 5.0 V I/O 12 mA drive, $V_{OL}$ = 0.6 V | | 12 | — | — | mA |
| | | 5.0 V I/O 16 mA drive, $V_{OL}$ = 0.6 V | | 16 | — | — | mA |
| $I_{OH}$ | High Level Output Current (GPIO Source Current) | 5.0 V I/O 4 mA drive, $V_{OH}$ = $V_{DD}$ - 0.6 V | | — | 4 | — | mA |
| | | 5.0 V I/O 8 mA drive, $V_{OH}$ = $V_{DD}$ - 0.6 V | | — | 8 | — | mA |
| | | 5.0 V I/O 12 mA drive, $V_{OH}$ = $V_{DD}$ - 0.6 V | | — | 12 | — | mA |
| | | 5.0 V I/O 16 mA drive, $V_{OH}$ = $V_{DD}$ - 0.6 V | | — | 16 | — | mA |
| $V_{OL}$ | Low Level Output Voltage | 5.0 V 4 mA drive I/O, $I_{OL}$ = 4 mA | | — | — | 0.6 | V |
| | | 5.0 V 8 mA drive I/O, $I_{OL}$ = 8 mA | | — | — | 0.6 | V |
| | | 5.0 V 12 mA drive I/O, $I_{OL}$ = 12 mA | | — | — | 0.6 | V |
| | | 5.0 V 16 mA drive I/O, $I_{OL}$ = 16 mA | | — | — | 0.6 | V |
| $V_{OH}$ | High Level Output Voltage | 5.0 V 4 mA drive I/O, $I_{OH}$ = 4 mA | | $V_{DD}$ - 0.6 | — | — | V |
| | | 5.0 V 8 mA drive I/O, $I_{OH}$ = 8 mA | | $V_{DD}$ - 0.6 | — | — | V |
| | | 5.0 V 12 mA drive I/O, $I_{OH}$ = 12 mA | | $V_{DD}$ - 0.6 | — | — | V |
| | | 5.0 V 16 mA drive I/O, $I_{OH}$ = 16 mA | | $V_{DD}$ - 0.6 | — | — | V |
| $R_{PU}$ | Internal Pull-up Resistor | $V_{DD}$ = 5.0 V | | — | 50 | — | kΩ |
| | | $V_{DD}$ = 3.3 V | | — | 76 | — | kΩ |
| $R_{PD}$ | Internal Pull-down Resistor | $V_{DD}$ = 5.0 V | | — | 50 | — | kΩ |
| | | $V_{DD}$ = 3.3 V | | — | 76 | — | kΩ |

## ADC Characteristics

### Table 22. ADC Characteristics

$T_A$ = 25 °C, unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Operating Voltage | — | 2.5 | 5 | 5.5 | V |
| $V_{ADCIN}$ | A/D Converter Input Voltage Range | — | 0 | — | $V_{REF+}$ | V |
| $V_{REF+}$ | A/D Converter Reference Voltage | — | — | $V_{DDA}$ | $V_{DDA}$ | V |
| $I_{ADC}$ | Current Consumption | $V_{DDA}$ = 5.0 V | — | 1.4 | 1.5 | mA |
| $I_{ADC\_DN}$ | Power Down Current Consumption | $V_{DDA}$ = 5.0 V | — | — | 0.1 | μA |
| $f_{ADC}$ | A/D Converter Clock Frequency | — | 0.7 | — | 16 | MHz |
| $f_S$ | Sampling Rate | — | 0.05 | — | 1 | Msps |
| $t_{DL}$ | Data Latency | — | — | 12.5 | — | $1/f_{ADC}$ Cycles |
| $t_{S\&H}$ | Sampling & Hold Time | — | — | 3.5 | — | $1/f_{ADC}$ Cycles |
| $t_{ADCCONV}$ | A/D Converter Conversion Time | ADST[7:0] = 2 | — | 16 | — | $1/f_{ADC}$ Cycles |
| $R_I$ | Input Sampling Switch Resistance | — | — | — | 1 | kΩ |
| $C_I$ | Input Sampling Capacitance | No pin / pad capacitance included | — | 4 | — | pF |
| $t_{SU}$ | Startup Time | — | — | — | 1 | μs |
| N | Resolution | — | — | 12 | — | bits |
| INL | Integral Non-linearity Error | $f_S$ = 750 ksps, $V_{DDA}$ = 5.0 V | — | ±2 | ±5 | LSB |
| DNL | Differential Non-linearity Error | $f_S$ = 750 ksps, $V_{DDA}$ = 5.0 V | — | ±1 | — | LSB |
| $E_O$ | Offset Error | — | — | — | ±10 | LSB |
| $E_G$ | Gain Error | — | — | — | ±10 | LSB |

Note: 1. Data based on characterization results only, not tested in production.

2. Due to the A/D Converter input channel and GPIO pin-shared function design limitation, the $V_{DDA}$ supply power of the A/D Converter has to be equal to the $V_{DD}$ supply power of the MCU in the application circuit.

3. The figure below shows the equivalent circuit of the A/D Converter Sample-and-Hold input stage where $C_I$ is the storage capacitor, $R_I$ is the resistance of the sampling switch and $R_S$ is the output impedance of the signal source $V_S$. Normally the sampling phase duration is approximately, $3.5/f_{ADC}$. The capacitance, $C_I$, must be charged within this time frame and it must be ensured that the voltage at its terminals becomes sufficiently close to $V_S$ for accuracy. To guarantee this, $R_S$ is not allowed to have an arbitrarily large value.

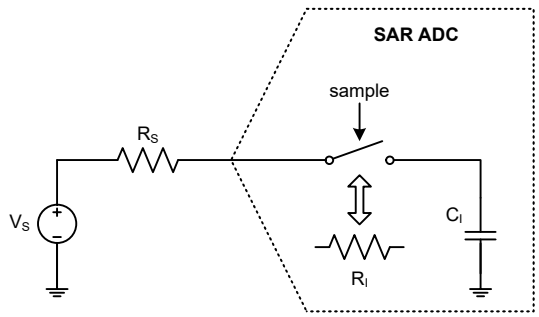



**Figure 12. ADC Sampling Network Model**

The worst case occurs when the extremities of the input range (0 V and $V_{REF}$) are sampled consecutively. In this situation a sampling error below 1/4 LSB is ensured by using the following equation:

$$R_S < \frac{3.5}{f_{ADC} C_I \ln(2^{N+2})} - R_I$$

Where $f_{ADC}$ is the ADC clock frequency and N is the ADC resolution (N = 12 in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model.

If, in a system where the A/D Converter is used, there are no rail-to-rail input voltage variations between consecutive sampling phases, $R_S$ may be larger than the value indicated by the equation above.



# MCTM/GPTM/PWM Characteristics

**Table 23. MCTM/GPTM/PWM Characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{TM}$ | Timer Clock Source for MCTM, GPTM and PWM | — | — | — | $f_{PCLK}$ | MHz |
| $t_{RES}$ | Timer Resolution Time | — | 1 | — | — | $1/f_{TM}$ |
| $f_{EXT}$ | External Single Frequency on Channel 1 ~ 4 | — | — | — | 1/2 | $f_{TM}$ |
| RES | Timer Resolution | — | — | — | 16 | bits |

# PD PHY Characteristics

## PD PHY Operating Voltage Characteristics

**Table 24. PD PHY Operating Voltage Characteristics**

$T_A$ = -40 °C ~ 85 °C

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD\_PD}$ | Operating Voltage | — | 2.6 | — | 5.5 | V |

## PD PHY Operating Current Characteristics

**Table 25. PD PHY Operating Current Characteristics**

$T_A$ = -40 °C ~ 85 °C

| Symbol | Operating Mode | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{DD\_PD}$ | Normal Mode | $V_{DD\_PD}$ = 3 V, PWR[3:0] = 0xD | — | 1.5 | 3 | mA |
| | | $V_{DD\_PD}$ = 5 V, PWR[3:0] = 0xD | — | 2 | 5 | mA |
| | SLEEP1 Mode | $V_{DD\_PD}$ = 3 V, PWR[3:0] = 0x2 | — | 10 | 20 | μA |
| | | $V_{DD\_PD}$ = 5 V, PWR[3:0] = 0x2 | — | 20 | 60 | μA |
| | SLEEP0 Mode | $V_{DD\_PD}$ = 3 V, PWR[3:0] = 0x0 | — | 3 | 6 | μA |
| | | $V_{DD\_PD}$ = 5 V, PWR[3:0] = 0x0 | — | 5 | 45 | μA |

## PD PHY LDO Characteristics

### Table 26. PD PHY LDO Characteristics

$V_{DD\_PD}$ = $V_{IN}$, $V_{IN}$ = $V_{OUT}$ + 0.8 V, $C_{LOAD}$ = 4.7 μF, $T_A$ = -40 °C ~ 85 °C, unless otherwise specified

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD\_PD}$ | Supply Voltage | — | 2.6 | — | 5.5 | V |
| $V_{OUT}$ | Output Voltage | $T_A$ = 25 °C, $I_{LOAD}$ = 0.5 mA | -4% | 1.8 | 4% | V |
| | | $I_{LOAD}$ = 0.5 mA | -8% | 1.8 | 8% | V |
| $I_Q$ | Quiescent Current | $V_{DD\_PD}$ = 5 V, No load | — | — | 10 | μA |
| $I_{OUT}$ | Output Current | $V_{IN}$ = 2.6 V, $\Delta V_{OUT}$ = 0.15 V, $V_{OUT}$ = 1.8 V | 5 | — | — | mA |
| TC | Temperature Coefficient | $I_{LOAD}$ = 5 mA | — | ±1.5 | ±2 | mV/°C |

## PD PHY HVO Characteristics

### Table 27. PD PHY HVO Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{OL}$ | Sink Current for HVO1, HVO2 Pins | $V_{DD\_PD}$ = 5 V, $V_{OL}$ = 0.1 $V_{DD\_PD}$ | 20 | 35 | — | mA |

## PD PHY Characteristics

### Table 28. PD PHY Characteristics

$T_A$ = -40 °C ~ 85 °C

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{VCONN}$ | VCONN Voltage | — | 3 | — | 5.5 | V |
| $V_{CCOVP}$ | CC1, CC2 Over Voltage Protection | — | -6% | $V_{DD\_PD}$ | 5% | V |
| $I_{AVDD}$ | AVDD Current while Waiting to Receive | — | — | 35 | — | μA |
| $I_{RX}$ | AVDD Current while Receiving | CDR_SELECT = 0 | — | 250 | — | μA |
| $I_{TX}$ | AVDD Current while Transmitting | — | — | — | 1.5 | mA |
| $I_{CC1LK}$ | CC1 Pins Leakage Current | — | — | — | 5 | μA |
| $I_{CC2LK}$ | CC2 Pins Leakage Current | — | — | — | 5 | μA |
| $V_{REF}$ | DAC Reference Voltage | — | 2.5 | 2.6 | 2.7 | V |
| $N_R$ | DAC Resolution | — | — | 6 | — | Bit |
| $V_{DAC}$ | DAC Threshold | DAC[5:0] = 000000b ~ 111111b | -60 | — | +40 | mV |
| $V_{SLC2}$ | Upper Slice Voltage Comparator Reference | — | 800 | 850 | 880 | mV |
| $V_{SLC1}$ | Middle Slice Voltage Comparator Reference | — | 520 | 550 | 590 | mV |
| $V_{SLC0}$ | Lower Slice Voltage Comparator Reference | — | 220 | 250 | 280 | mV |
| $T_{SLCT}$ | Slice Analog Activity Test Timer Time | — | 15 | — | 35 | μs |
| $V_{TH3}$ | 3 A CC Detect Threshold | — | 1.12 | 1.16 | 1.25 | V |
| $V_{TH1P5}$ | 1.5 A CC Detect Threshold | — | 580 | 610 | 640 | mV |
| $V_{TH\_DEF}$ | Default Current CC Detect Threshold | — | 160 | 200 | 250 | mV |
| $V_{RDTH330}$ | $R_D$ Voltage Threshold for 330 μA Pull Up | — | 1.9 | 2.4 | 2.7 | V |
| $V_{RDTH180}$ | $R_D$ Voltage Threshold for 180 μA Pull Up | — | 1.5 | 1.6 | 1.7 | V |
| $V_{RDTH80}$ | $R_D$ Voltage Threshold for 80 μA Pull Up | — | 1.5 | 1.6 | 1.7 | V |
| $V_{RATH330}$ | $R_A$ Voltage Threshold for 330 μA Pull Up | — | 760 | 800 | 830 | mV |
| $V_{RATH180}$ | $R_A$ Voltage Threshold for 180 μA Pull Up | — | 280 | 320 | 420 | mV |

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{RATH80}$ | $R_A$ Voltage Threshold for 80 μA Pull Up | — | 180 | 200 | 225 | mV |
| $f_{I2C}$ | I²C Clock Frequency | — | 400 | — | 1000 | kHz |

## PD PHY Power on Reset Characteristics

### Table 29. PD PHY Power on Reset Characteristics

$T_A$ = -40 °C ~ 85 °C

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{POR\_PD}$ | $V_{DD\_PD}$ Start Voltage to Ensure Power-on Reset | — | — | — | 100 | mV |
| $RR_{POR\_PD}$ | $V_{DD\_PD}$ Rising Rate to Ensure Power-on Reset | — | 0.035 | — | — | V/ms |
| $t_{POR\_PD}$ | Minimum Time for $V_{DD\_PD}$ Stays at $V_{POR\_PD}$ to Ensure Power-on Reset | — | 1 | — | — | ms |

# I²C Characteristics

### Table 30. I²C Characteristics

| Symbol | Parameter | Standard Mode | | Fast Mode | | Fast Plus Mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $f_{SCL}$ | SCL Clock Frequency | — | 100 | — | 400 | — | 1000 | kHz |
| $t_{SCL(H)}$ | SCL Clock High Time | 4.5 | — | 1.125 | — | 0.45 | — | μs |
| $t_{SCL(L)}$ | SCL Clock Low Time | 4.5 | — | 1.125 | — | 0.45 | — | μs |
| $t_{FALL}$ | SCL And SDA Fall Time | — | 1.3 | — | 0.34 | — | 0.135 | μs |
| $t_{RISE}$ | SCL And SDA Rise Time | — | 1.3 | — | 0.34 | — | 0.135 | μs |
| $t_{SU(SDA)}$ | SDA Data Setup Time | 500 | — | 125 | — | 50 | — | ns |
| $t_{H(SDA)}$ | SDA Data Hold Time (5) | 0 | — | 0 | — | 0 | — | ns |
| | SDA Data Hold Time (6) | 100 | — | 100 | — | 100 | — | ns |
| $t_{VD(SDA)}$ | SDA Data Valid Time | — | 1.6 | — | 0.475 | — | 0.25 | μs |
| $t_{SU(STA)}$ | START Condition Setup Time | 500 | — | 125 | — | 50 | — | ns |
| $t_{H(STA)}$ | START Condition Hold Time | 0 | — | 0 | — | 0 | — | ns |
| $t_{SU(STO)}$ | STOP Condition Setup Time | 500 | — | 125 | — | 50 | — | ns |

Note: 1. Data based on characterization results only, not tested in production.

2. To achieve 100 kHz standard mode, the peripheral clock frequency must be higher than 2 MHz.

3. To achieve 400 kHz fast mode, the peripheral clock frequency must be higher than 8 MHz.

4. To achieve 1 MHz fast mode plus, the peripheral clock frequency must be higher than 20 MHz.

5. The above characteristic parameters of the I²C bus timing are based on: COMBFILTEREN = 0 and SEQFILTER = 00.

6. The above characteristic parameters of the I²C bus timing are based on: COMBFILTEREN = 1 and SEQFILTER = 00.

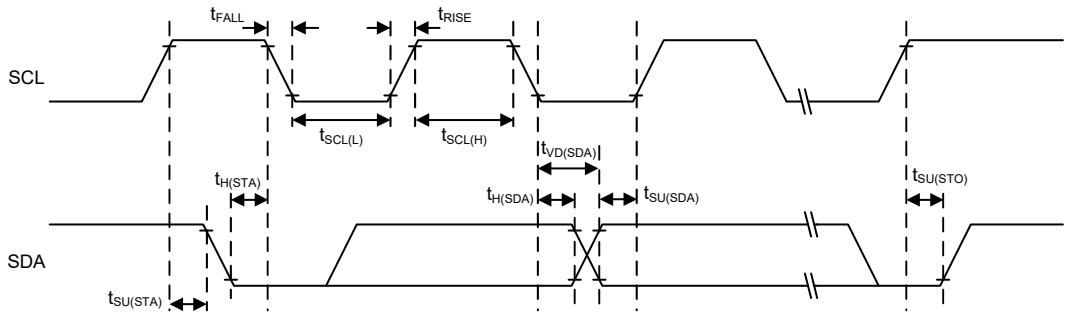



**Figure 13. I²C Timing Diagrams**

## SPI Characteristics

**Table 31. SPI Characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **SPI Master Mode** | | | | | | |
| $f_{SCK}$ | SPI Master Output SCK Clock Frequency | Master mode, SPI peripheral clock frequency $f_{PCLK}$ | — | — | $f_{PCLK}/2$ | MHz |
| $t_{SCK(H)}$ $t_{SCK(L)}$ | SCK Clock High and Low Time | — | $t_{SCK}/2$ - 2 | — | $t_{SCK}/2$ + 1 | ns |
| $t_{V(MO)}$ | Data Output Valid Time | — | — | — | 5 | ns |
| $t_{H(MO)}$ | Data Output Hold Time | — | 2 | — | — | ns |
| $t_{SU(MI)}$ | Data Input Setup Time | — | 5 | — | — | ns |
| $t_{H(MI)}$ | Data Input Hold Time | — | 5 | — | — | ns |
| **SPI Slave Mode** | | | | | | |
| $f_{SCK}$ | SPI Slave Input SCK Clock Frequency | Slave mode, SPI peripheral clock frequency $f_{PCLK}$ | — | — | $f_{PCLK}/3$ | MHz |
| $Duty_{SCK}$ | SPI Slave Input SCK Clock Duty Cycle | — | 30 | — | 70 | % |
| $t_{SU(SEL)}$ | SEL Enable Setup Time | — | 3 $t_{PCLK}$ | — | — | ns |
| $t_{H(SEL)}$ | SEL Enable Hold Time | — | 2 $t_{PCLK}$ | — | — | ns |
| $t_{A(SO)}$ | Data Output Access Time | — | — | — | 3 $t_{PCLK}$ | ns |
| $t_{DIS(SO)}$ | Data Output Disable Time | — | — | — | 10 | ns |
| $t_{V(SO)}$ | Data Output Valid Time | — | — | — | 25 | ns |
| $t_{H(SO)}$ | Data Output Hold Time | — | 15 | — | — | ns |
| $t_{SU(SI)}$ | Data Input Setup Time | — | 5 | — | — | ns |
| $t_{H(SI)}$ | Data Input Hold Time | — | 4 | — | — | ns |

Note: 1. $f_{SCK}$ is SPI output/input clock frequency and $t_{SCK} = 1/f_{SCK}$.
2. $f_{PCLK}$ is SPI peripheral clock frequency and $t_{PCLK} = 1/f_{PCLK}$.

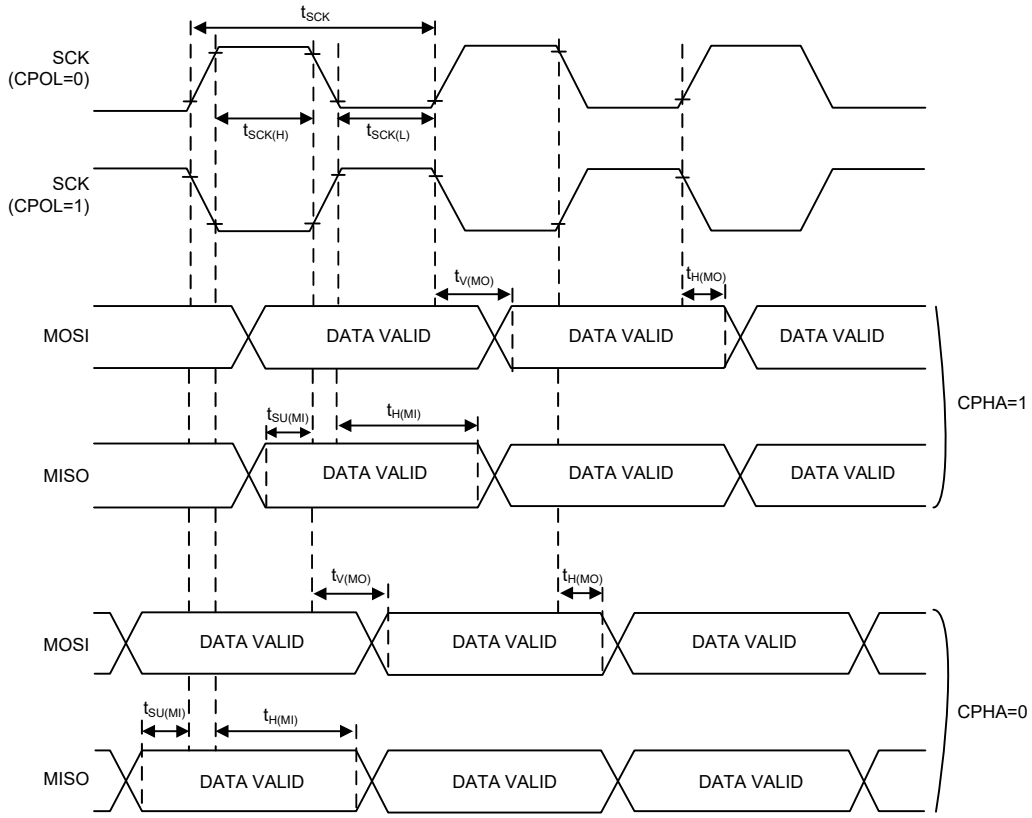



**Figure 14. SPI Timing Diagrams – SPI Master Mode**

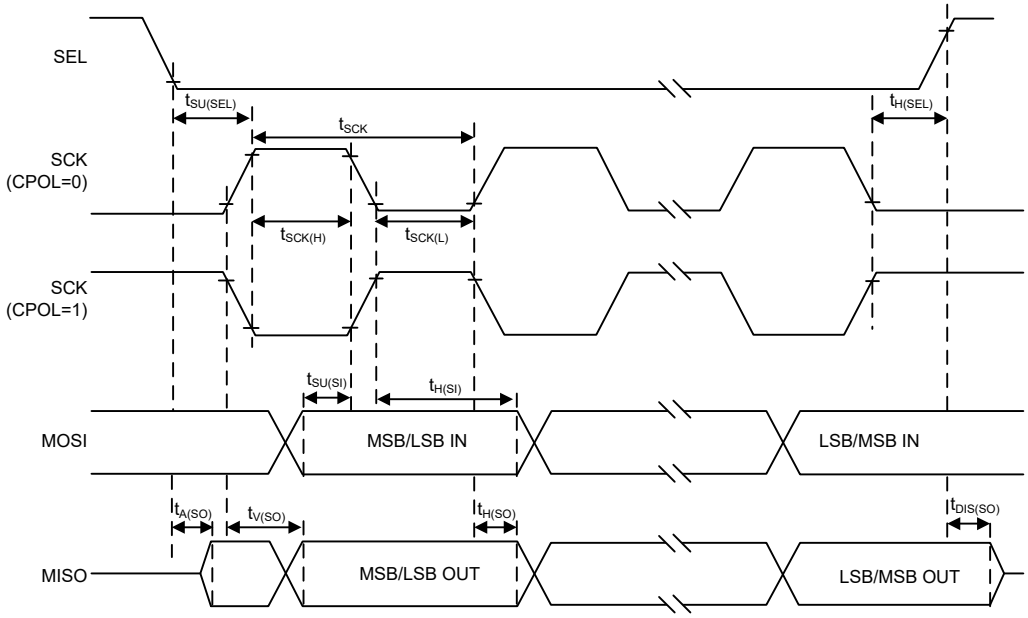



**Figure 15. SPI Timing Diagrams – SPI Slave Mode with CPHA=1**

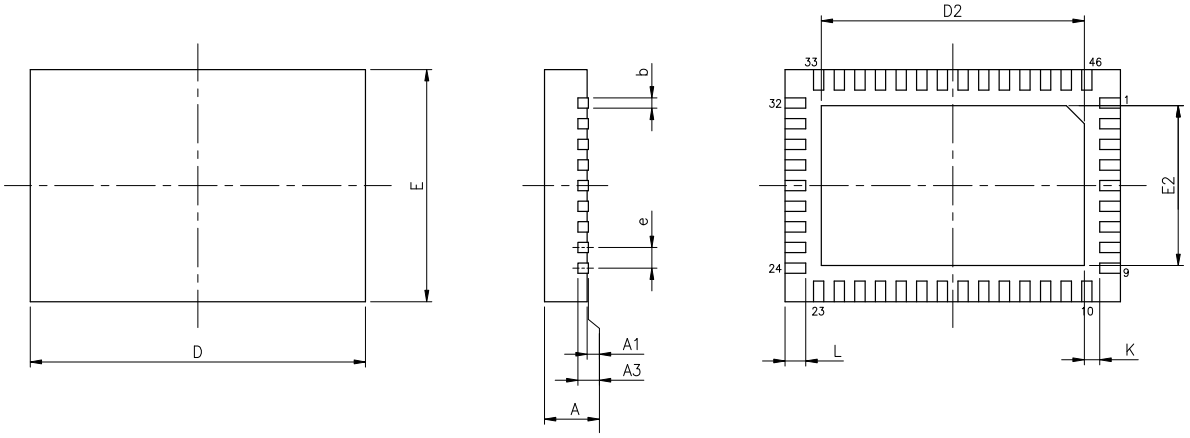
# 8 Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

## SAW Type 46-pin QFN (6.5mm × 4.5mm × 0.75mm) Outline Dimensions




| Symbol | Dimensions in inch | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | 0.028 | 0.030 | 0.031 |
| A1 | 0.000 | 0.001 | 0.002 |
| A3 | | 0.008 REF | |
| b | 0.006 | 0.008 | 0.010 |
| D | | 0.256 BSC | |
| E | | 0.177 BSC | |
| e | | 0.016 BSC | |
| D2 | 0.197 | — | 0.205 |
| E2 | 0.118 | — | 0.126 |
| L | 0.014 | 0.016 | 0.018 |
| K | 0.008 | — | — |

| Symbol | Dimensions in mm | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.203 REF | |
| b | 0.15 | 0.20 | 0.25 |
| D | | 6.50 BSC | |
| E | | 4.50 BSC | |
| e | | 0.40 BSC | |
| D2 | 5.00 | — | 5.20 |
| E2 | 3.00 | — | 3.20 |
| L | 0.35 | 0.40 | 0.45 |
| K | 0.20 | — | — |