HT32F59041
Datasheet

Enhanced 24-bit A/D Arm® Cortex®-M0+ Flash MCU
64 KB Flash and 8 KB SRAM with 1 MSPS 12-Bit ADC
24-Bit Delta Sigma ADC, DIV, USART, UART, SPI, I^2C
MCTM, GPTM, BFTM, PWM, CRC, RTC and WDT

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1 General Description

The Holtek HT32F59041 device is a high performance, low power consumption 32-bit microcontroller based around an Arm® Cortex®-M0+ processor core. The Cortex®-M0+ is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer, and including advanced debug support.

The device operates at a frequency of up to 20 MHz with a Flash accelerator to obtain maximum efficiency. It provides 64 KB of embedded Flash memory for code/data storage and 8 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as Hardware Divider DIV, ADC, I^2C, USART, UART, SPI, MCTM, GPTM, PWM, BFTM, CRC-16/32, RTC, WDT, SW-DP (Serial Wire Debug Port), etc., are also implemented in the device. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The device also contains a multi-channel 24-bit Delta Sigma A/D converter which includes a programmable gain amplifier and is designed for applications that interface differentially to analog signals.

The above features ensure that the device is suitable for use in a wide range of applications, especially in areas such as white goods application controllers, power monitors, alarm systems, consumer products, handheld equipment, data logging applications, motor controllers and so on.

2 Features

Core

- 32-bit Arm® Cortex®-M0+ processor core
- Up to 20 MHz operating frequency
- Single-cycle multiplication
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized, low-power processor. The processor is based on the ARMv6-M architecture and supports Thumb® instruction sets, single-cycle I/O port, hardware multiplier and low latency interrupt respond time.

On-chip Memory

- 64 KB on-chip Flash memory for instruction/data and options storage
- 8 KB on-chip SRAM
- Supports multiple boot modes

The Arm® Cortex®-M0+ processor accesses and debug accesses share the single external interface to external AHB peripherals. The processor accesses take priority over debug accesses. The maximum address range of the Cortex®-M0+ is 4 GB since it has a 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex®-M0+ processor to reduce the software complexity of repeated implementation by different device vendors. However, some regions are used by the Arm® Cortex®-M0+ system peripherals. Refer to the Arm® Cortex®-M0+ Technical Reference Manual for more information. Figure 2 in the Overview chapter shows the memory map of the device, including code, SRAM, peripheral and other pre-defined regions.

Flash Memory Controller – FMC

- 32-bit word programming with In System Programming Interface (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions for the embedded on-chip Flash Memory. The word program/page erase functions are also provided.

Reset Control Unit – RSTCU

- Supply supervisor:
  - Power on Reset / Power down Reset – POR / PDR
  - Brown-out Detector – BOD
  - Programmable Low Voltage Detector – LVD

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by external signals, internal events and the reset generators.

Clock Control Unit – CKCU

- External 4 to 20 MHz crystal oscillator
- External 32.768 kHz crystal oscillator
- Internal 20 MHz RC oscillator trimmed to ±2 % accuracy at 25 °C operating temperature
- Internal 32 kHz RC oscillator
- Independent clock divider and gating bits for peripheral clock sources

The Clock Control Unit, CKCU, provides a range of oscillator and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), an HSE clock monitor, clock pre-scalers, clock multiplexers, APB clock divider and gating circuitry. The AHB, APB and Cortex®-M0+ clocks are derived from the system clock (CK_SYS) which can come from the HSI, HSE, LSI or LSE. The Watchdog Timer and Real Time Clock (RTC) use either the LSI or LSE as their clock source.

Power Management Control Unit – PWRCU

- Single V_{DD} power supply: 2.5 V to 5.5 V
- Integrated 1.5 V LDO regulator for CPU core, peripherals and memories power supply
- Two power domains: V_{DD} and 1.5 V
- Three power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in the device provides many types of power saving modes such as Sleep, Deep-Sleep1 and Deep-Sleep2 mode. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.

Real Time Clock – RTC

- 24-bit up-counter with a programmable prescaler
- Alarm function
- Interrupt and Wake-up event

The Real Time Clock, RTC, includes an APB interface, a 24-bit count-up counter, a control register, a prescaler, a compare register and a status register. The RTC circuits are located in the V_{DD15} power domain. The RTC counter is used as a wakeup timer to generate a system resume or interrupt signal from the MCU power saving mode.

External Interrupt / Event Controller – EXTI

- Up to 16 EXTI lines with configurable trigger source and type
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge, or both edges
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

The External Interrupt/Event Controller, EXTI, comprises 16 edge detectors which can generate a wake-up event or interrupt requests independently. Each EXTI line can also be masked independently.

Hardware Divider – DIV

- Signed/unsigned 32-bit divider
- Operation in 8 clock cycles, load in 1 clock cycle
- Divide by zero error Flag

The divider is the truncated division and needs a software triggered start signal by using the control register "START" bit. After 8 clock cycles, the divider calculate complete flag will be set to 1, and if the divisor register data is zero, the divide by zero error flag will be set to 1.

12-Bit Analog to Digital Converter – ADC

- 12-bit SAR ADC engine
- Up to 1 Msps conversion rate
- Up to 12 external analog input channels

A 12-bit multi-channel ADC is integrated in the device. There are multiplexed channels, which include 12 external analog signal channels and 2 internal channels which can be measured. If the input voltage is required to remain within a specific threshold window, an Analog Watchdog function will monitor and detect these signals. An interrupt will then be generated to inform the device that the input voltage is not within the preset threshold levels. There are three conversion modes to convert an analog signal to digital data. The ADC can be operated in one shot, continuous and discontinuous conversion modes.

24-Bit Delta Sigma Analog to Digital Converter – ΔΣ ADC

- Internal Programmable Gain Amplifier
- Internal I^2C interface for external communication
- 5 Hz ~ 1.6 kHz ADC output data rate
- Internal temperature sensor for compensation

I/O Ports – GPIO

- 30 GPIOs
- Port A, B, C are mapped as 16 external interrupts – EXTI
- Almost all I/O pins have configurable output driving current

There are 30 General Purpose I/O pins, GPIO, for the implementation of logic input/output functions. Each of the GPIO ports has a series of related control and configuration registers to maximize flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

Basic Function Timer – BFTM

- One 32-bit compare match count-up counter – no I/O control features
- One shot mode – counting stops after compare match occurs
- Repetitive mode – restart counter when compare match occurs

The Basic Function Timer is a simple 32-bit up-counting counter designed to measure time intervals and generate a one shot or repetitive interrupts. The BFTM operates in two functional modes, repetitive and one shot modes. In the repetitive mode, the BFTM restarts the counter when a compare match event occurs. The BFTM also supports a one shot mode which forces the counter to stop counting when a compare match event occurs.

Motor Control Timer – MCTM

- One 16-bit up, down, up/down auto-reload counter
- 16-bit programmable prescaler allowing counter clock frequency divided by any factor between 1 and 65536
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output
- Complementary Outputs with programmable dead-time insertion
- Break input to force the timer's output signals into a reset or fixed condition

The Motor Control Timer consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR), one 8-bit repetition counter and several control/status registers. It can be used for a variety of purposes including measuring the pulse width of input signals or generating output waveforms such as compare match outputs, PWM outputs or complementary PWM outputs with dead-time insertion. The MCTM is capable of offering full functional support for motor control, hall sensor interfacing and break input.

PWM Generation and Capture Timer – GPTM

- One 16-bit up, down, up/down auto-reload counter
- Up to 4 independent channels for each timer
- 16-bit programmable prescaler allowing the counter clock frequency devided by any factor between 1 and 65536
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder

The General Purpose Timer consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR) and several control/status registers. They can be used for a variety of purposes including general time measurement, input signal pulse width measurement, output waveform generation such as single pulse generation or PWM output generation. The GPTM supports an Encoder Interface using a decoder with two inputs.

Pulse Width Modulation – PWM

- One 16-bit up, down, up/down auto-reload counter
- Up to 4 independent channels for each timer
- 16-bit programmable prescaler allowing counter clock frequency divided by any factor between 1 and 65536
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output

The Pulse Width Modulator consists of one 16-bit up/down-counter, four 16-bit Compare Registers (CRs), one 16-bit Counter-Reload Register (CRR) and several control/status registers. It can be used for a variety of purposes including general timer and output waveform generation such as single pulse generation or PWM output.

Watchdog Timer – WDT

- 12-bit down counter with 3-bit prescaler
- Reset event for the system
- Programmable watchdog timer window function
- Register write protection function

The Watchdog Timer is a hardware timing circuit that can be used to detect system failures due to software malfunctions. It includes a 12-bit count-down counter, a prescaler, a WDT delta value register, WDT operation control circuitry and a WDT protection mechanism. If the software does not reload the counter value before a Watchdog Timer underflow occurs, a reset will be generated when the counter underflows. In addition, a reset is also generated if the software reloads the counter when the counter value is greater than the WDT delta value. This means the counter must be reloaded within a limited timing window using a specific method. The Watchdog Timer counter can be stopped while the processor is in the debug mode. There is a register write protect function which can be enabled to prevent it from changing the Watchdog Timer configuration unexpectedly.

Inter-integrated Circuit – I^2C

- Supports both master and slave modes with a frequency of up to 1 MHz
- Provides an arbitration function and clock synchronization
- Supports 7-bit and 10-bit addressing modes and general call addressing
- Supports slave multi-addressing mode with address mask function

The I^2C is an internal circuit allowing communication with an external I^2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I^2C module provides three data transfer rates: 100 kHz in the Standard mode, 400 kHz in the Fast mode and 1 MHz in the Fast plus mode. The SCL period generation register is used to setup different kinds of duty cycle implementations for the SCL pulse.

The SDA line which is connected directly to the I^2C bus is a bi-directional data line between the master and slave devices and is used for data transmission and reception. The I^2C also has an arbitration detect function and clock synchronization to prevent situations where more than one master attempts to transmit data to the I^2C bus at the same time.

Serial Peripheral Interface – SPI

- Supports both master and slave modes
- Frequency of up to (f_{PCLK}/2) MHz for the master mode and (f_{PCLK}/3) MHz for the slave mode
- FIFO Depth: 8 levels
- Multi-master and multi-slave operation

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive function in both master and slave modes. The SPI interface uses 4 pins, which are the serial data input and output lines MISO and MOSI, the clock line, SCK, and the slave select line, SEL. One SPI device acts as a master device which controls the data flow using the SEL and SCK signals to indicate the start of data communication and the data sampling rate. To receive a data byte, the streamed data

bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but in a reverse sequence. The mode fault detection provides a capability for multi-master applications.

Universal Synchronous Asynchronous Receiver Transmitter – USART

- Supports both asynchronous and clocked synchronous serial communication modes
- Asynchronous operating baud-rate clock frequency up to (f_{PCLK}/16) MHz and synchronous operating clock frequency up to (f_{PCLK}/8) MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error
- Auto hardware flow control mode – RTS, CTS
- IrDA SIR encoder and decoder
- RS485 mode with output enable control
- FIFO Depth: 8 × 9 bits for both receiver and transmitter

The Universal Synchronous Asynchronous Receiver Transceiver, USART, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. The USART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The USART peripheral function supports four types of interrupt including Line Status Interrupt, Transmitter FIFO Empty Interrupt, Receiver Threshold Level Reaching Interrupt and Time Out Interrupt. The USART module includes a transmitter FIFO (TX FIFO) and receiver FIFO (RX FIFO). The software can detect a USART error status by reading the Line Status Register, LSR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Universal Asynchronous Receiver Transmitter – UART

- Asynchronous serial communication operating baud-rate clock frequency up to (f_{PCLK}/16) MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports Line Status Interrupt. The software can detect a UART error status by reading

the Line Status Register, LSR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Cyclic Redundancy Check – CRC

- Support CRC16 polynomial: 0x8005,
  $X^{16} + X^{15} + X^2 + 1$
- Support CCITT CRC16 polynomial: 0x1021,
  $X^{16} + X^{12} + X^5 + 1$
- Support IEEE-802.3 CRC32 polynomial: 0x04C11DB7,
  $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Supports 1's complement, byte reverse & bit reverse operation on data and checksum
- Supports byte, half-word & word data size
- Programmable CRC initial seed value
- CRC computation executed in 1 AHB clock cycle for 8-bit data and 4 AHB clock cycles for 32-bit data

The CRC calculation unit is an error detection technique test algorithm which is used to verify data transmission or storage data correctness. A CRC calculation takes a data stream or a block of data as its input and generates a 16-bit or 32-bit output remainder. Ordinarily, a data stream is suffixed by a CRC code and used as a checksum when being sent or stored. Therefore, the received or restored data stream is calculated by the same generator polynomial as described above. If the new CRC code result does not match the one calculated earlier, that means the data stream contains a data error.

Debug Support

- Serial Wire Debug Port – SW-DP
- 4 comparators for hardware breakpoint or code / literal patch
- 2 comparators for hardware watch points

Package and Operation Temperature

- 48-pin LQFP package
- Operation temperature range: -40 °C to + 85 °C

3 Overview

Device Information

Table 1. Features and Peripheral List

Peripherals		HT32F59041
Main Flash (KB)		63
Option Bytes Flash (KB)		1
SRAM (KB)		8
Timers	MCTM	1
	GPTM	1
	PWM	2
	BFTM	2
	WDT	1
	RTC	1
Communication	SPI	2
	USART	1
	UART	2
	I^2C	2
Hardware Divider		1
CRC-16/32		1
EXTI		16
12-bit ADC		1
Number of channels		12 Channels
24-bit ADC		1
Number of channels		4 Channels
GPIO		30
CPU frequency		Up to 20 MHz
Operating voltage		2.5 V ~ 5.5 V
Operating temperature		-40 °C ~ 85 °C
Package		48-pin LQFP

Note: The detailed functions listed here, except the 24-bit Delta Sigma A/D Converter, are compatible with the HT32F50241 device. Refer to the HT32F50241 user manual for detailed function descriptions.

Block Diagram

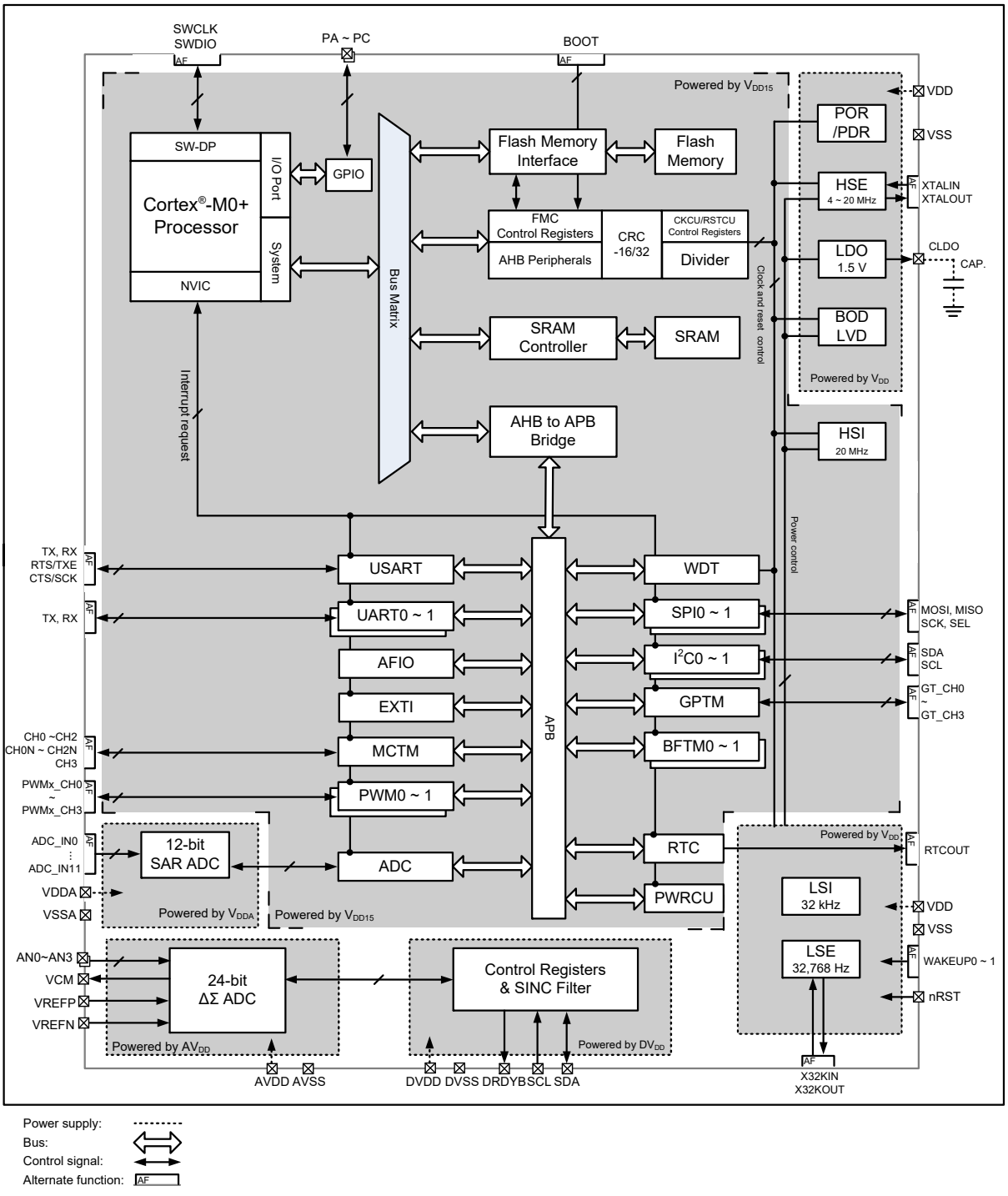


Figure 1. Block Diagram

Memory Map

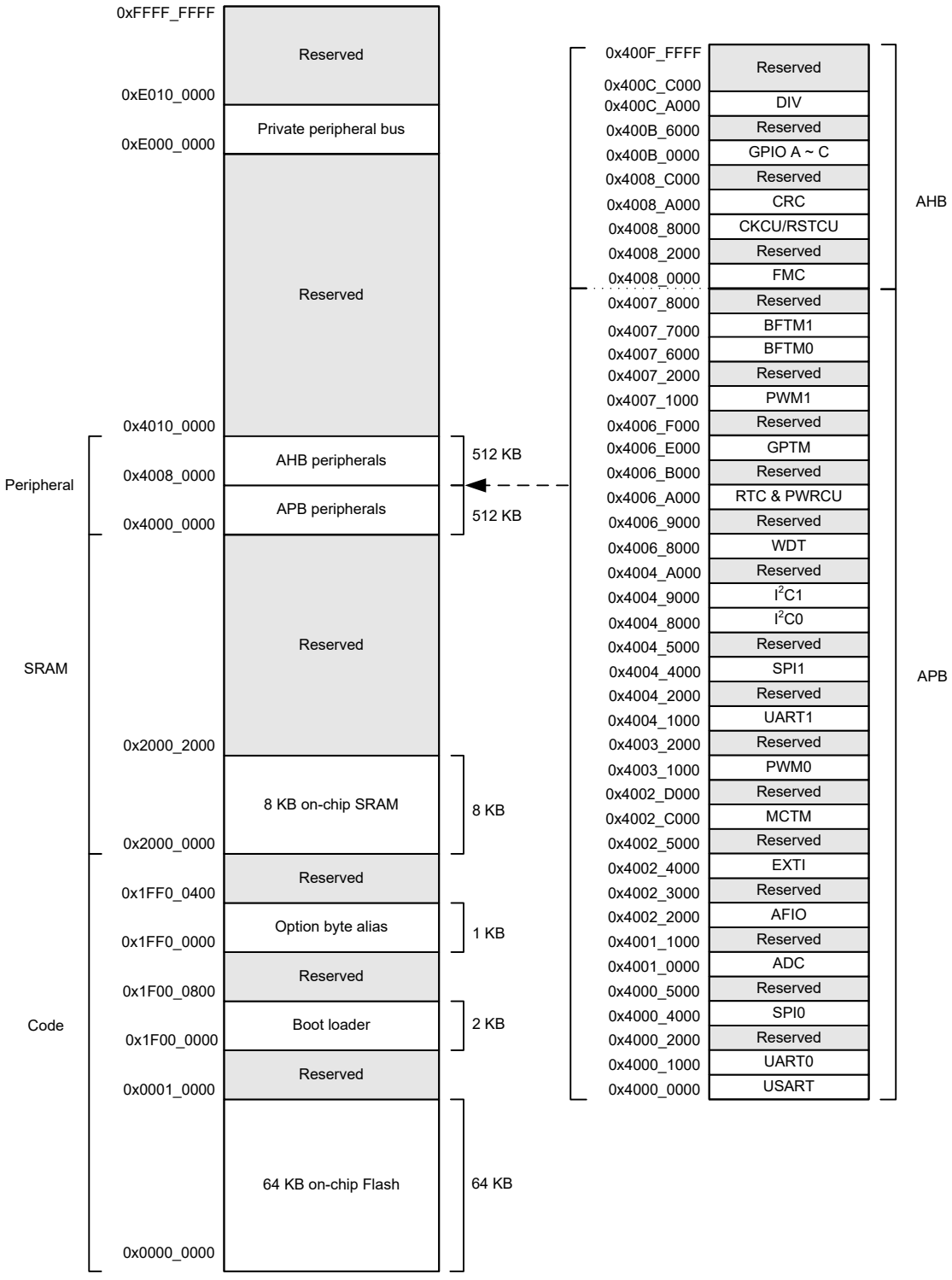


Figure 2. Memory Map

Table 2. Register Map

Start Address	End Address	Peripheral	Bus
0x4000_0000	0x4000_0FFF	USART	
0x4000_1000	0x4000_1FFF	UART0	
0x4000_2000	0x4000_3FFF	Reserved	
0x4000_4000	0x4000_4FFF	SPI0	
0x4000_5000	0x4000_FFFF	Reserved	
0x4001_0000	0x4001_0FFF	ADC	
0x4001_1000	0x4002_1FFF	Reserved	
0x4002_2000	0x4002_2FFF	AFIO	
0x4002_3000	0x4002_3FFF	Reserved	
0x4002_4000	0x4002_4FFF	EXTI	
0x4002_5000	0x4002_BFFF	Reserved	
0x4002_C000	0x4002_CFFF	MCTM	
0x4002_D000	0x4003_0FFF	Reserved	
0x4003_1000	0x4003_1FFF	PWM0	
0x4003_2000	0x4004_0FFF	Reserved	
0x4004_1000	0x4004_1FFF	UART1	
0x4004_2000	0x4004_3FFF	Reserved	APB
0x4004_4000	0x4004_4FFF	SPI1	
0x4004_5000	0x4004_7FFF	Reserved	
0x4004_8000	0x4004_8FFF	I^2C0	
0x4004_9000	0x4004_9FFF	I^2C1	
0x4004_A000	0x4006_7FFF	Reserved	
0x4006_8000	0x4006_8FFF	WDT	
0x4006_9000	0x4006_9FFF	Reserved	
0x4006_A000	0x4006_AFFF	RTC & PWRCU	
0x4006_B000	0x4006_DFFF	Reserved	
0x4006_E000	0x4006_EFFF	GPTM	
0x4006_F000	0x4007_0FFF	Reserved	
0x4007_1000	0x4007_1FFF	PWM1	
0x4007_2000	0x4007_5FFF	Reserved	
0x4007_6000	0x4007_6FFF	BFTM0	
0x4007_7000	0x4007_7FFF	BFTM1	
0x4007_8000	0x4007_FFFF	Reserved	

Start Address	End Address	Peripheral	Bus
0x4008_0000	0x4008_1FFF	FMC	AHB
0x4008_2000	0x4008_7FFF	Reserved	
0x4008_8000	0x4008_9FFF	CKCU/RSTCU	
0x4008_A000	0x4008_BFFF	CRC	
0x4008_C000	0x400A_FFFF	Reserved	
0x400B_0000	0x400B_1FFF	GPIOA	
0x400B_2000	0x400B_3FFF	GPIOB	
0x400B_4000	0x400B_5FFF	GPIOC	
0x400B_6000	0x400C_9FFF	Reserved	
0x400C_A000	0x400C_BFFF	DIV	
0x400C_C000	0x400F_FFFF	Reserved	

Clock Structure

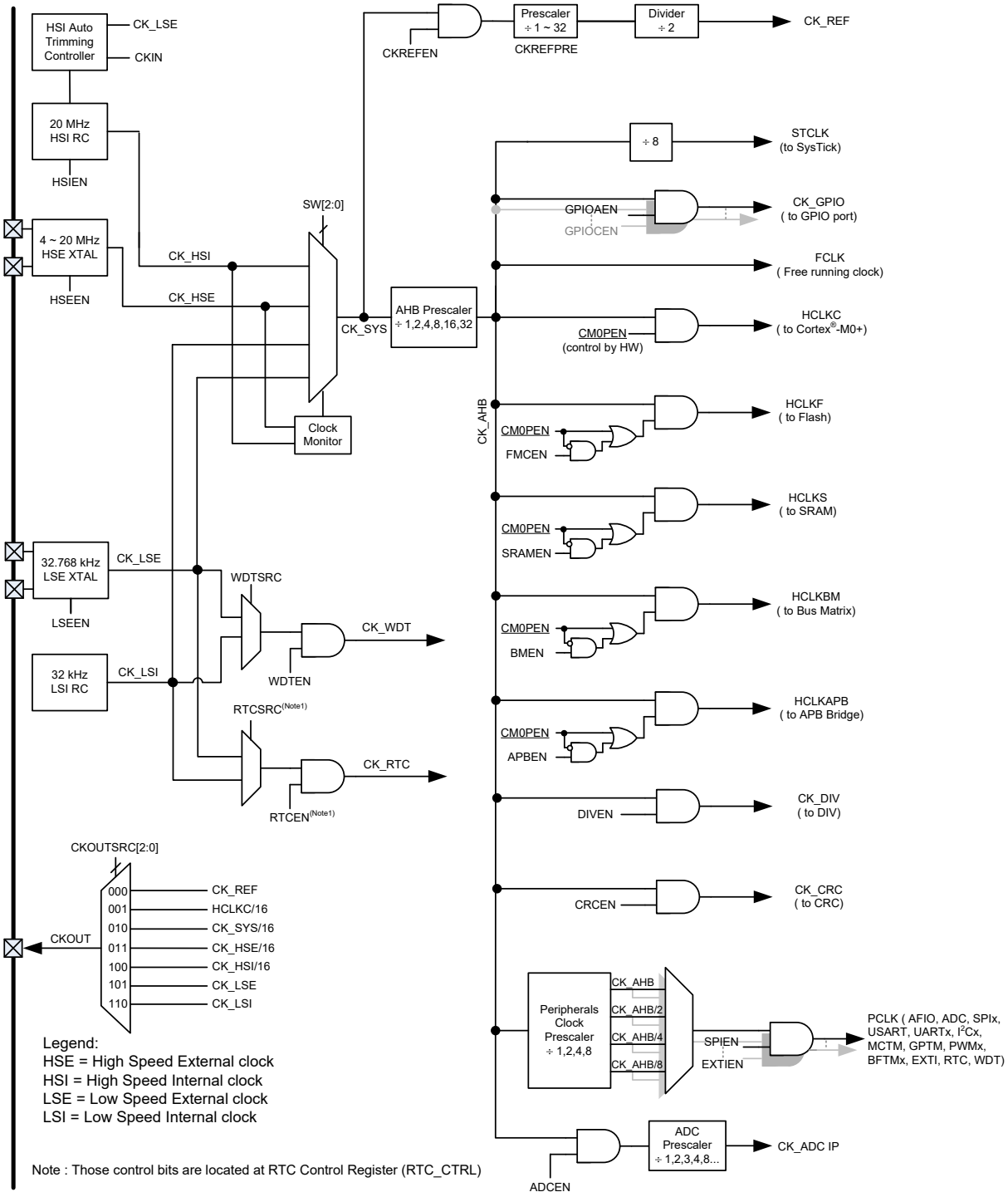


Figure 3. Clock Structure

4 24-Bit Delta Sigma A/D Converter – ΔΣ ADC

The device contains a high accuracy multi-channel 24-bit Delta Sigma type analog-to-digital converter which can directly interface to external analog signals, such as that from sensors or other control signals and convert these signals directly into a 24-bit digital value. In addition to the core analog to digital converter circuitry, the A/D converter module also includes an internal Programmable Gain Amplifier PGA. The PGA gain control, ADC gain control and ADC reference gain control determine the overall amplification gain for ADC input signal, giving users a flexible way of setting up an overall gain to achieve an optimum amplification of the input signal for their specific applications. The converter has a total of four inputs allowing the formation of two differential input channels. The converter output is filtered via a SINC filter and the result stored as a 24-bit value in three data registers. An internal voltage regulator and reference sources are also included as well as a temperature sensor for A/D converter compensation due to temperature effects.

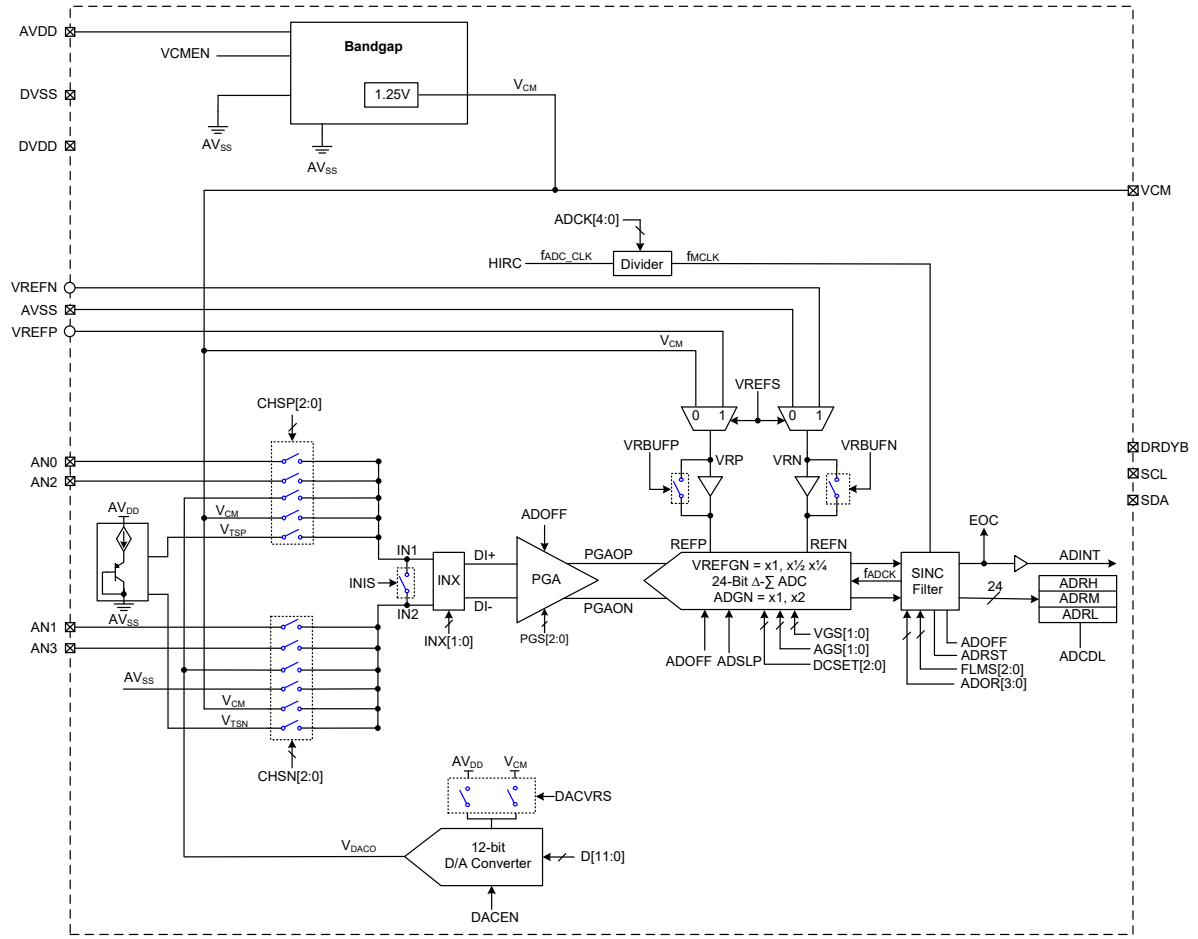


Figure 4. 24-bit A/D Converter Block Diagram

24-Bit A/D Converter Internal Registers

The 24-bit A/D converter is setup and operated using a series of internal registers. Device commands and data are written to and read from the 24-bit ADC module using its internal I^2C bus. This list provides a summary of all the 24-bit ADC module internal registers, their detailed operation is described under their relevant section in the functional description.

Register Initial Values

The following table shows the internal value of the individual register after a power on reset.

Register	Power On Reset Value
PWRC	0000 0000
PGAC0	-000 0000
PGAC1	-000 000-
PGACS	--00 0000
ADRL	xxxx xxxx
ADRM	xxxx xxxx
ADRH	xxxx xxxx
ADCR0	0010 0000
ADCR1	0000 000-
ADCS	---0 0000
ADCTE	1110 0100
DAH	0000 0000
DAL	---- 0000
DACC	00-- ----
SIMC0	0--- 00--
SIMTOC	0000 0000
HIRCC	---- -001

Table Legend

Item	Description
*	Warm reset
-	Not implemented
u	Unchanged
x	Unknown

Address	Register Name	Bit							
		7	6	5	4	3	2	1	0
00H	PWRC	VCMEN	D6	D5	D4	D3	D2	D1	D0
01H	PGAC0	—	VGS1	VGS0	AGS1	AGS0	PGS2	PGS1	PGS0
02H	PGAC1	—	INIS	INX1	INX0	DCSET2	DCSET1	DCSET0	—
03H	PGACS	—	—	CHSN2	CHSN1	CHSN0	CHSP2	CHSP1	CHSP0
04H	ADRL	D7	D6	D5	D4	D3	D2	D1	D0
05H	ADRM	D15	D14	D13	D12	D11	D10	D9	D8
06H	ADRH	D23	D22	D21	D20	D20	D19	D18	D17
07H	ADCR0	ADRST	ADSLP	ADOFF	ADOR3	ADOR2	ADOR1	ADOR0	VREFS
08H	ADCR1	FLMS2	FLMS1	FLMS0	VRBUFN	VRBUFP	ADCDL	EOC	—
09H	ADCS	—	—	—	ADCK4	ADCK3	ADCK2	ADCK1	ADCK0

Address	Register Name	Bit							
		7	6	5	4	3	2	1	0
0AH	ADCTE	D7	D6	D5	D4	D3	D2	D1	D0
0BH	DAH	D11	D10	D9	D8	D7	D6	D5	D4
0CH	DAL	—	—	—	—	D3	D2	D1	D0
0DH	DACC	DACEN	DACVRS	—	—	—	—	—	—
0EH	SIMC0	SIMS	—	—	—	SIMDEB1	SIMDEB0	—	—
10H	SIMTOC	SIMTOEN	SIMTOF	SIMTOS5	SIMTOS4	SIMTOS3	SIMTOS2	SIMTOS1	SIMTOS0
11H	HIRCC	—	—	—	—	—	HIRCO	HIRCF	HIRCEN
12H	Reserved, cannot be changed								

Internal Power Supply

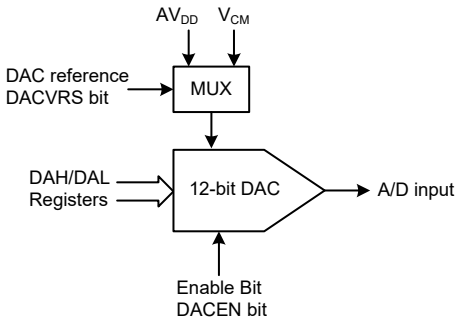
This 24-bit A/D Converter contains the VCM for the regulated power supply. The VCM can be used as the reference voltage for this 24-bit ADC module. The VCM function is controlled by the VCMEN bit and can be powered off to reduce the power consumption.

Reference Voltages

An internal voltage reference source, known as the VCM, is used as a converter reference. The VCM is sourced from a bandgap reference generator thus providing a temperature stable reference and has a output voltage level fixed at 1.25V. The VCM function is controlled by the VCMEN bit and can be switched off to reduce the power consumption.

The converter reference voltage range is supplied on two external reference pins, VREFP and VREFN. These offer a full reference voltage range of AV_{SS} to AV_{DD}. This externally supplied reference voltage can be attenuated by 0.5 or 0.25 using the VREFGN bits in the PGAC0 register.

An internal DAC is also provided as an additional reference voltage source. The DAC has two reference voltages which define the maximum value, supplied by either AV_{DD} or V_{CM}. The DAC 12-bit value is setup using two data registers, DAL and DAH and selected using the DACVRS bit in the DACC register. The overall enable bit for the DAC is the DACEN bit in the DACC register.



• **DAH Register – 0BH**

Bit	7	6	5	4	3	2	1	0
Name	D11	D10	D9	D8	D7	D6	D5	D4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 **D11~D4**: DAC output control code

• **DAL Register – 0CH**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	D3	D2	D1	D0
R/W	—	—	—	—	R/W	R/W	R/W	R/W
POR	—	—	—	—	0	0	0	0

Bit 7~4 Unimplemented, read as "0"

Bit 3~0 **D3~D0**: DAC output control code

Note: Writing to this register only writes to a shadow buffer. Not until data is written to the DAH register will the actual data be written into the DAL register.

• **DACC Register – 0DH**

Bit	7	6	5	4	3	2	1	0
Name	DACEN	DACVRS	—	—	—	—	—	—
R/W	R/W	R/W	—	—	—	—	—	—
POR	0	0	—	—	—	—	—	—

Bit 7 **DACEN**: DAC enable or disable control bit
0: Disable
1: Enable

Bit 6 **DACVRS**: DAC reference voltage selection
0: DAC reference voltage sourced from AV_{DD}
1: DAC reference voltage sourced from V_{CM}

Bit 5~0 Unimplemented, read as "0"

Power and Reference Control

The following table shows the overall control of the power and voltage sources.

Register Bits		Output Voltage	
ADOFF	VCMEN	Bandgap	VCM
1	0	Off	Disable
1	1	On	Enable
0	0	On	Disable
0	1	On	Enable

Power Control Table

Power Control Registers

• **PWRC Register – 00H**

Bit	7	6	5	4	3	2	1	0
Name	VCMEN	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **VCMEN**: VCM function enable control
0: Disable
1: Enable
If the VCM is disabled, there will be no power consumption and VCM output pin is floating.

Bit 6~0 **D6~D0**: Performance optimizing bits
010_1000B: when ADCR1[FLMS2 ~ 0] = 000B ($f_{ADCK} = f_{MCLK}/30$)
011_1100B: when ADCR1[FLMS2 ~ 0] = 010B ($f_{ADCK} = f_{MCLK}/12$)
Others: Reserved

Oscillator

There is an internal HIRC oscillator in the 24-bit A/D converter module, which can provide the required A/D conversion clock source of 4.9152 MHz.

Oscillator Control Register

There is a control register for the 24-bit A/D Converter internal oscillator. Note that a full 16 clock cycle time is required for the internal HIRC oscillator to stabilise.

• **HIRCC Register – 11H**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	HIRCO	HIRCF	HIRCEN
R/W	—	—	—	—	—	R/W	R	R/W
POR	—	—	—	—	—	0	0	1

Bit 7~3 Unimplemented, read as "0"

Bit 2 **HIRCO**: HIRC clock output
This bit must be reserved at "0"

Bit 1 **HIRCF**: HIRC oscillator stable flag
0: Unstable
1: Stable
The HIRC stable time will spend 16 clocks when HIRCEN is enabled.

Bit 0 **HIRCEN**: HIRC oscillator enable control
0: Disable
1: Enable

Input Signal Gain Control Amplifier – PGA

An internal programmable gain amplifier is provided to amplify the differential input signal before being converted. All input signals to the 24-bit analog to digital converter must pass through the PGA. This pre-processing of the input signal enables an optimal signal range to be setup to obtain a converted value with optimal resolution.

PGA Registers

The PGA is controlled using a series of registers to setup the gain value and also to select the input source.

- **PGAC0 Register – 01H**

Bit	7	6	5	4	3	2	1	0
Name	—	VGS1	VGS0	AGS1	AGS0	PGS2	PGS1	PGS0
R/W	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	0	0	0	0	0	0	0

Bit 7 Unimplemented, read as "0"

Bit 6~5 **VGS1~VGS0**: REFP/REFN differential reference voltage gain selection
00: VREFGN = 1
01: VREFGN = 1/2
10: VREFGN = 1/4
11: Reserved

Bit 4~3 **AGS1~AGS0**: ADC converter PGAOP/PGAON differential input signal gain selection
00: ADGN = 1
01: ADGN = 2 (for Gain = 128 = PGAGN × ADGN = 64 × 2)
10: Reserved
11: Reserved

Bit 2~0 **PGS2~PGS0**: PGA DI+/DI- differential channel input gain selection
000: PGAGN = 1
001: PGAGN = 2
010: PGAGN = 4
011: PGAGN = 8
100: PGAGN = 16
101: PGAGN = 32
110: PGAGN = 64
111: Reserved

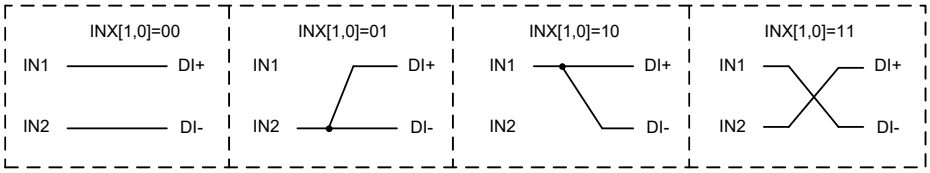
- **PGAC1 Register – 02H**

Bit	7	6	5	4	3	2	1	0
Name	—	INIS	INX1	INX0	DCSET2	DCSET1	DCSET0	—
R/W	—	R/W	R/W	R/W	R/W	R/W	R/W	—
POR	—	0	0	0	0	0	0	—

Bit 7 Unimplemented, read as "0".

Bit 6 **INIS**: Selected input terminals IN1/IN2 internal connection
0: Not connected
1: Connected

Bit 5~4 **INX1, INX0**: The selected input ends, IN1/IN2 and the PGA differential input ends, DI+/DI- connection control bits



Bit 3~1 **DCSET2~DCSET0**: Differential input signal PGAOP/PGAON offset selection

000: DCSET = +0V
001: DCSET = +0.25 × ΔVR_I
010: DCSET = +0.5 × ΔVR_I
011: DCSET = +0.75 × ΔVR_I
100: DCSET = +0V
101: DCSET = -0.25 × ΔVR_I
110: DCSET = -0.5 × ΔVR_I
111: DCSET = -0.75 × ΔVR_I

The voltage, ΔVR_I, is the differential reference voltage which is amplified by the specific gain selection based on the selected inputs.

Bit 0 Unimplemented, read as "0"

PGA Input Channel Selection

In addition to the external analog input to be measured by the converter, there are several other internal analog voltage lines which can be connected to the converter. These come from a range of sources such as the temperature sensor and are normally used for calibration purposes.

- **PGACS Register − 03H**

Bit	7	6	5	4	3	2	1	0
Name	—	—	CHSN2	CHSN1	CHSN0	CHSP2	CHSP1	CHSP0
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	—	0	0	0	0	0	0

Bit 7~6 Unimplemented, read as "0"

Bit 5~3 **CHSN2~CHSN0**: PGA negative input end IN2 selection

000: AN1
001: AN3
010: Reserved
011: Reserved
100: V_{DACO}
101: AV_{SS}
110: V_{CM}
111: V_{TSN} – Temperature sensor negative output

These bits are used to select the negative input, IN2. If the IN2 input is selected as a single end input, the V_{CM} voltage must be selected as the positive input on IN1 for single end input applications. It is recommended that when the V_{TSN} signal is selected as the negative input, the V_{TSP} signal should be selected as the positive input for proper operations.

Bit 2~0 **CHSP2~CHSP0**: Positive input end IN1 selection
000: AN0
001: AN2
010: Reserved
011: Reserved
100: V_{DACO}
101: Reserved
110: V_{CM}
111: V_{TSP} – Temperature sensor positive output
These bits are used to select the positive input, IN1. If the IN1 input is selected as a single end input, the V_{CM} voltage must be selected as the negative input on IN2 for single end input applications. It is recommended that when the V_{TSP} signal is selected as the positive input, the V_{TSN} signal should be selected as the negative input for proper operations.

24-Bit Analog to Digital Converter Operation

The 24-bit analog to digital converter received a differential analog signal from the PGA output and converts in using a Delta Sigma converter into a 24-bit digital value. The overall operation of the converter is controlled by a series of control registers.

- **ADCR0 Register − 07H**

Bit	7	6	5	4	3	2	1	0
Name	ADRST	ADSLP	ADOFF	ADOR3	ADOR2	ADOR1	ADOR0	VREFS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	1	0	0	0	0	0

Bit 7 **ADRST**: A/D converter software reset enable control
0: Disable
1: Enable
This bit is used to reset the A/D converter internal digital SINC filter. This bit is set low for A/D normal operations. However, if set high, the internal digital SINC filter will be reset and the current A/D converted data will be aborted. A new A/D data conversion process will not be initiated until this bit is set low again.

Bit 6 **ADSLP**: A/D converter sleep mode enable control
0: Normal mode
1: Sleep mode
This bit is used to determine whether the A/D converter enters the sleep mode or not when the A/D converter is powered on by setting the ADOFF bit low. When the A/D converter is powered on and the ADSLP bit is low, the A/D converter will operate normally. However, the A/D converter will enter the sleep mode if the ADSLP bit is set high as the A/D converter has been powered on. The whole A/D converter circuit will be switched off except the PGA and internal Bandgap circuit to reduce the power consumption and VCM start-up stable time.

Bit 5 **ADOFF**: A/D converter module power on/off control
0: Power on
1: Power off

This bit controls the power of the A/D converter module. This bit should be cleared to zero to enable the A/D converter. If the bit is set high then the A/D converter will be switched off reducing the device power consumption. As the A/D converter will consume a limited amount of power, even when not executing a conversion, this may be an important consideration in power sensitive battery powered applications.

Setting the ADOFF bit high will power down the A/D converter module regardless of the ADSLP and ADRST bit settings.

Bit 4~1 **ADOR3~ADOR0**: A/D conversion oversampling rate selection
0000: Oversampling rate OSR = 32768
0001: Oversampling rate OSR = 16384
0010: Oversampling rate OSR = 8192
0011: Oversampling rate OSR = 4096
0100: Oversampling rate OSR = 2048
0101: Oversampling rate OSR = 1024
0110: Oversampling rate OSR = 512
0111: Oversampling rate OSR = 256
1000: Oversampling rate OSR = 128
Others: Reserved

Bit 0 **VREFS**: A/D converter reference voltage pair selection
0: Internal reference voltage pair – V_{CM} & AV_{SS}
1: External reference voltage pair – V_{REFP} & V_{REFN}

- **ADCR1 Register – 08H**

Bit	7	6	5	4	3	2	1	0
Name	FLMS2	FLMS1	FLMS0	VRBUFN	VRBUFP	ADCDL	EOC	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—
POR	0	0	0	0	0	0	0	—

Bit 7~5 **FLMS2~FLMS0**: A/D converter clock divided ratio selection
000: $f_{ADCK} = f_{MCLK}/30$, N = 30
010: $f_{ADCK} = f_{MCLK}/12$, N = 12
Others: Reserved

Bit 4 **VRBUFN**: A/D converter negative reference voltage input (VRN) buffer control
0: Disable input buffer and enable bypass function
1: Enable input buffer and disable bypass function

Bit 3 **VRBUFP**: A/D converter positive reference voltage input (VRP) buffer control
0: Disable input buffer and enable bypass function
1: Enable input buffer and disable bypass function

Bit 2 **ADCDL**: A/D converted data latch function enable control
0: A/D converted data updated
1: A/D converted data not updated

If the A/D converted data latch function is enabled, the latest converted data value will be latched and not be updated by any subsequent converted results until this function is disabled. Although the converted data is latched into the data registers, the A/D converter circuits remain operational and EOC flag will not change state. It is recommended that this bit should be set high before reading the converted data in the ADRL, ADRM and ADRH registers. After the converted data has been read out, the bit can then be cleared to zero to disable the A/D converter data latch function and allow further conversion values to be stored. In this way, the possibility of

obtaining undesired data during A/D converter conversions can be prevented.

Bit 1 **EOC**: End of A/D conversion flag
0: A/D conversion in progress
1: A/D conversion ended
This flag will be automatically set high by the hardware when a conversion process has completed but must be cleared by the application software.

Bit 0 Unimplemented, read as "0"

A/D Data Rate Definition

The Delta Sigma ADC data rate can be calculated by the equation list below.

Data Rate = f_{ADCK} / OSR

= (f_{MCLK}/N) / OSR

= f_{MCLK} / (N × OSR)

f_{ADCK}: f_{MCLK}/N

f_{MCLK}: f_{ADC_CLK} or f_{ADC_CLK}/2/(ADCK + 1) using the ADCK bit field.

N: 30 or 12 determined by the FLMS bit field.

OSR: Oversampling rate determined by the ADOR field.

For example; if a data rate of 10Hz is desired. An f_{MCLK} clock source with a frequency of 4.9152 MHz ADC can be selected. Then set the FLMS field to “000” to obtain an “N” equal to 30. Finally, set the ADOR field to “0001” to select an oversampling rate equal to 16384. Therefore, the Data Rate = 4.9152 MHz / (30 × 16384) = 10 Hz.

Note that the A/D converter has a notch rejection function for an AC power supply with a frequency of 50 Hz or 60 Hz when the data rate is equal to 10Hz.

A/D Converter Clock Source

The clock source for the A/D converter should be typically fixed at a value of 4.9152 MHz, which originates from the 24-bit ADC clock f_{ADC_CLK}. This can be chosen to be either f_{ADC_CLK} or a subdivision of f_{ADC_CLK}. The division ratio value is determined by the ADCK4 ~ ADCK0 bits in the ADCS register to obtain a 4.9152 MHz clock source for the ADC.

Internal OSC = 4.9152 MHz, f_{ADCK} = f_{MCLK}/30.

Data Rate (Hz)	ADCK4 ~ 0	ADOR3 ~ 0	FLMS2 ~ 0
10	11111	0001	000

Internal OSC = 4.9152 MHz, f_{ADCK} = f_{MCLK}/12.

Data Rate (Hz)	ADCK4 ~ 0	ADOR3 ~ 0	FLMS2 ~ 0
25	11111	0001	010

• **ADCS Register – 09H**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	ADCK4	ADCK3	ADCK2	ADCK1	ADCK0
R/W	—	—	—	R/W	R/W	R/W	R/W	R/W
POR	—	—	—	0	0	0	0	0

Bit 7~5 Unimplemented, read as "0"

Bit 4~0 **ADCK4~ADCK0**: 24-bit A/D converter clock source f_{MCLK} divided ratio selection
00000~11110: $f_{MCLK} = f_{ADC\_CLK}/2/(ADCK[4:0] + 1)$
11111: $f_{MCLK} = f_{ADC\_CLK}$

• **ADCTE Register – 0AH**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	1	1	1	0	0	1	0	0

Bit 7~0 Reserved bits, should be fixed as 1110_0111B.

A/D Operating Modes

The 24-bit A/D Converter has four operating modes, which are the Normal mode, Power down mode, Sleep mode and Reset mode. These modes are controlled by a combination of the ADOFF, ADSLP and ADRST bits in the ADCR0 register as shown in the accompanying table. The ADOFF controls the overall on/off condition and if high will power down the A/D converter to reduce power. When the ADOFF bit is low, the converter will be powered on and the ADSLP bit will determine if the converter is in the normal operating mode or in the sleep mode.

ADOFF	ADSLP	ADRST	Operating Mode	Description
1	x	x	Power down mode	Bandgap off, PGA off, ADC off, Temperature sensor off, VRN/VRP buffer off, SINC filter off
0	1	x	Sleep mode	Bandgap on, PGA on, ADC off, Temperature sensor off, VRN/VRP buffer off, SINC filter on
0	0	0	Normal mode	Bandgap on, PGA on, ADC on, Temperature sensor on/off, VRN/VRP buffer on/off, SINC filter on
0	0	1	Reset mode	Bandgap on, PGA on, ADC on, Temperature sensor on/off, VRN/VRP buffer on/off, SINC filter Reset

"x" unknown

A/D Operating Mode Summary

Note: 1. The VCM generator can be switched on or off by configuring the VCMEN bit.
2. The Temperature sensor can be switched on or off by configuring the CHSN[2:0] or CHSP[2:0] bits.
3. The VRN buffer can be switched on or off by configuring the VRBUFN bit while the VRP buffer can be switched on or off by configuring the VRBUFP bit.

A/D Conversion Process

To enable the A/D Converter, the first step is to disable the ADC power down and sleep mode by clearing the ADOFF and ADSLP bits to make sure the A/D Converter is powered up. The ADRST bit in the ADCR0 register is used to start and reset the A/D converter after power on. To set

ADRST bit from low to high and then low again, an analog to digital converted data in SINC filter will be initiated. After this setup is complete, the A/D Converter is ready for operation. These three bits are used to control the overall start operation of the internal analog to digital converter.

The EOC bit in the ADCR1 register is used to indicate when the analog to digital conversion process is complete. This bit will be automatically set to "1" by the Hardware after a conversion cycle has ended. The ADC converted data will be updated continuously by new converted data. If the ADC converted data latch function is enabled, the latest converted data will be latched and the following new converted data will be discarded until this data latch function is disabled.

The differential reference voltage supply to the A/D Converter can be supplied from either the internal power supply, V_{CM} and AV_{SS}, or from an external reference source supplied on pins VREFP and VREFN. The desired selection is made using the VREFS bit in the ADCR0 register.

Summary of A/D conversion steps

- Step 1
  Enable the power VCM for PGA and ADC.
- Step 2
  Select the PGA, ADC, reference voltage gains by PGAC0 register.
- Step 3
  Select the PGA settings for input connection, VCM voltage level and buffer option by PGAC1 register.
- Step 4
  Select the required A/D conversion clock source 4.9152 MHz by correctly programming bits ADCK4 ~ ADCK0 in the ADCS register.
- Step 5
  Select output data rate by cofiguring the ADOR[2:0] bits in the ADCR0 register and FLMS[2:0] bits in the ADCR1 register.
- Step 6
  Select which channel is to be connected to the internal PGA by correctly programming the CHSP2 ~ CHSP0 and CHSN2 ~ CHSN0 bits which are also contained in the PGACS register.
- Step 7
  Release the power down mode and sleep mode by clearing the ADOFF and ADSLP bits in ADCR0 register.
- Step 8
  Reset the A/D by setting the ADRST to high in the ADCR0 register and clearing this bit to zero to release reset status.
- Step 9
  To check when the analog to digital conversion process is complete, the EOC bit in the ADCR1 register can be polled. The conversion process is complete when this bit goes high. When this occurs the A/D data registers ADRL, ADRM and ADRH can then be read to obtain the conversion value.

A/D Transfer Function

As the converted value is 24-bits its full-scale converted digitised value has a decimal value of 8388607 to -8388608. The converted data format is formed by a two's complement binary value. The MSB of the converted data is the signed bit. Since the full-scale analog input value is equal to the amplified value of the VCM or differential reference input voltage, ΔVR_I, selected by the VREFS bit in ADCR0 register, this gives a single bit analog input value of ΔVR_I divided by 8388608.

1 LSB = ΔVR_I/8388608

The A/D Converter input voltage value can be calculated using the following equation:

ΔSI_I = (PGAGN × ADGN × ΔDI±) + DCSET

ΔVR_I = VREFGN × ΔVR ±

ADC_Conversion_Data = (ΔSI_I / ΔVR_I) × K

Where K is equal to 2^{23}.

Notes: 1. The PGAGN, ADGN, VREFGN values are determined by the PGS, AGS, VGS control bits.

2. ΔSI_I is the differential input signal after amplification and offset adjustment

3. PGAGN: Programmable Gain Amplifier gain

4. ADGN: A/D Converter gain

5. VREFGN: Reference voltage gain

6. ΔDI±: Differential input signal derived from external channels or internal signals

7. DCSET: Offset voltage

8. ΔVR±: Differential reference voltage

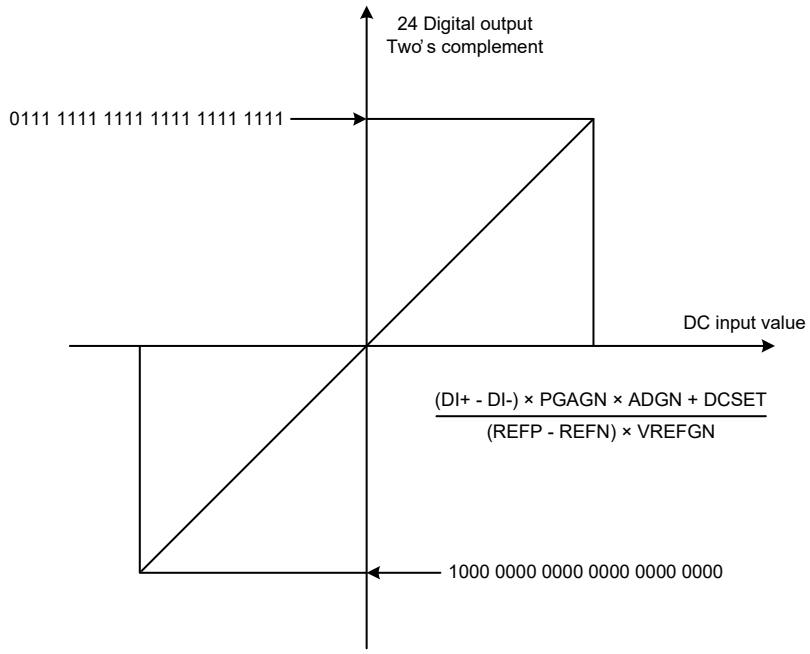
9. ΔVR_I: Differential reference input voltage after amplification

Due to the digital system design of the converter, the maximum A/D converted value is 8388607 and the minimum value is -8388608, therefore the centre value is 0. The ADC_Conversion_Data equation illustrates this range of converted data variation.

Converted Data 2's Compliment Hex Value	Decimal Value
0x7FFFFF	8388607
0x800000	-8388608

A/D Conversion Data Range

The following diagram shows the relationship between the DC input value and the ADC converted data which is presented in Two's Complement format.



A/D Converted Data

The 24-bit A/D converter data is stored in three individual registers, ADRL, ADRM and ADRH. The converted data is related to the input voltage and the PGA selection setup and is generated in a two's complement binary code formal. The length of this output code is 24 bits and the MSB is a signed bit. When the MSB is "0", this indicates that the input is "positive", while if the MSB is "1", this indicates that the input is "negative". The maximum value is 8388607 and the minimum value is -8388608. If the input signal exceeds the maximum value, the converted data is limited to 8388607, and if the input signal is less than the minimum value, the converted data is limited to -8388608.

- **ADRL Register − 04H**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	R	R	R	R	R	R	R
POR	x	x	x	x	x	x	x	x

Bit 7~0 A/D conversion data register bit 7~bit 0

- **ADRM Register − 05H**

Bit	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8
R/W	R	R	R	R	R	R	R	R
POR	x	x	x	x	x	x	x	x

Bit 7~0 A/D conversion data register bit 15~bit 8

• **ADRH Register − 06H**

Bit	7	6	5	4	3	2	1	0
Name	D23	D22	D21	D20	D19	D18	D17	D16
R/W	R	R	R	R	R	R	R	R
POR	x	x	x	x	x	x	x	x

Bit 7~0 A/D conversion data register bit 23~bit 16

Converting the Digital Value to a Voltage

The analog voltage value can be recovered using the following equations:

If the MSB = 0 for positive value converted data:

$$\text{Input Voltage} = \frac{(\text{Converted\_data}) \times \text{LSB} - \text{DCSET}}{\text{PGAGN} \times \text{ADGN}}$$

If the MSB = 1for negative converted data:

$$\text{Input voltage} = \frac{(\text{Two's\_complement\_of\_Converted\_data}) \times \text{LSB} - \text{DCSET}}{\text{PGAGN} \times \text{ADGN}}$$

Note: Two's complement = One's complement + 1

Temperature Sensor

The 24-bit A/D converter module includes a fully internal temperature sensor to allow for compensation due to temperature effects. By selecting the PGA input channels to V_{TSN} and V_{TSN} signals, the A/D Converter can obtain temperature information and then use the result to compensate the A/D converted data to minimise the effects of temperature.

Effective Number of Bits – ENOB

Although the analog to digital converter is a 24-bit type various factors such as the PGA gain and the data rate affect the actual number of effective number of converted bits.

Programming Considerations

During microcontroller operations where the A/D converter is not being used, the A/D internal circuitry can be switched off to reduce power consumption, by setting bit ADOFF high in the ADCR0 register. When this happens, the internal A/D converter circuits will not consume power irrespective of what analog voltage is applied to their input lines.

When writing to the DAC registers, DAH and DAL, note that this must be carried out in a special sequence. This is because when writing to the DAL register, the data is only written into a shadow buffer register. Only when data is written to the DAH register will data in the shadow buffer be transferred to the DAL register. Therefore when writing data to the DAC registers first write data to the DAL register and then to the DAH register.

External Interface Communication

The 24-bit A/D converter communicates with external hardware using its internal I^2C interface. Originally developed by Philips, the I^2C interface is a two line low speed serial interface for synchronous serial data transfer. With the advantage of only two lines for communication, a

relatively simple communication protocol and the ability to accommodate multiple devices on the same bus has made it an extremely popular interface type for many applications.

I²C Interface Operation

The I²C serial interface is a two line interface, a serial data line, SDA, and serial clock line, SCL. As many devices may be connected together on the same bus, their outputs are both open drain types. For this reason it is necessary that external pull-high resistors are connected to these outputs. Note that no chip select line exists, as each device on the I²C bus is identified by a unique address which will be transmitted and received on the I²C bus. When two devices communicate with each other on the bidirectional I²C bus, one is known as the master device and one as the slave device. Both master and slave can transmit and receive data, however, it is the master device that has overall control of the bus, and it is only the master that will drive the SCL clock line. This 24-bit ADC module only operates in the slave mode, and will therefore only operate in response to the master. There are two methods for this 24-bit ADC module to transfer data on the I²C bus, the slave transmit mode and the slave receive mode.

Several registers control the overall operation of the I²C bus interface.

I²C Address and Register Write/Read

I²C Address Selection

As this 24-bit ADC module only operates as a slave, and as it may be connected to a common I²C bus along with other I²C devices, it will require a specific address for it to be communicated to by the master. The address of 24-bit ADC module is fixed at 0xD0.

- **SIMC0 Register – 0EH**

Bit	7	6	5	4	3	2	1	0
Name	SIMS	—	—	—	SIMDEB1	SIMDEB0	—	—
R/W	R/W	—	—	—	R/W	R/W	—	—
POR	0	—	—	—	0	0	—	—

Bit 7 **SIMS**:
0: Normal operation
1: Results in unpredictable behavior
This bit must be kept at a zero value for normal operation

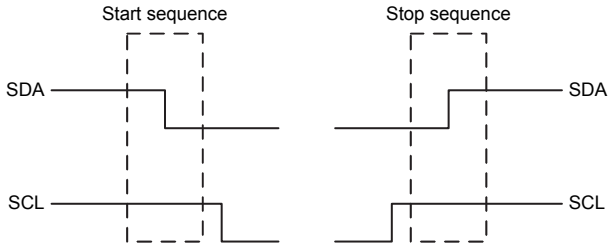
Bit 6~4 Unimplemented, read as "0"

Bit 3~2 **SIMDEB1~SIMDEB0**: I²C debounce time selection
00: No debounce
01: 2 ADC clock debounce
10: 4 ADC clock debounce
11: 4 ADC clock debounce

Bit 1~0 Unimplemented, read as "0"

Start and Stop Operations

Normally the SDA line can only change when the SCL line is low. There are two exceptions however and that is for the Start and Stop operations, where the SCL line will be forced high by the master and the SDA line will change sate. As the diagram shows when the SCL line is high, a high to low SDA line transition indicates a start operation and a low to high SDA line transition indicates a stop operation.



I²C Bus Data Transfer

Data is transferred on the I²C bus in 8 bit packets, first transmitting the MSB which is the most significant bit and lastly the LSB bit, the least significant bit. When the data has been setup on the SDA line, the SCL line then generates a high pulse to latch the data. When the SCL line is high the SDA line is not permitted to change state. After 8-bits have been transmitted, the device will then send a 9th bit which is the acknowledge bit. Therefore in total there are 9 bits transmitted and subsequently 9 SCL clock pulses to transfer each 8-bits or byte of data. When the receiving device sends back a low ACK bit, this is to acknowledge that it has received the 8-bits of data and is ready to receive another byte. If a high ACK bit is sent back, this indicates that it is unable to receive any further data and the master should then send a stop sequence.

- **I²C Register Write/Read**

Write Process

Bit	7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0		
Start	Device Address							Write	ACK	Register Address								ACK	Register Data								ACK	Stop

Read Process

Bit	7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0			7	6	5	4	3	2	1	0			7	6	5	4	3	2	1	0		
Start	Device Address							Write	ACK	Register Address								ACK	Start	Device Address							Read	ACK	Register Data								ACK	Stop

I²C Bus Start Signal

The START signal can only be generated by the master device connected to the I²C bus and not by the slave device. This START signal will be detected by all devices connected to the I²C bus. A START condition occurs when a high to low transition on the SDA line takes place when the SCL line remains high.

Slave Address

The transmission of a START signal by the master will be detected by all devices on the I²C bus. To determine which slave device the master wishes to communicate with, the address of the slave device will be sent out immediately following the START signal.

I²C Bus Slave Address Acknowledge Signal

After the master has transmitted a calling address, any slave device on the I²C bus, whose own internal address matches the calling address, must generate an acknowledge signal. The acknowledge signal will inform the master that a slave device has accepted its calling address. If no acknowledge signal is received by the master then a STOP signal must be transmitted by the master to end the communication.

I²C Bus Data and Acknowledge Signal

The transmitted data is 8-bits wide and is transmitted after the slave device has acknowledged receipt of its slave address. The order of serial bit transmission is the MSB first and the LSB last. After receipt of 8-bits of data, the receiver must transmit an acknowledge signal, level 0, before it can receive the next data byte. If the slave transmitter does not receive an acknowledge bit signal from the master receiver, then the slave transmitter will release the SDA line to allow the master to send a STOP signal to release the I²C Bus.

I²C Timeout Function

The I²C interface includes a timeout function which is controlled by a single register. This register sets the overall enable/disable function as well as the timeout value in ADC clock units. Determining whether the I²C bus has timed out is implemented by reading the SIMTOF bit. This bit will be automatically set high when the I²C bus times out, but needs to be cleared manually by the application program.

- **SIMTOC Register − 10H**

Bit	7	6	5	4	3	2	1	0
Name	SIMTOEN	SIMTOF	SIMTOS5	SIMTOS4	SIMTOS3	SIMTOS2	SIMTOS1	SIMTOS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **SIMTOEN**: I²C time-out control
0: Disable
1: Enable

Bit 6 **SIMTOF**: I²C time-out flag
0: Not occurred
1: Occurred
The bit is set by time-out function and is cleared by the application program.

Bit 5~0 **SIMTOS5~SIMTOS0**: I²C time-out selection time
The I²C Time-Out clock source is $f_{ADC\_CLK}/32$. ($f_{SUB} = f_{ADC\_CLK}/128$)
The I²C Time-Out time is ([SIMTOS5:SIMTOS0] + 1) × ($32/f_{SUB}$)

5 Pin Assignment

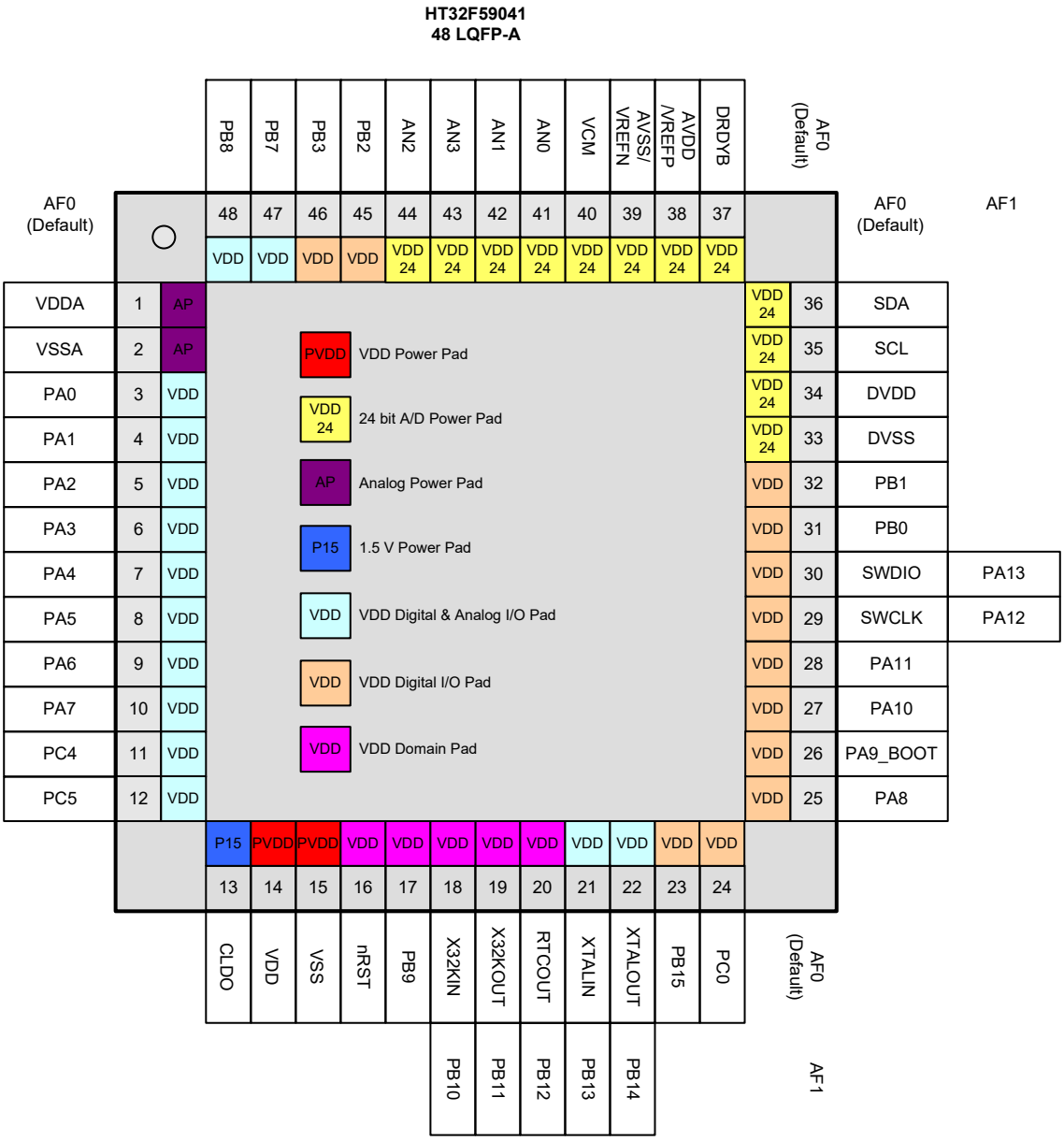


Figure 5. 48-pin LQFP Pin Assignment

Table 3. Pin Assignment

Package	Alternate Function Mapping															
	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
48LQFP	System Default	GPIO	ADC	N/A	MCTM /GPTM	SPI	USART /UART	I²C	N/A	N/A	N/A	N/A	N/A	PWM	N/A	System Other
1	VDDA															
2	VSSA															
3	PA0		ADC_IN2		GT_CH0	SPI1_SCK	USR_RTS	I2C1_SCL								
4	PA1		ADC_IN3		GT_CH1	SPI1_MOSI	USR_CTS	I2C1_SDA								
5	PA2		ADC_IN4		GT_CH2	SPI1_MISO	USR_TX									
6	PA3		ADC_IN5		GT_CH3	SPI1_SEL	USR_RX									
7	PA4		ADC_IN6		GT_CH0	SPI0_SCK	UR1_TX	I2C0_SCL								
8	PA5		ADC_IN7		GT_CH1	SPI0_MOSI	UR1_RX	I2C0_SDA								
9	PA6		ADC_IN8		GT_CH2	SPI0_MISO										
10	PA7		ADC_IN9		GT_CH3	SPI0_SEL										
11	PC4		ADC_IN10				USR_TX							PWM1_CH0		
12	PC5		ADC_IN11				USR_RX							PWM1_CH1		
13	CLDO															
14	VDD															
15	VSS															
16	nRST															
17	PB9				MT_CH3									PWM1_CH2		WAKEUP1
18	X32KIN	PB10			GT_CH0	SPI1_SEL	USR_TX							PWM1_CH3		
19	X32KOUT	PB11			GT_CH1	SPI1_SCK	USR_RX							PWM0_CH3		
20	RTCOUT	PB12				SPI0_MISO	UR0_RX							PWM0_CH0		WAKEUP0
21	XTALIN	PB13					UR0_TX	I2C0_SCL								
22	XTALOUT	PB14					UR0_RX	I2C0_SDA								
23	PB15				MT_CH0	SPI0_SEL		I2C1_SCL						PWM0_CH1		
24	PC0				MT_CH0N	SPI0_SCK		I2C1_SDA						PWM0_CH2		
25	PA8						USR_TX							PWM1_CH3		
26	PA9_BOOT					SPI0_MOSI								PWM1_CH0		CKOUT
27	PA10				MT_CH1	SPI0_MOSI	USR_RX							PWM0_CH1		
28	PA11				MT_CH1N	SPI0_MISO								PWM0_CH2		
29	SWCLK	PA12														
30	SWDIO	PA13														
31	PB0				MT_CH1	SPI1_MOSI	USR_TX	I2C0_SCL						PWM0_CH1		
32	PB1				MT_CH1N	SPI1_MISO	USR_RX	I2C0_SDA						PWM1_CH1		

Package	Alternate Function Mapping															
	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
48LQFP	System Default	GPIO	ADC	N/A	MCTM /GPTM	SPI	USART /UART	I²C	N/A	N/A	N/A	N/A	N/A	PWM	N/A	System Other
33	DVSS															
34	DVDD															
35	SCL															
36	SDA															
37	DRDYB															
38	AVDD															
38	VREFP															
39	AVSS															
39	VREFN															
40	VCM															
41	AN0															
42	AN1															
43	AN3															
44	AN2															
45	PB2				MT_ CH2	SPI0_ SEL	UR1_TX							PWM0_ CH2		CKIN
46	PB3				MT_ CH2N	SPI0_ SCK	UR1_RX							PWM1_ CH2		
47	PB7		ADC_ IN0		MT_ CH1	SPI0_ MISO	UR0_TX	I2C1_ SCL						PWM0_ CH3		
48	PB8		ADC_ IN1		MT_ CH1N	SPI0_ SEL	UR0_RX	I2C1_ SDA						PWM1_ CH3		

Table 4. Pin Description

Pin Number	Pin Name	Type(1)	I/O Structure(2)	Output Driving	Description
48LQFP					Default Function (AF0)
1	VDDA	P	—	—	Analog voltage for ADC
2	VSSA	P	—	—	Ground reference for the ADC
3	PA0	AI/O	5V	4/8/12/16 mA	PA0
4	PA1	AI/O	5V	4/8/12/16 mA	PA1
5	PA2	AI/O	5V	4/8/12/16 mA	PA2
6	PA3	AI/O	5V	4/8/12/16 mA	PA3
7	PA4	AI/O	5V	4/8/12/16 mA	PA4
8	PA5	AI/O	5V	4/8/12/16 mA	PA5
9	PA6	AI/O	5V	4/8/12/16 mA	PA6
10	PA7	AI/O	5V	4/8/12/16 mA	PA7
11	PC4	AI/O	5V	4/8/12/16 mA	PC4
12	PC5	AI/O	5V	4/8/12/16 mA	PC5
13	CLDO	P	—	—	Core power LDO 1.5 V output It is recommended to connect a 2.2 μF capacitor as close as possible between this pin and VSS.
14	VDD	P	—	—	Voltage for digital I/O
15	VSS	P	—	—	Ground reference for digital I/O
16	nRST(3)	I	5V_PU	—	External reset pin

Pin Number 48LQFP	Pin Name	Type(1)	I/O Structure(2)	Output Driving	Description Default Function (AF0)
17	PB9(3)	I/O (V_{DD})	5V	4/8/12/16 mA	PB9
18	PB10(3)	AI/O (V_{DD})	5V	4/8/12/16 mA	X32KIN
19	PB11(3)	AI/O (V_{DD})	5V	4/8/12/16 mA	X32KOUT
20	PB12(3)	I/O (V_{DD})	5V	4/8/12/16 mA	RTCOUT
21	PB13	AI/O	5V	4/8/12/16 mA	XTALIN
22	PB14	AI/O	5V	4/8/12/16 mA	XTALOUT
23	PB15	I/O	5V	4/8/12/16 mA	PB15
24	PC0	I/O	5V	4/8/12/16 mA	PC0
25	PA8	I/O	5V	4/8/12/16 mA	PA8
26	PA9	I/O	5V_PU	4/8/12/16 mA	PA9_BOOT
27	PA10	I/O	5V	4/8/12/16 mA	PA10
28	PA11	I/O	5V	4/8/12/16 mA	PA11
29	PA12	I/O	5V_PU	4/8/12/16 mA	SWCLK
30	PA13	I/O	5V_PU	4/8/12/16 mA	SWDIO
31	PB0	I/O	5V	4/8/12/16 mA	PB0
32	PB1	I/O	5V	4/8/12/16 mA	PB1
33	DVSS	P	—	—	24-bit ADC digital negative power supply
34	DVDD	P	—	—	24-bit ADC digital power supply
35	SCL	I	—	—	24-bit ADC internal I^2C interface clock line
36	SDA	I/O	—	—	24-bit ADC internal I^2C interface data line
37	DRDYB	O	—	—	24-bit ADC data ready indication: indicates valid data by going low
38	AVDD	P	—	—	24-bit ADC analog power supply
38	VREFP	AI	—	—	24-bit ADC positive reference input voltage
39	AVSS	P	—	—	24-bit ADC analog negative power supply
39	VREFN	AI	—	—	24-bit ADC negative reference input voltage
40	VCM	AO	—	—	24-bit ADC internal Common mode voltage output
41	AN0	AI	—	—	24-bit ADC input channel 0
42	AN1	AI	—	—	24-bit ADC input channel 1
43	AN3	AI	—	—	24-bit ADC input channel 3
44	AN2	AI	—	—	24-bit ADC input channel 2
45	PB2	I/O	5V	4/8/12/16 mA	PB2
46	PB3	I/O	5V	4/8/12/16 mA	PB3
47	PB7	AI/O	5V	4/8/12/16 mA	PB7
48	PB8	AI/O	5V	4/8/12/16 mA	PB8

Note: 1. I = input, O = output, A = Analog port, P = power supply, V_{DD} = V_{DD} Power.
2. 5V = 5 V operation I/O type, PU = Pull-up.
3. These pins are located at the V_{DD} power domain.

6 Electrical Characteristics

Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	External Main Supply Voltage	V_{SS} - 0.3	V_{SS} + 5.5	V
V_{DDA}	External Analog Supply Voltage	V_{SSA} - 0.3	V_{SSA} + 5.5	V
DV_{DD}	24-bit A/D Converter Module Supply Voltage	DV_{SS} - 0.3	DV_{SS} + 6.0	V
V_{IN}	Input Voltage on I/O	V_{SS} - 0.3	V_{DD} + 0.3	V
T_A	Ambient Operating Temperature Range	-40	+85	°C
T_{STG}	Storage Temperature Range	-55	+150	°C
T_J	Maximum Junction Temperature	—	125	°C
P_D	Total Power Dissipation	—	500	mW
V_{ESD}	Electrostatic Discharge Voltage – Human Body Mode	-4000	+4000	V

Recommended DC Operating Conditions

Table 6. Recommended DC Operating Conditions

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	—	2.5	5.0	5.5	V
V_{DDA}	Analog Operating Voltage	—	2.5	5.0	5.5	V

On-Chip LDO Voltage Regulator Characteristics

Table 7. LDO Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{LDO}	Internal Regulator Output Voltage	V_{DD} ≥ 2.5 V Regulator input @ I_{LDO} = 35 mA and voltage variant = ±5 %, After trimming	1.425	1.5	1.57	V
I_{LDO}	Output Current	V_{DD} = 2.5 V Regulator input @ V_{LDO} = 1.5 V	—	30	35	mA
C_{LDO}	External Filter Capacitor Value for Internal Core Power Supply	The capacitor value is dependent on the core power current consumption	1	2.2	—	μF

Power Consumption

Table 8. Power Consumption Characteristics

Symbol	Parameter	Conditions	Min.	Max.		Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	
I_{DD}	Supply Current (Run Mode)	V_{DD} = 5.0 V, HSI = 20 MHz, f_{CPU} = 20 MHz, f_{PCLK} = 20 MHz, all peripherals enabled	6.5	7.2	—	mA
		V_{DD} = 5.0 V, HSI = 20 MHz, f_{CPU} = 20 MHz, f_{BUS} = 20 MHz, all peripherals disabled	4.0	4.5	—	mA
		V_{DD} = 5.0 V, HSI = 20 MHz, f_{CPU} = 10 MHz, f_{BUS} = 10 MHz, all peripherals enabled	3.5	3.9	—	mA
		V_{DD} = 5.0 V, HSI = 20 MHz, f_{CPU} = 10 MHz, f_{BUS} = 10 MHz, all peripherals disabled	2.25	2.50	—	mA
		V_{DD} = 5.0 V, HSI off, LSI on, f_{CPU} = 32 kHz, f_{BUS} = 32 kHz, all peripherals enabled	32	41	—	µA
		V_{DD} = 5.0 V, HSI off, LSI on, f_{CPU} = 32 kHz, f_{BUS} = 32 kHz, all peripherals disabled	28	37	—	µA
	Supply Current (Sleep Mode)	V_{DD} = 5.0 V, HSI = 20 MHz, f_{CPU} = 0 MHz, f_{BUS} = 20 MHz, all peripherals enabled	3.5	3.9	—	mA
		V_{DD} = 5.0 V, HSI = 20 MHz, f_{CPU} = 0 MHz, f_{BUS} = 20 MHz, all peripherals disabled	0.80	0.92	—	mA
		V_{DD} = 5.0 V, HSI = 20 MHz, f_{CPU} = 0 MHz, f_{BUS} = 10 MHz, all peripherals enabled	2.20	2.25	—	mA
		V_{DD} = 5.0 V, HSI = 20 MHz, f_{CPU} = 0 MHz, f_{BUS} = 10 MHz, all peripherals disabled	0.65	0.75	—	mA
	Supply current (Deep-Sleep1 Mode)	V_{DD} = 5.0 V, all clock off (HSE/HSI/LSE), LDO in low power mode, LSI on, RTC on	—	23	—	µA
	Supply current (Deep-Sleep2 Mode)	V_{DD} = 5.0 V, all clock off (HSE/HSI/LSE), LDO off (DMOS on), LSI on, RTC on	—	6.5	—	µA

Note: 1. HSE means high speed external oscillator while HSI means 20 MHz high speed internal oscillator.
2. LSE means 32.768 kHz low speed external oscillator while LSI means 32 kHz low speed internal oscillator.
3. RTC means the real time clock.
4. Code = while (1) { 208 NOP } executed in Flash.
5. f_{BUS} means f_{HCLK} and f_{PCLK}.

Reset and Supply Monitor Characteristics

Table 9. V_{DD} Power Reset Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{POR}	Power On Reset Threshold (Rising Voltage on V_{DD})	T_A = -40 °C ~ 85 °C	2.22	2.35	2.48	V
V_{PDR}	Power Down Reset Threshold (Falling Voltage on V_{DD})		2.12	2.2	2.33	V
$V_{PORHYST}$	POR Hysteresis	—	—	150	—	mV
t_{POR}	Reset Delay Time	V_{DD} = 5.0 V	—	0.1	0.2	ms

Note: 1. Data based on characterization results only, not tested in production.
2. Guaranteed by design, not tested in production.
3. If the LDO is turned on, the V_{DD} POR has to be in the de-assertion condition. When the V_{DD} POR is in the assertion state then the LDO will be turned off.

Table 10. LVD/BOD Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{BOD}	Voltage of Brown Out Detection	T_A = -40 °C ~ 85 °C After factory-trimmed, V_{DD} Falling edge		2.37	2.45	2.53	V
V_{LVD}	Voltage of Low Voltage Detection	T_A = -40 °C ~ 85 °C, V_{DD} Falling edge	LVDS = 000	2.57	2.65	2.73	V
			LVDS = 001	2.77	2.85	2.93	V
			LVDS = 010	2.97	3.05	3.13	V
			LVDS = 011	3.17	3.25	3.33	V
			LVDS = 100	3.37	3.45	3,53	V
			LVDS = 101	4.15	4.25	4.35	V
			LVDS = 110	4.35	4.45	4.55	V
			LVDS = 111	4.55	4.65	4.75	V
$V_{LVDHTST}$	LVD Hysteresis	V_{DD} = 5.0 V	—	—	100	—	mV
t_{suLVD}	LVD Setup Time	V_{DD} = 5.0 V	—	—	—	5	μs
t_{atLVD}	LVD Active Delay Time	V_{DD} = 5.0 V	—	—	—	—	ms
I_{DDLVD}	Operation Current (3)	V_{DD} = 5.0 V	—	—	10	20	μA

Note: 1. Data based on characterization results only, not tested in production.
2. Guaranteed by design, not tested in production.
3. Bandgap current is not included.
4. LVDS field is in the PWRCU LVDCSR register.

External Clock Characteristics

Table 11. High Speed External Clock (HSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	T_A = -40 °C ~ 85 °C	2.5	—	5.5	V
f_{HSE}	High Speed External Oscillator Frequency (HSE)	V_{DD} = 2.5 V ~ 5.0 V	4	—	20	MHz
C_{LHSE}	Load Capacitance	V_{DD} = 5.0 V, R_{ESR} = 100 Ω @ 20 MHz	—	—	12	pF
R_{FHSE}	Internal Feedback Resistor between XTALIN and XTALOUT pins	V_{DD} = 5.0 V	—	0.5	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 5.0 V, C_L = 12 pF @ 20 MHz, HSEDR = 0	—	—	110	Ω
		V_{DD} = 2.5 V, C_L = 12 pF @ 20 MHz, HSEDR = 1				
D_{HSE}	HSE Oscillator Duty Cycle	—	40	—	60	%
I_{DDHSE}	HSE Oscillator Current Consumption	V_{DD} = 5.0 V, R_{ESR} = 100 Ω, C_L = 12 pF @ 8 MHz, HSEDR = 0	—	0.85	—	mA
		V_{DD} = 5.0 V, R_{ESR} = 25 Ω, C_L = 12 pF @ 20 MHz, HSEDR = 1	—	3.0	—	
I_{PWDHSE}	HSE Oscillator Power Down Current	V_{DD} = 5.0 V	—	—	0.01	μA
t_{SUHSE}	HSE Oscillator Startup Time	V_{DD} = 5.0 V	—	—	4	ms

Note: The following guidelines are recommended to increase the stability of the crystal circuit of the HSE clock in the PCB layout:

1. The crystal oscillator should be located as close as possible to the MCU to keep the trace lengths as short as possible to reduce any parasitic capacitance.
2. Shield lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
3. Keep any high frequency signal lines away from the crystal area to prevent any crosstalk adverse effects.

Table 12. Low Speed External Clock (LSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Operation Range	T_A = -40 °C ~ 85 °C	2.5	—	5.5	V
f_{CK_LSE}	LSE Frequency	V_{DD} = 2.5 V ~ 5.5 V	—	32.768	—	kHz
R_F	Internal Feedback Resistor	—	—	10	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 5.0 V	30	—	TBD	kΩ
C_L	Recommended Load Capacitances	V_{DD} = 5.0 V	6	—	TBD	pF
I_{DDLSE}	Oscillator Supply Current (High current mode)	f_{CK_LSE} = 32.768 kHz, R_{ESR} = 50 kΩ, $C_L \geq 7$ pF, V_{DD} = 2.5 V ~ 5.5 V, T_A = -40 °C ~ +85 °C	—	4.0	5.6	μA
	Oscillator Supply Current (Low Current Mode)	f_{CK_LSE} = 32.768 kHz, R_{ESR} = 50 kΩ, $C_L < 7$ pF, V_{DD} = 2.5 V ~ 5.5 V, T_A = -40 °C ~ +85 °C	—	3.6	4.5	μA
	Power Down Current	—	—	—	0.01	μA
t_{SULSE}	Startup Time (Low Current Mode)	f_{CK_LSI} = 32.768 kHz, V_{DD} = 2.5 V ~ 5.5 V	500	—	—	ms

Internal Clock Characteristics

Table 13. High Speed Internal Clock (HSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	T_A = -40 °C ~ 85 °C	2.5	—	5.5	V
f_{HSI}	HSI Frequency	V_{DD} = 5 V @ 25 °C	—	20	—	MHz
ACC_{HSI}	Factory Calibrated HSI Oscillator Frequency Accuracy	V_{DD} = 5.0 V, T_A = 25 °C	-2	—	2	%
		V_{DD} = 2.5 V ~ 5.5 V, T_A = -40 °C ~ 85 °C	-3	—	3	%
Duty	Duty Cycle	f_{HSI} = 20 MHz	35	—	65	%
I_{DDHSI}	Oscillator Supply Current	f_{HSI} = 20 MHz @ V_{DD} = 2.5 V ~ 5.5 V	—	—	140	μA
	Power Down Current		—	—	0.01	μA
T_{SUHSI}	HSI Oscillator Startup time	f_{HSI} = 20 MHz	—	—	20	μs

Table 14. Low Speed Internal Clock (LSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	T_A = -40 °C ~ 85 °C	2.5	—	5.5	V
f_{LSI}	Low Speed Internal Oscillator Frequency (LSI)	V_{DD} = 5.0 V, T_A = -40 °C ~ 85 °C	21	32	43	kHz
ACC_{LSI}	LSI Frequency Accuracy	V_{DD} = 5.0 V, with factory-trimmed	-10	—	+10	%
I_{DDLSI}	LSI Oscillator Operating Current	V_{DD} = 5.0 V	—	0.5	0.8	μA
t_{SULSI}	LSI Oscillator Startup Time	V_{DD} = 5.0 V	—	—	100	μs

Memory Characteristics

Table 15. Flash Memory Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{ENDU}	Number of Guaranteed Program/Erase Cycles before failure (Endurance)	T_A = -40 °C ~ 85 °C	10	—	—	K cycles
t_{RET}	Data Retention Time	T_A = -40 °C ~ 85 °C	10	—	—	Years
t_{PROG}	Word Programming Time	T_A = -40 °C ~ 85 °C	20	—	—	μs
t_{ERASE}	Page Erase Time	T_A = -40 °C ~ 85 °C	2	—	—	ms
t_{MERASE}	Mass Erase Time	T_A = -40 °C ~ 85 °C	10	—	—	ms

I/O Port Characteristics

Table 16. I/O Port Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{IL}	Low Level Input Current	5.0 V I/O	V_I = V_{SS}, On-chip pull-up resister disabled	—	—	3	μA
		Reset pin		—	—	3	μA
I_{IH}	High Level Input Current	5.0 V I/O	V_I = V_{DD}, On-chip pull-down resister disabled	—	—	3	μA
		Reset pin		—	—	3	μA
V_{IL}	Low Level Input Voltage	5.0 V I/O		-0.5	—	V_{DD} × 0.35	V
		Reset pin		-0.5	—	V_{DD} × 0.35	V
V_{IH}	High Level Input Voltage	5.0 V I/O		V_{DD} × 0.65	—	V_{DD} + 0.5	V
		Reset pin		V_{DD} × 0.65	—	V_{DD} + 0.5	V
V_{HYS}	Schmitt Trigger Input Voltage Hysteresis	5.0 V I/O		—	0.12 × V_{DD}	—	mV
		Reset pin		—	0.12 × V_{DD}	—	mV
I_{OL}	Low Level Output Current (GPIO Sink Current)	5.0 V I/O 4 mA drive, V_{OL} = 0.6 V		4	—	—	mA
		5.0 V I/O 8 mA drive, V_{OL} = 0.6 V		8	—	—	mA
		5.0 V I/O 12 mA drive, V_{OL} = 0.6 V		12	—	—	mA
		5.0 V I/O 16 mA drive, V_{OL} = 0.6 V		16	—	—	mA
I_{OH}	High Level Output Current (GPIO Source Current)	5.0 V I/O 4 mA drive, V_{OH} = V_{DD} - 0.6 V		—	4	—	mA
		5.0 V I/O 8 mA drive, V_{OH} = V_{DD} - 0.6 V		—	8	—	mA
		5.0 V I/O 12 mA drive, V_{OH} = V_{DD} - 0.6 V		—	12	—	mA
		5.0 V I/O 16 mA drive, V_{OH} = V_{DD} - 0.6 V		—	16	—	mA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OL}	Low Level Output Voltage	5.0 V 4 mA drive I/O, I_{OL} = 4 mA	—	—	0.6	V
		5.0 V 8 mA drive I/O, I_{OL} = 8 mA	—	—	0.6	V
		5.0 V 12 mA drive I/O, I_{OL} = 12 mA	—	—	0.6	V
		5.0 V 16 mA drive I/O, I_{OL} = 16 mA	—	—	0.6	V
V_{OH}	High Level Output Voltage	5.0 V 4 mA drive I/O, I_{OH} = 4 mA	V_{DD} - 0.6	—	—	V
		5.0 V 8 mA drive I/O, I_{OH} = 8 mA	V_{DD} - 0.6	—	—	V
		5.0 V 12 mA drive I/O, I_{OH} = 12 mA	V_{DD} - 0.6	—	—	V
		5.0 V 16 mA drive I/O, I_{OH} = 16 mA	V_{DD} - 0.6	—	—	V
R_{PU}	Internal Pull-up Resistor	V_{DD} = 5.0 V	—	50	—	kΩ
		V_{DD} = 3.3 V	—	76	—	kΩ
R_{PD}	Internal Pull-down Resistor	V_{DD} = 5.0 V	—	50	—	kΩ
		V_{DD} = 3.3 V	—	76	—	kΩ

12-Bit ADC Characteristics

Table 17. 12-Bit ADC Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	—	2.5	5.0	5.5	V
V_{ADCIN}	A/D Converter Input Voltage Range	—	0	—	V_{REF+}	V
V_{REF+}	A/D Converter Reference Voltage	—	—	V_{DDA}	V_{DDA}	V
I_{ADC}	Current Consumption	V_{DDA} = 5.0 V	—	1.4	1.5	mA
I_{ADC_DN}	Power Down Current Consumption	V_{DDA} = 5.0 V	—	—	0.1	μA
f_{ADC}	A/D Converter Clock Frequency	—	0.7	—	16	MHz
f_S	Sampling Rate	—	0.05	—	1	MHz
t_{DL}	Data Latency	—	—	12.5	—	$1/f_{ADC}$ Cycles
$t_{S\&H}$	Sampling & Hold Time	—	—	3.5	—	$1/f_{ADC}$ Cycles
$t_{ADCCONV}$	A/D Converter Conversion Time	—	—	16	—	$1/f_{ADC}$ Cycles
R_I	Input Sampling Switch Resistance	—	—	—	1	kΩ
C_I	Input Sampling Capacitance	No pin/pad capacitance included	—	4	—	pF
t_{SU}	Start Up Time	—	—	—	1	μs
N	Resolution	—	—	12	—	bits

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
INL	Integral Non-linearity Error	f_S = 750 kHz, V_{DDA} = 5.0 V	—	±2	±5	LSB
DNL	Differential Non-linearity Error	f_S = 750 kHz, V_{DDA} = 5.0 V	—	±1	—	LSB
E_O	Offset Error	—	—	—	±10	LSB
E_G	Gain Error	—	—	—	±10	LSB

Note: 1. Guaranteed by design, not tested in production.

2. Due to the A/D Converter input channel and GPIO pin-shared function design limitation, the V_{DDA} supply power of the A/D Converter has to be equal to the V_{DD} supply power of the MCU in the application circuit.
3. The figure below shows the equivalent circuit of the A/D Converter Sample-and-Hold input stage where C_I is the storage capacitor, R_I is the resistance of the sampling switch and R_S is the output impedance of the signal source V_S. Normally the sampling phase duration is approximately, $3.5/f_{ADC}$. The capacitance, C_I, must be charged within this time frame and it must be ensured that the voltage at its terminals becomes sufficiently close to V_S for accuracy. To guarantee this, R_S is not allowed to have an arbitrarily large value.

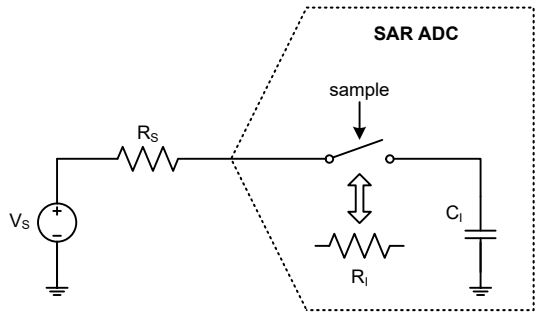


Figure 6. ADC Sampling Network Model

The worst case occurs when the extremities of the input range (0 V and V_{REF}) are sampled consecutively. In this situation a sampling error below 1/4 LSB is ensured by using the following equation:

$$R_S < \frac{3.5}{f_{ADC} C_I \ln(2^{N+2})} - R_I$$

Where f_{ADC} is the ADC clock frequency and N is the ADC resolution (N = 12 in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model.

If, in a system where the A/D Converter is used, there are no rail-to-rail input voltage variations between consecutive sampling phases, R_S may be larger than the value indicated by the equation above.

24-Bit ADC Characteristics

Table 18. 24-Bit ADC Characteristics

$DV_{DD} = AV_{DD}$, T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
AV_{DD}	Supply Voltage for VCM, ADC, PGA	—	2.4	—	5.5	V
V_{OUT_VCM}	VCM Output Voltage (VCM Pin)	AV_{DD} = 3.3 V, No load	-5%	1.25	+5%	V
TC_{VCM}	VCM Temperature Coefficient	Ta = -40 °C ~ 85 °C, AV_{DD} = 3.3V, I_{LOAD} = 10 μA	—	—	0.24	mV/°C
ΔV_{LINE_VCM}	VCM Line Regulation	2.4 V ≤ AV_{DD} ≤ 3.3 V, No load	—	—	0.4	%/V
t_{VCMS}	VCM Turn-on Stable Time	AV_{DD} = 3.3V, No load	—	—	10	ms
I_{OH}	Source Current for VCM Pin	AV_{DD} = 3.3V, ΔV_{OUT_VCM} = -2%	3	—	—	mA
I_{OL}	Sink Current for VCM Pin	AV_{DD} = 3.3V, ΔV_{OUT_VCM} = +2%	3	—	—	mA
ADC & ADC Internal Reference Voltage (Sigma Delta ADC)						
I_{ADC}	Additional Current for ADC Enable	VCM enable, VRBUFP = 1 and VRBUFN = 1	—	—	1120	μA
		VCM enable, VRBUFP = 0 and VRBUFN = 0	—	820	970	μA
		VCM disable, VRBUFP = 0 and VRBUFN = 0	—	500	650	μA
I_{ADSTB}	Standby Current	ADC power down, no load	—	—	1	μA
RS_{ADC}	Resolution	—	—	—	24	bit
INL	Integral Non-linearity	AV_{DD} = 3.3 V, V_{REF} = 1.25 V, ΔSI = ±450 mV, PGA Gain = 1	—	±50	—	ppm
NFB	Noise Free Bits	V_{REF} = 2.5 V, Gain = 32 Data rate = 10 Hz	—	18.0	—	Bit
		V_{REF} = 2.5 V, Gain = 64 Data rate = 10 Hz	—	17.4	—	Bit
		V_{REF} = 2.5 V, Gain = 128 Data rate = 10 Hz	—	16.7	—	Bit
ENOB	Effective Number of Bits	V_{REF} = 2.5 V, Gain = 32 Data rate = 10 Hz	—	20.7	—	Bit
		V_{REF} = 2.5 V, Gain = 64 Data rate = 10 Hz	—	20.1	—	Bit
		V_{REF} = 2.5 V, Gain = 128 Data rate = 10 Hz	—	19.4	—	Bit
f_{ADCK}	ADC Clock Frequency	—	40	409.6	440	kHz
f_{ADO}	ADC Output Data Rate	f_{MCLK} = 4.9152 MHz, FLMS[2:0] = 000B	5	—	640	Hz
		f_{MCLK} = 4.9152 MHz, FLMS[2:0] = 010B	12.5	—	1600	Hz
V_{REFP}	External Reference Input Voltage	VREFS = 1, VRBUFP = 0, VRBUFN = 0	V_{REFN} + 1	—	AV_{DD}	V
V_{REFN}			0	—	V_{REFP} - 1	V
V_{REF}		V_{REF} = (V_{REFP} - V_{REFN}) × VREFGN	1	—	AV_{DD}/2	V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
PGA						
V_{CM_PGA}	Common Mode Voltage Range	—	0.4	—	AV_{DD} - 0.95	V
ΔD_I	Differentail Input Voltage Range	Gain = PGAGN × ADGN, ΔD_I = DI+ - DI-	$-V_{REF}$/ Gain	—	$+V_{REF}$/ Gain	V
Temperature Sensor						
TC_{TS}	Temperature Sensor Temperature Coefficient	Ta = -40°C ~ 85°C, V_{REF} = 1.25V, VGS[1:0] = 00B (Gain = 1), VRBUFP = 0, VRBUFN = 0	—	175	—	µV/ °C

Effective Number of Bits (ENOB)

V_{REF}=2.5V, f_{ADCK}=163kHz

Data Rate (SPS)	PGA Gain							
	1	2	4	8	16	32	64	128
5	21.5	21.2	21.1	21.1	21.0	20.9	20.4	19.6
10	21.2	21.0	21.0	20.9	20.8	20.7	20.1	19.4
20	21.1	20.7	20.7	20.6	20.5	20.3	19.7	18.9
40	20.6	20.5	20.4	20.2	20.1	19.9	19.2	18.5
80	20.2	20.1	20.0	19.9	19.8	19.5	18.8	18.0
160	19.7	19.5	19.5	19.4	19.3	19.0	18.4	17.6
320	19.1	18.9	18.9	18.8	18.7	18.5	17.9	17.1
640	18.6	18.4	18.4	18.3	18.3	18.0	17.4	16.6

V_{REF}=2.5V, f_{ADCK}=409kHz

Data Rate (SPS)	PGA Gain							
	1	2	4	8	16	32	64	128
12.5	21.9	21.4	21.4	21.3	21.1	20.7	19.9	19.2
25	21.6	21.1	21.1	21.0	20.9	20.4	19.6	18.8
50	21.2	20.9	20.8	20.7	20.4	19.9	19.2	18.3
100	20.8	20.5	20.4	20.3	20.0	19.5	18.8	17.9
200	20.3	19.7	19.7	19.6	19.4	18.9	18.2	17.4
400	19.3	19.0	19.0	18.9	18.8	18.4	17.8	16.9
800	18.8	18.6	18.6	18.5	18.3	17.9	17.2	16.5
1600	18.4	18.2	18.2	18.1	17.9	17.4	16.8	16.1

V_{REF}=1.65V, f_{ADCK}=163kHz

Data Rate (SPS)	PGA Gain							
	1	2	4	8	16	32	64	128
5	21.5	21.2	21.2	21.1	20.9	20.5	20.0	19.2
10	21.3	21.0	20.9	20.7	20.5	20.2	19.5	18.7
20	20.9	20.6	20.5	20.4	20.2	19.8	19.1	18.3
40	20.4	20.1	20.1	20.0	19.8	19.4	18.8	18.0
80	19.8	19.5	19.5	19.4	19.2	18.8	18.2	17.5
160	19.3	19.0	19.0	18.9	18.7	18.4	17.8	17.0
320	18.8	18.5	18.5	18.4	18.3	17.9	17.3	16.5
640	18.3	18.1	18.1	18.0	17.8	17.5	16.8	16.0

V_{REF}=1.65V, f_{ADCK}=409kHz

Data Rate (SPS)	PGA Gain							
	1	2	4	8	16	32	64	128
12.5	21.8	21.4	21.2	21.1	20.7	20.3	19.5	18.6
25	21.4	21.1	20.9	20.7	20.3	19.7	19.0	18.2
50	20.9	20.6	20.5	20.3	19.9	19.4	18.6	17.7
100	20.4	20.2	20.0	19.8	19.4	18.9	18.1	17.3
200	19.8	19.4	19.3	19.2	18.9	18.4	17.7	16.8
400	19.0	18.8	18.7	18.6	18.4	17.8	17.2	16.3
800	18.7	18.4	18.3	18.2	17.9	17.4	16.7	15.8
1600	18.2	18.0	17.9	17.7	17.3	16.7	16.2	15.4

V_{REF}=1.2V, f_{ADCK}=163kHz

Data Rate (SPS)	PGA Gain							
	1	2	4	8	16	32	64	128
5	20.6	20.4	20.4	20.3	20.3	20.1	19.6	18.9
10	20.5	20.3	20.3	20.2	20.0	19.9	19.2	18.4
20	20.3	19.9	19.9	19.8	19.7	19.4	18.8	18.0
40	19.8	19.5	19.5	19.4	19.2	18.9	18.3	17.5
80	19.3	19.1	19.1	19.0	18.8	18.5	17.8	17.0
160	19.0	18.8	18.7	18.6	18.3	18.0	17.4	16.5
320	18.5	18.2	18.2	18.1	17.8	17.5	16.9	16.1
640	17.9	17.7	17.7	17.6	17.3	17.0	16.4	15.6

V_{REF}=1.2V, f_{ADCK}=409kHz

Data Rate (SPS)	PGA Gain							
	1	2	4	8	16	32	64	128
12.5	20.9	20.7	20.5	20.3	20.1	19.8	19.1	18.2
25	20.7	20.4	20.2	20.1	19.8	19.4	18.6	17.8
50	20.3	20.1	19.8	19.7	19.4	18.8	18.1	17.4
100	19.9	19.6	19.4	19.2	18.9	18.4	17.7	16.8
200	19.5	19.2	19.0	18.8	18.5	17.9	17.2	16.4
400	18.9	18.7	18.6	18.4	18.0	17.5	16.7	15.9
800	18.5	18.2	18.0	17.8	17.5	16.9	16.2	15.4
1600	17.9	17.6	17.5	17.3	16.9	16.4	15.7	14.9

MCTM/GPTM/PWM Characteristics

Table 19. MCTM/GPTM/PWM Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{TM}	Timer Clock Source for MCTM, GPTM and PWM	—	—	—	f_{PCLK}	MHz
t_{RES}	Timer Resolution Time	—	1	—	—	f_{TM}
f_{EXT}	External Single Frequency on Channel 1 ~ 4	—	—	—	1/2	f_{TM}
RES	Timer Resolution	—	—	—	16	bits

I²C Characteristics

Table 20. I²C Characteristics

Symbol	Parameter	Standard Mode		Fast Mode		Fast Plus Mode		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	SCL Clock Frequency	—	100	—	400	—	1000	kHz
$t_{SCL(H)}$	SCL Clock High Time	4.5	—	1.125	—	0.45	—	μs
$t_{SCL(L)}$	SCL Clock Low Time	4.5	—	1.125	—	0.45	—	μs
t_{FALL}	SCL And SDA Fall Time	—	1.3	—	0.34	—	0.135	μs
t_{RISE}	SCL And SDA Rise Time	—	1.3	—	0.34	—	0.135	μs
$t_{SU(SDA)}$	SDA Data Setup Time	500	—	125	—	50	—	ns
$t_{H(SDA)}$	SDA Data Hold Time (Note 5)	0	—	0	—	0	—	ns
	SDA Data Hold Time (Note 6)	100	—	100	—	100	—	ns
$t_{VD(SDA)}$	SDA Data Valid Time	—	1.6	—	0.475	—	0.25	μs
$t_{SU(STA)}$	START Condition Setup Time	500	—	125	—	50	—	ns
$t_{H(STA)}$	START Condition Hold Time	0	—	0	—	0	—	ns
$t_{SU(STO)}$	STOP Condition Setup Time	500	—	125	—	50	—	ns

Note: 1. Guaranteed by design, not tested in production.
2. To achieve 100 kHz standard mode, the peripheral clock frequency must be higher than 2 MHz.
3. To achieve 400 kHz fast mode, the peripheral clock frequency must be higher than 8 MHz.
4. To achieve 1 MHz fast mode plus, the peripheral clock frequency must be higher than 20 MHz.
5. The above characteristic parameters of the I²C bus timing are based on: COMB_FILTER_En = 0 and SEQ_FILTER = 00.
6. The above characteristic parameters of the I²C bus timing are based on: COMB_FILTER_En = 1 and SEQ_FILTER = 00.

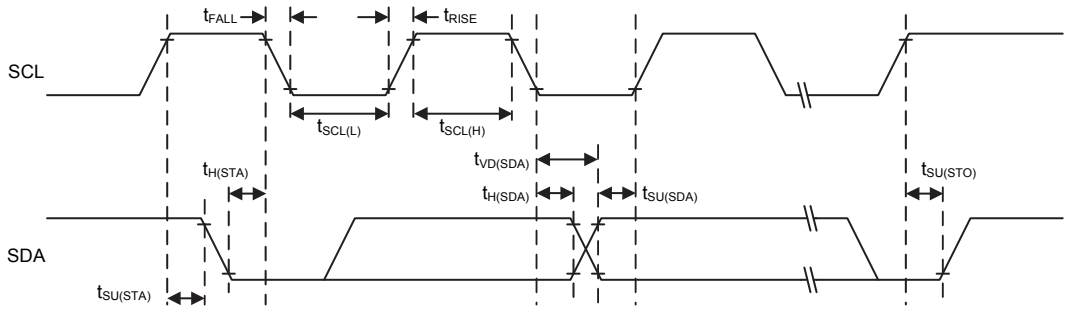


Figure 7. I²C Timing Diagrams

SPI Characteristics

Table 21. SPI Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SPI Master Mode						
f_{SCK}	SPI Master Output SCK Clock Frequency	Master mode SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/2$	MHz
$t_{SCK(H)}$ $t_{SCK(L)}$	SCK Clock High and Low Time	—	$t_{SCK}/2$ - 2	—	$t_{SCK}/2$ + 1	ns
$t_{V(MO)}$	Data Output Valid Time	—	—	—	5	ns
$t_{H(MO)}$	Data Output Hold Time	—	2	—	—	ns
$t_{SU(MI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(MI)}$	Data Input Hold Time	—	5	—	—	ns
SPI Slave Mode						
f_{SCK}	SPI Slave Input SCK Clock Frequency	Slave mode SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/3$	MHz
$Duty_{SCK}$	SPI Slave Input SCK Clock Duty Cycle	—	30	—	70	%
$t_{SU(SEL)}$	SEL Enable Setup Time	—	3 t_{PCLK}	—	—	ns
$t_{H(SEL)}$	SEL Enable Hold Time	—	2 t_{PCLK}	—	—	ns
$t_{A(SO)}$	Data Output Access Time	—	—	—	3 t_{PCLK}	ns
$t_{DIS(SO)}$	Data Output Disable Time	—	—	—	10	ns
$t_{V(SO)}$	Data Output Valid Time	—	—	—	25	ns
$t_{H(SO)}$	Data Output Hold Time	—	15	—	—	ns
$t_{SU(SI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(SI)}$	Data Input Hold Time	—	4	—	—	ns

Note: 1. f_{SCK} is SPI output/input clock frequency and $t_{SCK} = 1/f_{SCK}$.
2. f_{PCLK} is SPI peripheral clock frequency and $t_{PCLK} = 1/f_{PCLK}$.

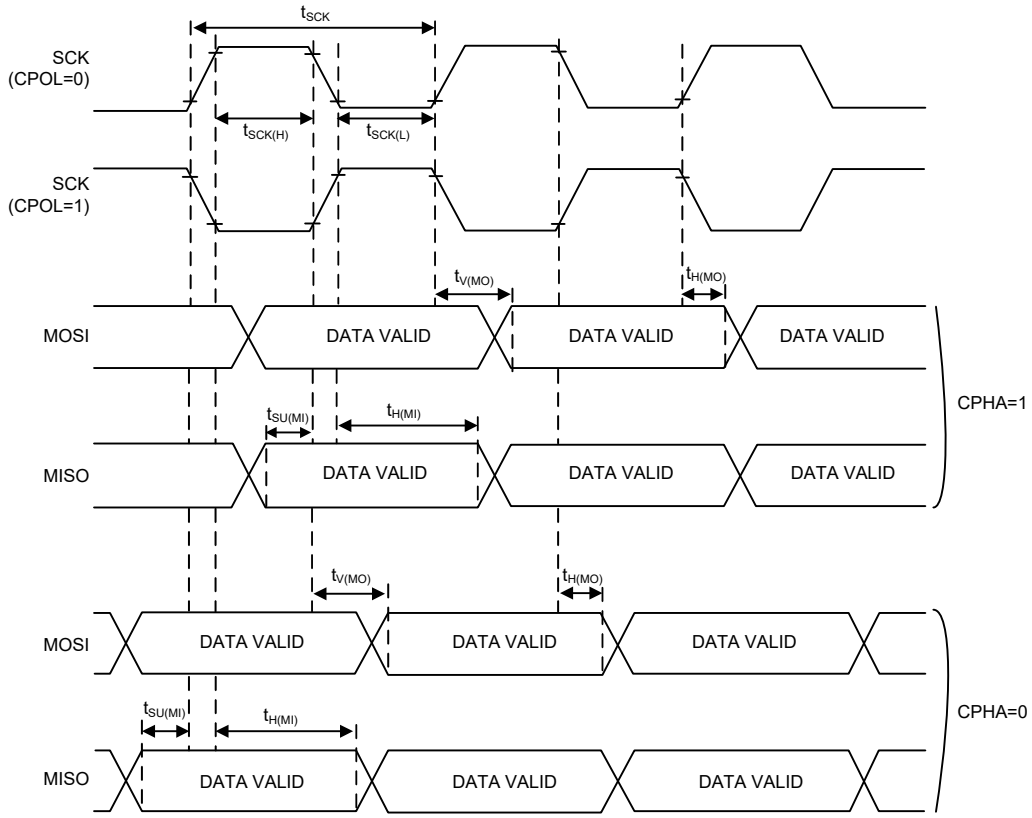


Figure 8. SPI Timing Diagrams – SPI Master Mode

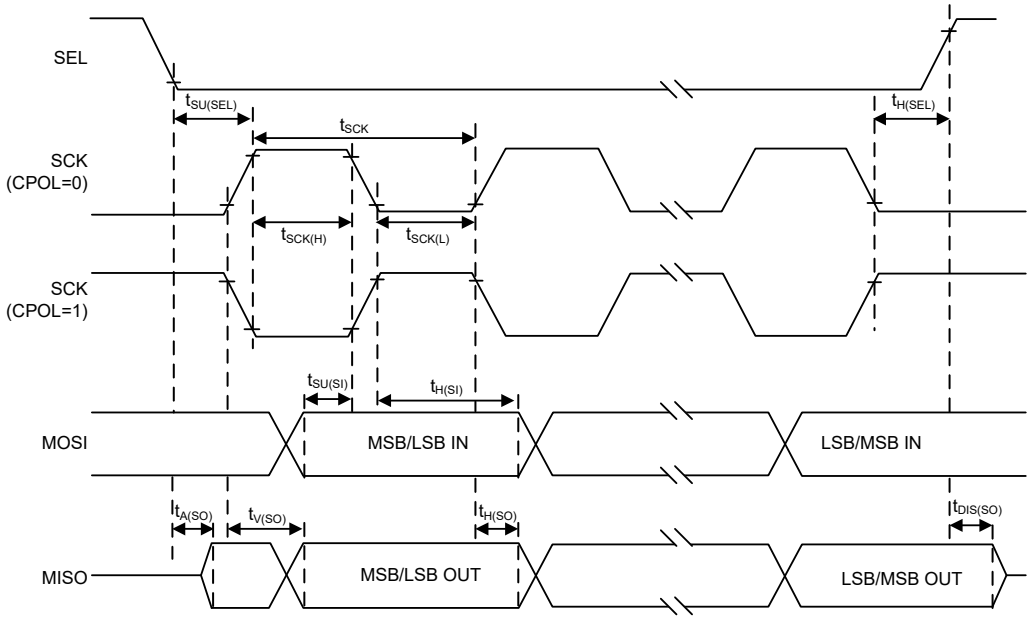


Figure 9. SPI Timing Diagrams – SPI Slave Mode with CPHA = 1

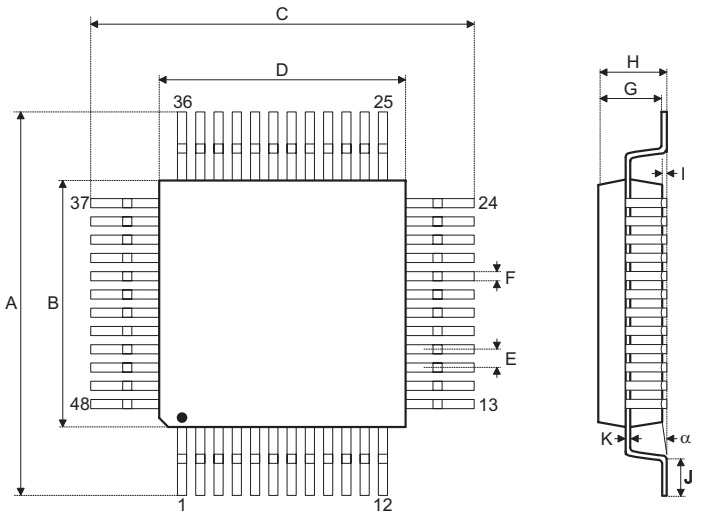
7 Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

48-pin LQFP (7mm × 7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.020 BSC	—
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.0 BSC	—
B	—	7.0 BSC	—
C	—	9.0 BSC	—
D	—	7.0 BSC	—
E	—	0.5 BSC	—
F	0.17	0.22	0.27
G	1.35	1.4	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°