HT32F52342/HT32F52352
Datasheet

32-Bit Arm® Cortex®-M0+ Microcontroller,
up to 128 KB Flash and 16 KB SRAM with 1 MSPS ADC, USART,
UART, SPI, I²C, I²S, MCTM, GPTM, BFTM, SCI, CRC, RTC, WDT,
PDMA, EBI and USB2.0 FS

Revision: V1.50 Date: April 29, 2019

www.holtek.com

Table of Contents

List of Tables

List of Figures

1 General Description

The HOLTEK HT32F52342/52352 devices are high performance, low power consumption 32-bit microcontrollers based around an Arm® Cortex®-M0+ processor core. The Cortex®-M0+ is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer, and including advanced debug support.

The devices operate at a frequency of up to 48 MHz with a Flash accelerator to obtain maximum efficiency. It provides up to 128 KB of embedded Flash memory for code/data storage and 16 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as ADC, I^2C, USART, UART, SPI, I^2S, GPTM, MCTM, SCI, CRC-16/32, RTC, WDT, PDMA, EBI, USB2.0 FS, SW-DP (Serial Wire Debug Port), etc., are also implemented in the device series. Several power saving modes provide the flexibility for maximum optimisation between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features ensure that the devices are suitable for use in a wide range of applications, especially in areas such as white goods application control, power monitors, alarm systems, consumer products, handheld equipment, data logging applications, motor control and so on.

2 Features

Core

- 32-bit Arm® Cortex®-M0+ processor core
- Up to 48 MHz operating frequency
- 0.93 DMIPS/MHz (Dhrystone v2.1)
- Single-cycle multiplication
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized, low-power processor. The processor is based on the ARMv6-M architecture and supports Thumb® instruction sets; single-cycle I/O port; hardware multiplier and low latency interrupt respond time.

On-chip Memory

- Up to 128 KB on-chip Flash memory for instruction/data and options storage
- 16 KB on-chip SRAM
- Supports multiple boot modes

The Arm® Cortex®-M0+ processor accesses and debug accesses share the single external interface to external AHB peripherals. The processor accesses take priority over debug accesses. The maximum address range of the Cortex®-M0+ is 4 GB since it has a 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex®-M0+ processor to reduce the software complexity of repeated implementation by different device vendors. However, some regions are used by the Arm® Cortex®-M0+ system peripherals. Refer to the Arm® Cortex®-M0+ Technical Reference Manual for more information. Figure 2 shows the memory map of the HT32F52342/52352 series of devices, including code, SRAM, peripheral, and other pre-defined regions.

Flash Memory Controller – FMC

- Flash accelerator for maximum efficiency
- 32-Bit word programming with In System Programming Interface (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions and pre-fetch buffer for the embedded on-chip Flash Memory. Since the access speed of the Flash Memory is slower than the CPU, a wide access interface with a pre-fetch buffer and cache are provided for the Flash Memory in order to reduce the CPU waiting time which will cause CPU instruction execution delays. Flash Memory word program/page erase functions are also provided.

Reset Control Unit – RSTCU

- Supply supervisor:
  - Power On Reset / Power Down Reset – POR/PDR
  - Brown-out Detector – BOD
  - Programmable Low Voltage Detector – LVD

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by an external signal, internal events and the reset generators.

Clock Control Unit – CKCU

- External 4 to 16 MHz crystal oscillator
- External 32,768 Hz crystal oscillator
- Internal 8 MHz RC oscillator trimmed to ±2 % accuracy at 3.3V operating voltage and 25 °C operating temperature
- Internal 32 kHz RC oscillator
- Integrated system clock PLL
- Independent clock divider and gating bits for peripheral clock sources

The Clock Control unit, CKCU, provides a range of oscillator and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), a Phase Lock Loop (PLL), a HSE clock monitor, clock prescalers, clock multiplexers, APB clock divider and gating circuitry. The AHB, APB and Cortex®-M0+ clocks are derived from the system clock (CK_SYS) which can come from the LSI, LSE, HSI, HSE or PLL. The Watchdog Timer and Real Time Clock (RTC) use either the LSI or LSE as their clock source.

Power Management – PWRCU

- Single V_{DD} power supply: 2.0 V to 3.6 V
- Integrated 1.5 V LDO regulator for CPU core, peripherals and memories power supply
- V_{BAT} battery power supply for RTC and backup registers
- Three power domains: V_{DD}, 1.5 V and Backup
- Four power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2, Power-Down

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in these devices provides many types of power saving modes such as Sleep, Deep-Sleep1, Deep-Sleep2 and Power-Down mode. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.

External Interrupt/Event Controller – EXTI

- Up to 16 EXTI lines with configurable trigger source and type
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge, or both edge
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

The External Interrupt/Event Controller, EXTI, comprises 16 edge detectors which can generate a wake-up event or interrupt requests independently. Each EXTI line can also be masked independently.

Analog to Digital Converter – ADC

- 12-bit SAR ADC engine
- Up to 1 Msps conversion rate
- Up to 12 external analog input channels

A 12-bit multi-channel ADC is integrated in the device. There are multiplexed channels, which include 12 external analog signal channels and 2 internal channels which can be measured. If the input voltage is required to remain within a specific threshold window, an Analog Watchdog function will monitor and detect these signals. An interrupt will then be generated to inform the device that the input voltage is not within the preset threshold levels. There are three conversion modes to convert an analog signal to digital data. The ADC can be operated in one shot, continuous and discontinuous conversion modes.

Analog Comparator – CMP

- Rail-to-rail comparator
- Each comparator has configurable negative inputs used for flexible voltage selection
- Dedicated I/O pin or internal voltage reference provided by 6-bit scaler
- Programmable hysteresis
- Programming speed and consumption
- Comparator output can be output to I/O or to timers or ADC trigger inputs
- 6-bit scaler can be configurable to dedicated I/O for voltage reference
- Comparator has interrupt generation capability with wakeup from Sleep or Deep Sleep modes through the EXTI controller

The two general purpose comparators (CMP) are implemented within the device. They can be configured either as standalone comparators or combined with the different kinds of peripheral IPs. Each comparator is capable of asserting interrupts to the NVIC or waking up the MCU from Dthe eep Sleep mode through the EXTI wakeup event management unit.

I/O Ports – GPIO

- Up to 51 GPIOs
- Port A, B, C, D are mapped as 16 external interrupts – EXTI
- Almost all I/O pins have a configurable output driving current.

There are up to 51 General Purpose I/O pins, GPIO, named from PA0~PA15 to PD0~PD3 for the implementation of logic input/output functions. Each of the GPIO ports has a series of related control and configuration registers to maximise flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

Motor Control Timer – MCTM

- One 16-bit up, down, up/down auto-reload counter
- 16-bit programmable prescaler allowing counter clock frequency division by any factor between 1 and 65536
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output
- Complementary Outputs with programmable dead-time insertion
- Supports 3-phase motor control and hall sensor interface
- Break input to force the timer's output signals into a reset or fixed condition

The Motor Control Timer consists of a single 16-bit up/down counter, four 16-bit CCRs (Capture/Compare Registers), single one 16-bit counter-reload register (CRR), single 8-bit repetition counter and several control/status registers. It can be used for a variety of purposes including measuring the pulse widths of input signals or generating output waveforms such as compare match outputs, PWM outputs or complementary PWM outputs with dead-time insertion. The MCTM is capable of offering full functional support for motor control, hall sensor interfacing and brake input.

PWM Generation and Capture Timers – GPTM

- One 16-bit up, down, up/down auto-reload counter
- 16-bit programmable prescaler allowing counter clock frequency division by any factor between 1 and 65536
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder

The General Purpose Timer consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR) and several control/status registers. They can be used for a variety of purposes including general time measurement, input signal pulse width measurement, output waveform generation such as single pulse generation, or PWM output generation. The GPTM supports an Encoder Interface using a decoder with two inputs.

Single Channel Generation and Capture Timers – SCTM

- One 16-bit up and auto-reload counter
- One channel for each timer
- 16-bit programmable prescaler allowing counter clock frequency division by any factor between 1 and 65536
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned
- Single Pulse Mode Output

The Single-Channel Timer consists of one 16-bit up-counter, one 16-bit Capture/Compare Register (CCR), one 16-bit Counter-Reload Register (CRR) and several control/status registers. It can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as single pulse generation or PWM output.

Basic Function Timer – BFTM

- One 32-Bit compare/match count-up counter – no I/O control features
- One shot mode – counting stops after a match condition
- Repetitive mode – restart counter after a match condition

The Basic Function Timer is a simple count-up 32-bit counter designed to measure time intervals and generate a one shot or repetitive interrupts. The BFTM operates in two functional modes, repetitive or one shot mode. In the repetitive mode the BFTM restarts the counter when a compare match event occurs. The BFTM also supports a one shot mode which forces the counter to stop counting when a compare match event occurs.

Watchdog Timer – WDT

- 12-Bit down counter with 3-bit prescaler
- Reset event for the system
- Programmable watchdog timer window function
- Register write protection function

The Watchdog Timer is a hardware timing circuit that can be used to detect system failures due to software malfunctions. It includes a 12-bit count-down counter, a prescaler, a WDT delta value register, WDT operation control circuitry and a WDT protection mechanism. If the software does not reload the counter value before a Watchdog Timer underflow occurs, a reset will be generated when the counter underflows. In addition, a reset is also generated if the software reloads the counter when the counter value is greater than the WDT delta value. This means the counter must be reloaded within a limited timing window using a specific method. The Watchdog Timer counter can be stopped while the processor is in the debug mode. There is a register write protect function which can be enabled to prevent it from changing the Watchdog Timer configuration unexpectedly.

Real Time Clock – RTC

- 32-Bit up-counter with a programmable prescaler
- Alarm function
- Interrupt and Wake-up event

The Real Time Clock, RTC, includes an APB interface, a 32-bit count-up counter, a control register, a prescaler, a compare register and a status register. Most of the RTC circuits are located in the Backup Domain except for the APB interface. The APB interface is located in the V_{DD15} power domain. Therefore, it is necessary to be isolated from the ISO signal that comes from the power control unit when the V_{DD15} power domain is powered off, that is when the device enters the Power-Down mode. The RTC counter is used as a wakeup timer to generate a system resume signal from the Power-Down mode.

Inter-integrated Circuit – I^2C

- Supports both master and slave modes with a frequency of up to 1 MHz
- Provide an arbitration function and clock synchronisation
- Supports 7-bit and 10-bit addressing modes and general call addressing
- Supports slave multi-addressing mode with maskable address

The I^2C is an internal circuit allowing communication with an external I^2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I^2C module provides three data transfer rates: 1. 100 kHz in the Standard mode, 2. 400 kHz in the Fast mode and 3. 1 MHz in the Fast plus mode. The SCL period generation register is used to setup different kinds of duty cycle implementations for the SCL pulse.

The SDA line which is connected directly to the I^2C bus is a bi-directional data line between the master and slave devices and is used for data transmission and reception. The I^2C also has an arbitration detect function and clock synchronisation to prevent situations where more than one master attempts to transmit data to the I^2C bus at the same time.

Serial Peripheral Interface – SPI

- Supports both master and slave mode
- Frequency of up to (f_{PCLK}/2) MHz for the master mode and (f_{PCLK}/3) MHz for the slave mode
- FIFO Depth: 8 levels
- Multi-master and multi-slave operation

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive function in both master and slave mode. The SPI interface uses 4 pins, which are the serial data input and output lines, MISO and MOSI, the clock line, SCK, and the slave select line, SEL. One SPI device acts as a master device which controls the data flow using the SEL and SCK signals to indicate the start of data communication and the data sampling rate. To receive a data byte, the streamed data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but in a reverse sequence. The mode fault detection provides a capability for multi-master applications.

Universal Synchronous Asynchronous Receiver Transmitter – USART

- Supports both asynchronous and clocked synchronous serial communication modes
- Asynchronous operating baud rate up to (f_{PCLK}/16) MHz and synchronous operating rate up to (f_{PCLK}/8) MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8, or 9-bit character
  - Parity: Even, odd, or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun, and frame error
- Auto hardware flow control mode – RTS, CTS
- IrDA SIR encoder and decoder
- RS485 mode with output enable control
- FIFO Depth: 8 × 9 bits for both receiver and transmitter

The Universal Synchronous Asynchronous Receiver Transceiver, USART, provides a flexible full duplex data exchange using synchronous or asynchronous data transfer. The USART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The USART peripheral function supports four types of interrupt including Line Status Interrupt, Transmitter FIFO Empty Interrupt, Receiver Threshold Level Reaching Interrupt and Time Out Interrupt. The USART module includes a transmitter FIFO, (TX_FIFO) and receiver FIFO (RX_FIFO). The software can detect a USART error status by reading the Line Status Register, LSR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Universal Asynchronous Receiver Transmitter – UART

- Asynchronous serial communication operating baud-rate up to (f_{PCLK}/16) MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8, or 9-bit character
  - Parity: Even, odd, or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun, and frame error

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports Line Status Interrupt. The software can detect a UART error status by reading the Line Status Register, LSR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Smart Card Interface – SCI

- Supports ISO 7816-3 standard
- Character mode
- Single transmit buffer and single receive buffer
- 11-bit ETU (elementary time unit) counter
- 9-bit guard time counter
- 24-bit general purpose waiting time counter
- Parity generation and checking
- Automatic character retry on parity error detection in transmission and reception modes

The Smart Card Interface is compatible with the ISO 7816-3 standard. This interface includes Card Insertion/Removal detection, SCI data transfer control logic and data buffers, internal Timer Counters and corresponding control logic circuits to perform all the necessary Smart Card operations. The Smart Card interface acts as a Smart Card Reader to facilitate communication with the external Smart Card. The overall functions of the Smart Card interface are controlled by a series of registers including control and status registers together with several corresponding interrupts which are generated to get the attention of the microcontroller for SCI transfer status.

Inter-IC Sound – I²S

- Master or slave mode
- Mono and stereo
- I2S-justified, Left-justified and Right-justified mode
- 8/16/24/32-bit sample size with 32-bit channel extended
- 8 × 32-bit TX & RX FIFO with PDMA supported
- 8-bit Fractional Clock Divider with rate control

The I²S is a synchronous communication interface that can be used as a master or slave to exchange data with other audio peripherals, such as ADCs or DACs. The I²S supports a variety of data formats. In addition to the stereo I2S-justified, Left-justified and Right-justified modes, there are mono PCM modes with 8/16/24/32-bit sample size. When the I²S operates in the master mode, then when using the fractional divider, it can provide an accurate sampling frequency output and support the rate control function and fine-tuning of the output frequency to avoid system problems caused by the cumulative frequency error between different devices.

Cyclic Redundancy Check – CRC

- Support CRC16 polynomial: 0x8005,
  $X^{16} + X^{15} + X^2 + 1$
- Support CCITT CRC16 polynomial: 0x1021,
  $X^{16} + X^{12} + X^5 + 1$
- Support IEEE-802.3 CRC32 polynomial: 0x04C11DB7,
  $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Supports 1's complement, byte reverse & bit reverse operation on data and checksum
- Supports byte, half-word & word data size
- Programmable CRC initial seed value
- CRC computation executed in 1 AHB clock cycle for 8-bit data and 4 AHB clock cycles for 32-bit data
- Supports PDMA to complete a CRC computation of a block of memory

The CRC calculation unit is an error detection technique test algorithm which is used to verify data transmission or storage data correctness. A CRC calculation takes a data stream or a block of data as its input and generates a 16- or 32-bit output remainder. Ordinarily, a data stream is suffixed by a CRC code and used as a checksum when being sent or stored. Therefore, the received or restored data stream is calculated by the same generator polynomial as described above. If the new CRC code result does not match the one calculated earlier, then this means that the data stream contains a data error.

Peripheral Direct Memory Access – PDMA

- 6 channels with trigger source grouping
- 8-/16-/32-bit width data transfer
- Supports Address increment, decrement or fixed mode
- 4-level programmable channel priority
- Auto reload mode
- Supports trigger source: ADC, SPI, USART, UART, I^2C, I^2S, GPTM, MCTM, SCI and software request

The Peripheral Direct Memory Access controller, PDMA, moves data between the peripherals and the system memory on the AHB bus. Each PDMA channel has a source address, destination address, block length and transfer count. The PDMA can exclude the CPU intervention and avoid interrupt service routine execution. It improves system performance as the software does not need to connect each data movement operation.

External Bus Interface – EBI

- Programmable interface for various memory types
- Translate the AHB transactions into the appropriate external device protocol
- Individual chip select signal for per memory bank
- Programmable timing to support a wide range of devices
- Automatic translation when AHB transaction width and external memory interface width is different
- Write buffer to decrease the stalling of the AHB write burst transaction
- Multiplexed and non-multiplexed address and data line configurations
  - Up to 21 address lines
  - Up to 16-bit data bus width

The external bus interface is able to access external parallel interface devices such as SRAM, Flash and LCD modules. The interface is memory mapped into the CPU internal address map. The data and address lines are multiplexed in order to reduce the number of pins required to connect to the external devices. The read/write timing of the bus can be adjusted to meet the timing specification of the external devices. Note the interface only supports asynchronous 8 or 16-bit bus interface.

Universal Serial Bus Device Controller – USB

- Complies with USB 2.0 full-speed (12 Mbps) specification
- On-chip USB full-speed transceiver
- 1 control endpoint (EP0) for control transfer
- 3 single-buffered endpoints for bulk and interrupt transfer
- 4 double-buffered endpoints for bulk, interrupt and isochronous transfer
- 1,024 bytes EP_SRAM used as the endpoint data buffers

The USB device controller is compliant with the USB 2.0 full-speed specification. There is one control endpoint known as Endpoint 0 and seven configurable endpoints. A 1024-byte SRAM is used as the endpoint buffer. Each endpoint buffer size is programmable using corresponding registers, which provides maximum flexibility for various applications. The integrated USB full-speed transceiver helps to minimise the overall system complexity and cost. The USB functional block also contains the resume and suspend feature to meet the requirements of low-power consumption.

Debug Support

- Serial Wire Debug Port – SW-DP
- 4 comparators for hardware breakpoint or code / literal patch
- 2 comparators for hardware watchpoints

Package and Operation Temperature

- 33-pin QFN, 48/64-pin LQFP package
- Operation temperature range: -40 °C to +85 °C

3 Overview

Device Information

Table 1. Features and Peripheral List

Peripherals		HT32F52342	HT32F52352
Main Flash (KB)		64	127.5
Option Bytes Flash (KB)		0.5	0.5
SRAM (KB)		8	16
Timers	MCTM	1	
	GPTM	2	
	SCTM	2	
	BFTM	2	
	RTC	1	
	WDT	1	
Communication	USB	1	
	SPI	2	
	USART	2	
	UART	2	
	I²C	2	
	I²S	1	
	SCI (ISO7816-3)	2	
EBI		1	
CRC-16/32		1	
GPIO		Up to 51	
EXTI		16	
12-bit ADC Number of channels		1	
		12 Channels	
Comparator		2	
CPU frequency		Up to 48 MHz	
Operating voltage		2.0 V ~ 3.6 V	
Operating temperature		-40 °C ~ +85 °C	
Package		33-pin QFN, 48/64-pin LQFP	

Block Diagram

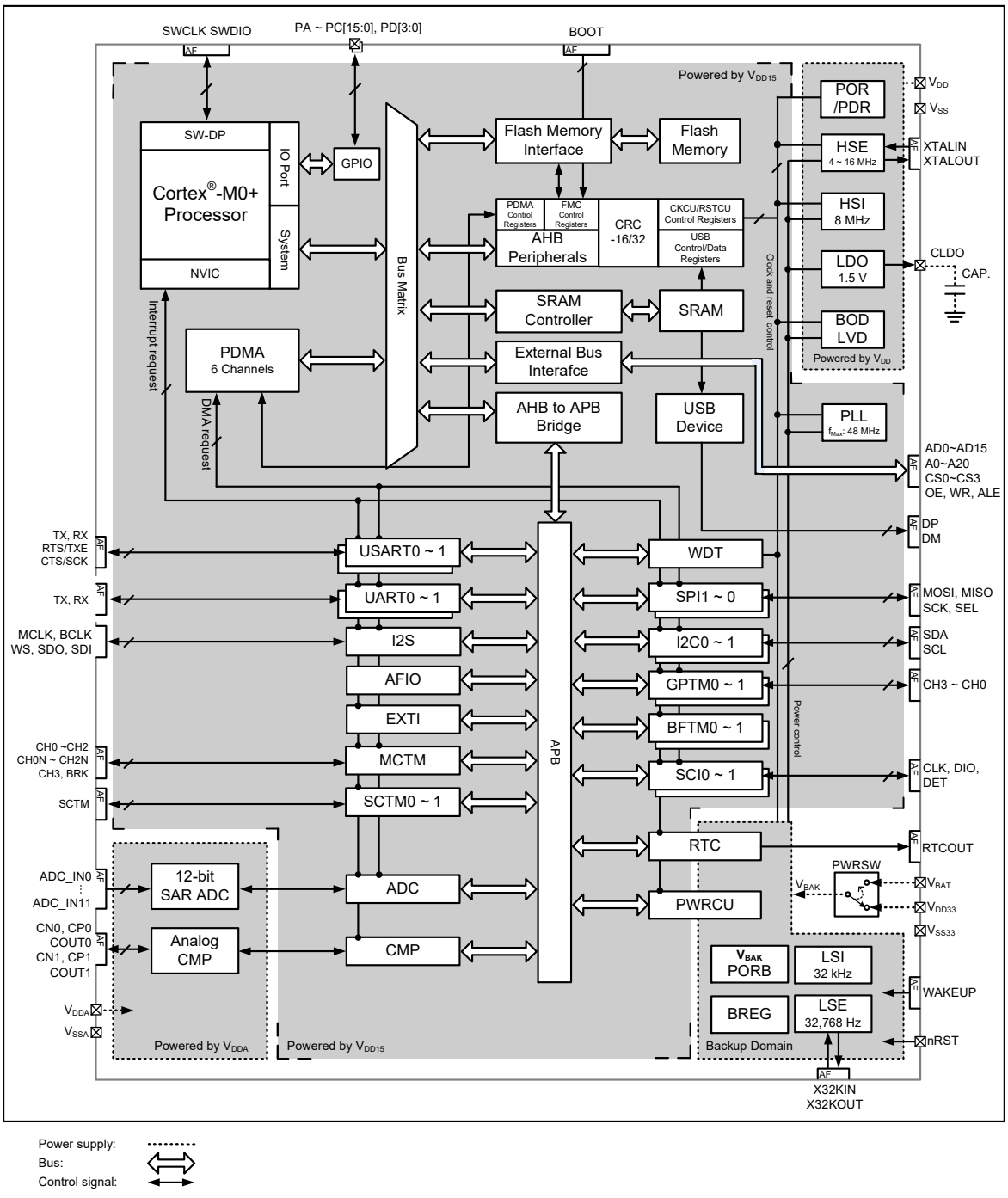


Figure 1. Block Diagram

Memory Map

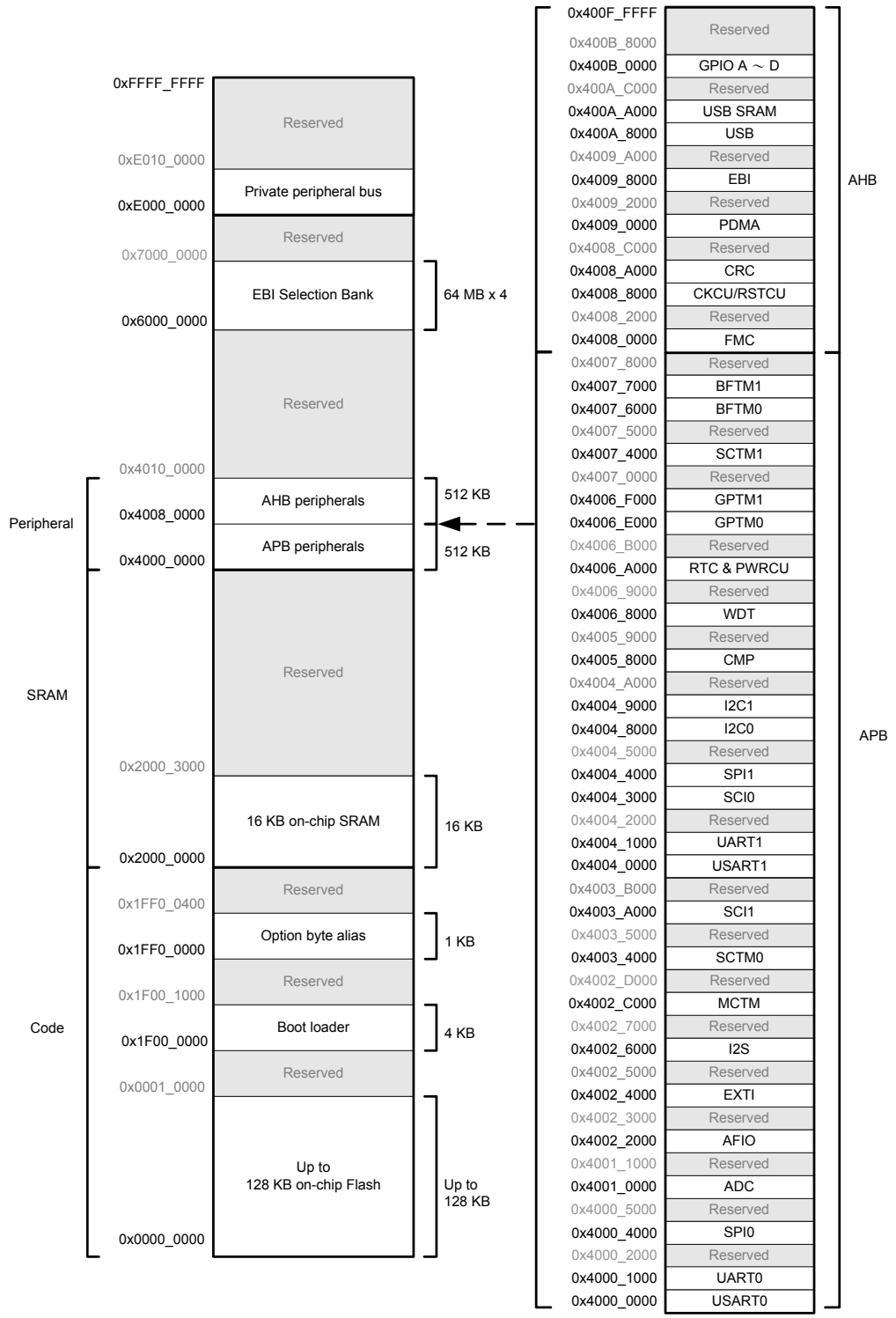


Figure 2. Memory Map

Table 2. Register Map

Start Address	End Address	Peripheral	Bus
0x4000_0000	0x4000_0FFF	USART0	APB
0x4000_1000	0x4000_1FFF	UART0	
0x4000_2000	0x4000_3FFF	Reserved	
0x4000_4000	0x4000_4FFF	SPI0	
0x4000_5000	0x4001_9FFF	Reserved	
0x4001_0000	0x4001_0FFF	ADC	
0x4001_1000	0x4002_1FFF	Reserved	
0x4002_2000	0x4002_2FFF	AFIO	
0x4002_3000	0x4002_3FFF	Reserved	
0x4002_4000	0x4002_4FFF	EXTI	
0x4002_5000	0x4002_BFFF	Reserved	
0x4002_6000	0x4002_6FFF	I^2S	
0x4002_7000	0x4002_BFFF	Reserved	
0x4002_C000	0x4002_CFFF	MCTM	
0x4002_D000	0x4003_3FFF	Reserved	
0x4003_4000	0x4003_4FFF	SCTM0	
0x4003_5000	0x4003_9FFF	Reserved	
0x4003_A000	0x4003_AFFF	SCI1	
0x4003_C000	0x4004_0FFF	Reserved	
0x4004_0000	0x4004_0FFF	USART1	
0x4004_1000	0x4004_1FFF	UART1	
0x4004_2000	0x4004_2FFF	Reserved	
0x4004_3000	0x4004_3FFF	SCI0	
0x4004_4000	0x4004_4FFF	SPI1	
0x4004_5000	0x4004_7FFF	Reserved	
0x4004_8000	0x4004_8FFF	I2C0	
0x4004_9000	0x4004_9FFF	I2C1	
0x4004_A000	0x4005_7FFF	Reserved	
0x4005_8000	0x4005_8FFF	Comparator	
0x4005_9000	0x4006_7FFF	Reserved	
0x4006_8000	0x4006_8FFF	WDT	
0x4006_9000	0x4006_9FFF	Reserved	
0x4006_A000	0x4006_AFFF	RTC/PWRCU	
0x4006_B000	0x4006_DFFF	Reserved	
0x4006_E000	0x4006_EFFF	GPTM0	
0x4006_F000	0x4006_FFFF	GPTM1	
0x4007_0000	0x4007_3FFF	Reserved	
0x4007_4000	0x4007_4FFF	SCTM1	
0x4007_5000	0x4007_5FFF	Reserved	
0x4007_6000	0x4007_6FFF	BFTM0	
0x4007_7000	0x4007_7FFF	BFTM1	
0x4007_8000	0x4007_FFFF	Reserved	

Start Address	End Address	Peripheral	Bus
0x4008_0000	0x4008_1FFF	FMC	AHB
0x4008_2000	0x4008_7FFF	Reserved	
0x4008_8000	0x4008_9FFF	CKCU/RSTCU	
0x4008_A000	0x4008_BFFF	CRC	
0x4008_C000	0x4008_FFFF	Reserved	
0x4009_0000	0x4009_1FFF	PDMA Control Registers	
0x4009_2000	0x400C_BFFF	Reserved	
0x4009_8000	0x4009_9FFF	EBI Control Registers	
0x4009_A000	0x400A_7FFF	Reserved	
0x400A_8000	0x400A_BFFF	USB	
0x400A_C000	0x400A_FFFF	Reserved	
0x400B_0000	0x400B_1FFF	GPIOA	
0x400B_2000	0x400B_3FFF	GPIOB	
0x400B_4000	0x400B_5FFF	GPIOC	
0x400B_6000	0x400B_7FFF	GPIOD	
0x400B_8000	0x400F_FFFF	Reserved	

Clock Structure

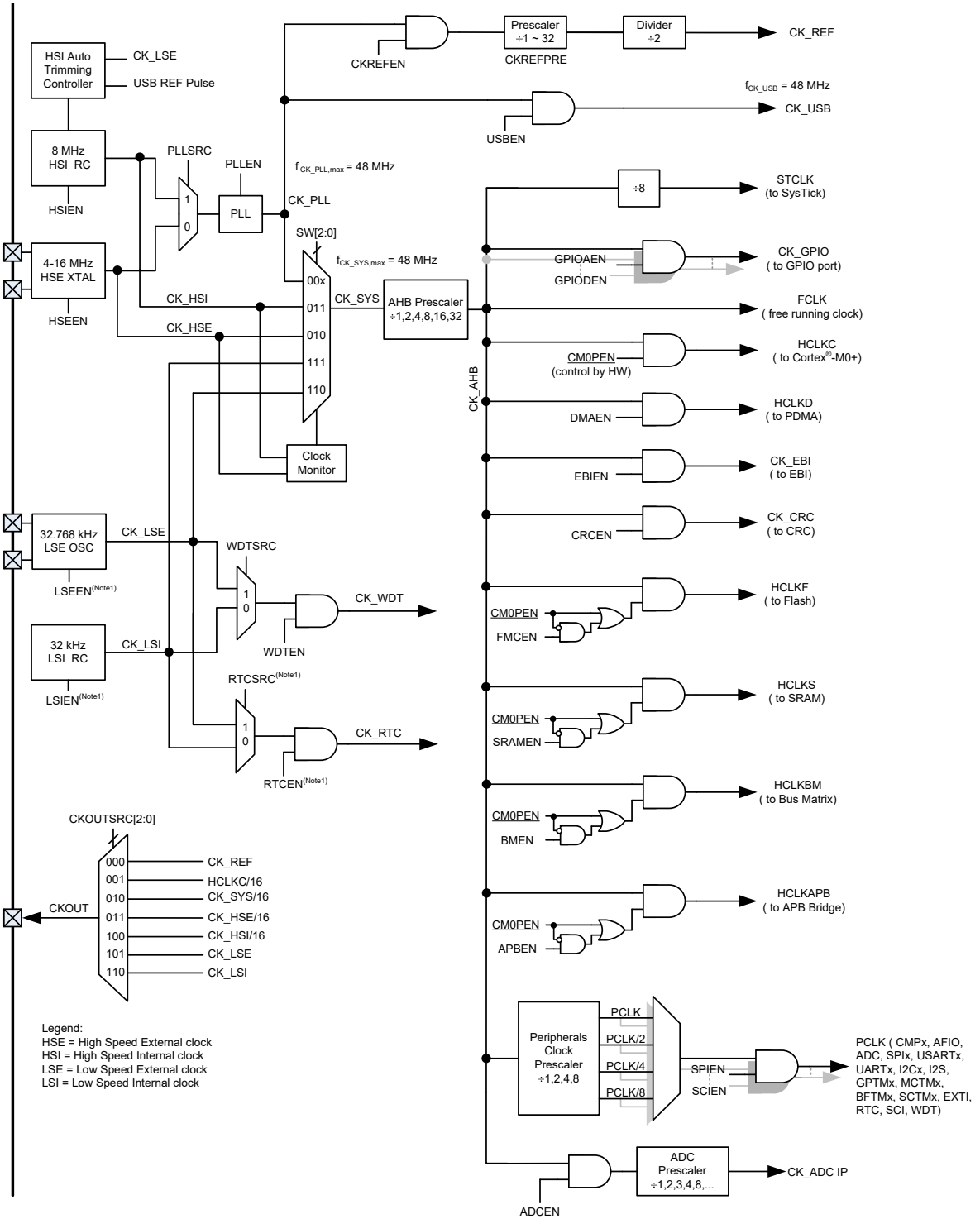


Figure 3. Clock Structure

4 Pin Assignment

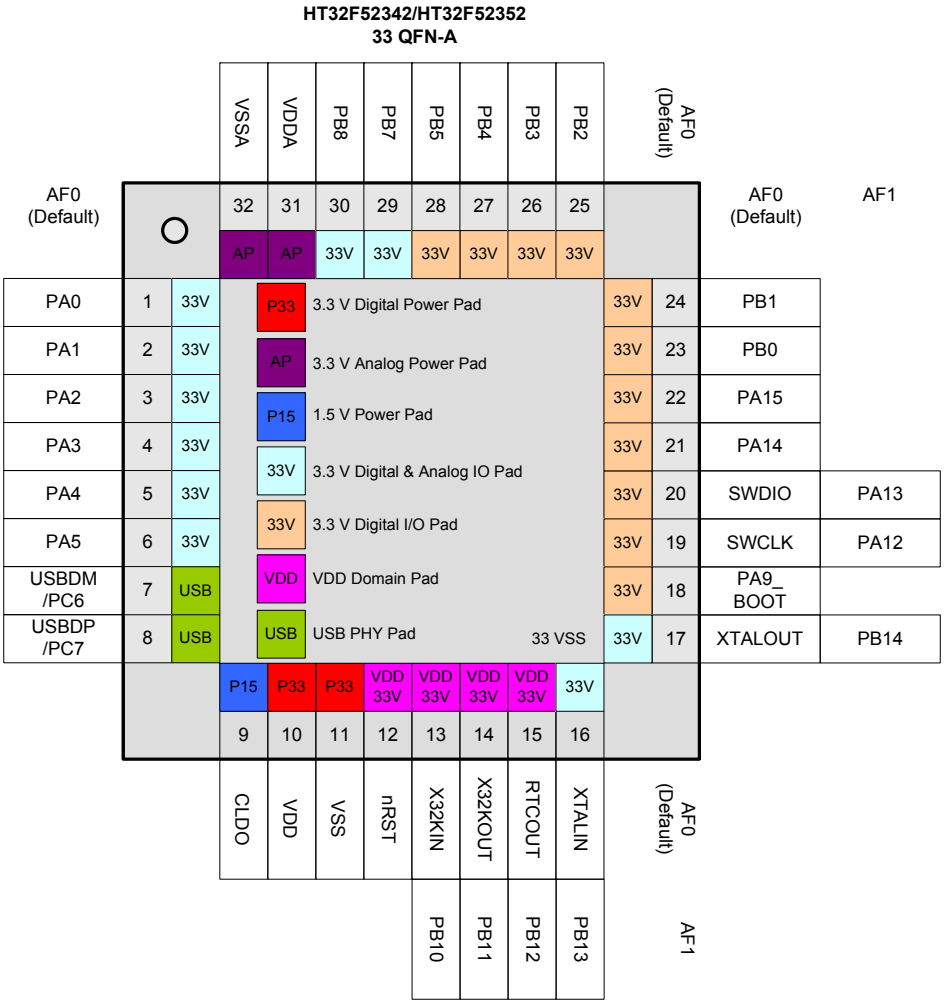


Figure 4. 33-pin QFN Pin Assignment

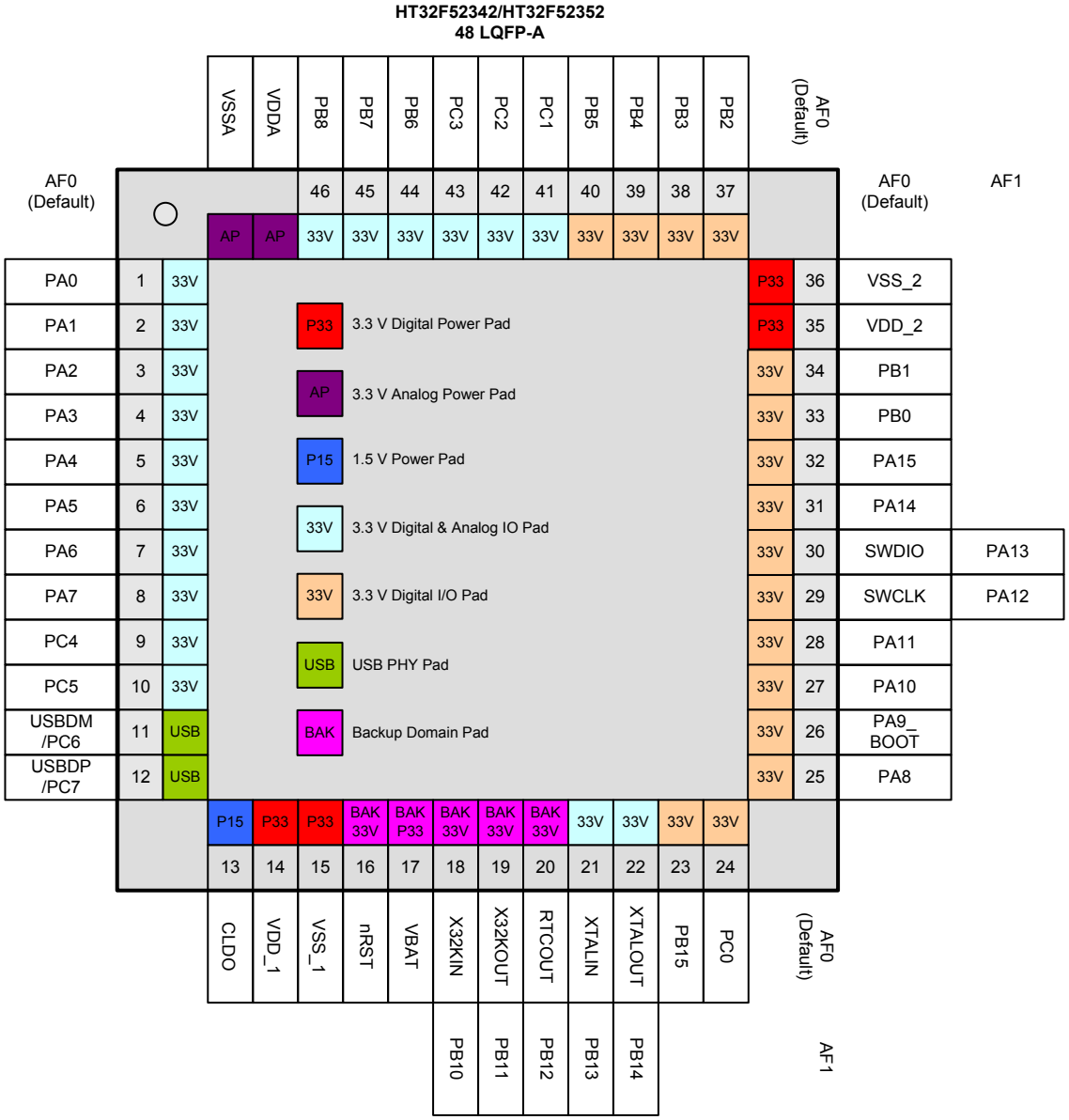


Figure 5. 48-pin LQFP Pin Assignment

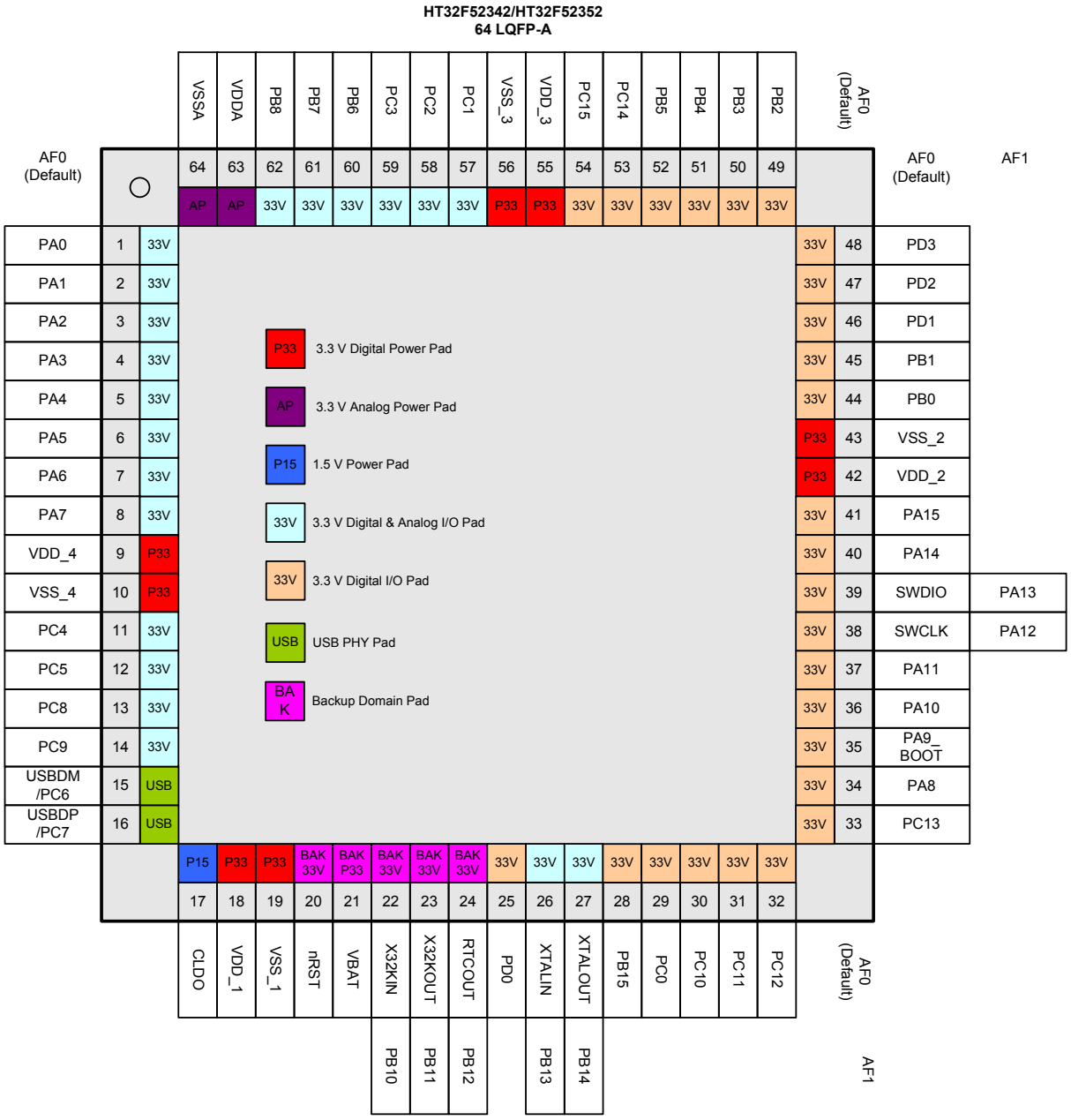


Figure 6. 64-pin LQFP Pin Assignment

Table 3. Pin Assignment for 33-pin QFN, 48/64-pin LQFP Packages

Package			Alternate Function Mapping															
			AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
64 LQFP	48 LQFP	33 QFN	System Default	GPIO	ADC	CMP	MCTM /GPTM	SPI	USART /UART	I²C	SCI	EBI	I2S	N/A	N/A	SCTM	N/A	System Other
1	1	1	PA0		ADC_IN0		GT1_CH0	SPI1_SCK	USR0_RTS	I2C1_SCL	SCI0_CLK		I2S_WS					
2	2	2	PA1		ADC_IN1		GT1_CH1	SPI1_MOSI	USR0_CTS	I2C1_SDA	SCI0_DIO		I2S_BCLK					
3	3	3	PA2		ADC_IN2		GT1_CH2	SPI1_MISO	USR0_TX				I2S_SDO					
4	4	4	PA3		ADC_IN3		GT1_CH3	SPI1_SEL	USR0_RX				I2S_SDI					
5	5	5	PA4		ADC_IN4		GT0_CH0	SPI0_SCK	USR1_TX	I2C0_SCL	SCI1_CLK							
6	6	6	PA5		ADC_IN5		GT0_CH1	SPI0_MOSI	USR1_RX	I2C0_SDA	SCI1_DIO							
7	7		PA6		ADC_IN6		GT0_CH2	SPI0_MISO	USR1_RTS		SCI1_DET							
8	8		PA7		ADC_IN7		GT0_CH3	SPI0_SEL	USR1_CTS				I2S_MCLK					
9			VDD_4															
10			VSS_4															
11	9		PC4		ADC_IN8		GT0_CH0	SPI1_SEL	UR0_TX	I2C1_SCL		EBI_A19				SCTM0		
12	10		PC5		ADC_IN9		GT0_CH1	SPI1_SCK	UR0_RX	I2C1_SDA		EBI_A20				SCTM1		
13			PC8		ADC_IN10		GT0_CH2	SPI1_MOSI				EBI_A0						
14			PC9		ADC_IN11		GT0_CH3	SPI1_MISO				EBI_A1						
15	11	7	PC6				MT_CH2		USR0_TX	I2C0_SCL								
15	11	7	USBDM															
16	12	8	USBDP															
16	12	8	PC7				MT_CH2N		USR0_RX	I2C0_SDA								
17	13	9	CLDO															
18	14	10	VDD_1															
19	15	11	VSS_1															
20	16	12	nRST															
21	17		VBAT															
22	18	13	X32KIN	PB10														
23	19	14	X32KOUT	PB11														
24	20	15	RTCOUT	PB12														WAKEUP
25			PD0							I2C0_SDA		EBI_A18	I2S_SDI			SCTM0		
26	21	16	XTALIN	PB13														
27	22	17	XTALOUT	PB14														
28	23		PB15				MT_CH0	SPI0_SEL	USR1_TX	I2C1_SCL		EBI_A16	I2S_MCLK					
29	24		PC0				MT_CH0N	SPI0_SCK	USR1_RX	I2C1_SDA		EBI_A17						
30			PC10				GT1_CH0	SPI1_SEL				EBI_AD13	I2S_WS					
31			PC11				GT1_CH1	SPI1_SCK				EBI_AD14	I2S_BCLK					
32			PC12				GT1_CH2	SPI1_MOSI	UR1_TX	I2C0_SCL		EBI_AD15	I2S_SDO					
33			PC13				GT1_CH3	SPI1_MISO	UR1_RX	I2C0_SDA		EBI_CS3	I2S_SDI					
34	25		PA8						USR0_TX		SCI1_CLK		I2S_MCLK					
35	26	18	PA9 _BOOT					SPI0_MOSI			SCI1_DIO	EBI_A1	I2S_WS					CKOUT
36	27		PA10				MT_CH1		USR0_RX		SCI0_DET							

Package			Alternate Function Mapping															
			AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
64 LQFP	48 LQFP	33 QFN	System Default	GPIO	ADC	CMP	MCTM /GPTM	SPI	USART /UART	I²C	SCI	EBI	I2S	N/A	N/A	SCTM	N/A	System Other
37	28		PA11				MT_ CH1N	SPI0_ MISO			SCI1_ DET	EBI_ A0	I2S_ MCLK			SCTM0		
38	29	19	SWCLK	PA12														
39	30	20	SWDIO	PA13														
40	31	21	PA14				MT_ CH0	SPI1_ SEL	USR1_ TX	I2C1_ SCL	SCI0_ CLK	EBI_ AD0						
41	32	22	PA15				MT_ CH0N	SPI1_ SCK	USR1_ RX	I2C1_ SDA	SCI0_ DIO	EBI_ AD1				SCTM1		
42			VDD_2															
43			VSS_2															
44	33	23	PB0				MT_ CH1	SPI1_ MOSI	USR0_ TX	I2C0_ SCL		EBI_ AD2						
45	34	24	PB1				MT_ CH1N	SPI1_ MISO	USR0_ RX	I2C0_ SDA		EBI_ AD3						
46			PD1				MT_ CH2		USR1_ RTS		SCI0_ CLK	EBI_ AD10						
47			PD2				MT_ CH2N		USR1_ CTS		SCI0_ DIO	EBI_ AD11						
48			PD3				MT_ CH3				SCI0_ DET	EBI_ AD12						
	35		VDD_2															
	36	33	VSS_2															
49	37	25	PB2				MT_ CH2	SPI0_ SEL	UR0_ TX			EBI_ AD4						
50	38	26	PB3				MT_ CH2N	SPI0_ SCK	UR0_ RX			EBI_ AD5				SCTM1		
51	39	27	PB4				MT_ BRK	SPI0_ MOSI	UR1_ TX			EBI_ AD6				SCTM0		
52	40	28	PB5				MT_ BRK	SPI0_ MISO	UR1_ RX			EBI_ AD7						
53			PC14				MT_ CH3			I2C0_ SCL		EBI_ AD8						
54			PC15							I2C0_ SDA		EBI_ AD9				SCTM1		
55			VDD_3															
56			VSS_3															
57	41		PC1			CN0	MT_ CH0	SPI1_ SEL	UR1_ TX			EBI_ OE	I2S_ MCLK					
58	42		PC2			CP0	MT_ CH0N	SPI1_ SCK				EBI_ CS0						
59	43		PC3			COUT0		SPI1_ MOSI	UR1_ RX			EBI_ WE						
60	44		PB6			CN1	MT_ CH2	SPI1_ MISO	UR0_ TX		SCI1_ CLK	EBI_ ALE	I2S_ BCLK					
61	45	29	PB7			CP1	MT_ CH2N			I2C1_ SCL	SCI1_ DET	EBI_ CS1	I2S_ SDO					
62	46	30	PB8			COUT1	MT_ CH3		UR0_ RX	I2C1_ SDA	SCI1_ DIO	EBI_ CS2	I2S_SDI					
63	47	31	VDDA															
64	48	32	VSSA															

Table 4. Pin Description

Pin Number			Pin Name	Type (Note1)	I/O Structure (Note2)	Output Driving	Description
64LQFP	48LQFP	33QFN					Default Function (AF0)
1	1	1	PA0	AI/O	33V	4/8/12/16 mA	PA0
2	2	2	PA1	AI/O	33V	4/8/12/16 mA	PA1
3	3	3	PA2	AI/O	33V	4/8/12/16 mA	PA2
4	4	4	PA3	AI/O	33V	4/8/12/16 mA	PA3
5	5	5	PA4	AI/O	33V	4/8/12/16 mA	PA4
6	6	6	PA5	AI/O	33V	4/8/12/16 mA	PA5
7	7		PA6	AI/O	33V	4/8/12/16 mA	PA6
8	8		PA7	AI/O	33V	4/8/12/16 mA	PA7
9	—		VDD_4	P	—	—	Voltage for digital I/O
10	—		VSS_4	P	—	—	Ground reference for digital I/O
11	9		PC4	AI/O	33V	4/8/12/16 mA	PC4
12	10		PC5	AI/O	33V	4/8/12/16 mA	PC5
13	—		PC8	AI/O	33V	4/8/12/16 mA	PC8
14	—		PC9	AI/O	33V	4/8/12/16 mA	PC9
15	11	7	PC6	I/O	33V	4/8/12/16 mA	PC6
15	11	7	USBDM	AI/O	—	—	USB Differential data bus conforming to the Universal Serial Bus standard.
16	12	8	USBDP	AI/O	—	—	USB Differential data bus conforming to the Universal Serial Bus standard.
16	12	8	PC7	I/O	33V	4/8/12/16 mA	PC7
17	13	9	CLDO	P	—	—	Core power LDO 1.5 V output. It is recommended to connect a 2.2 μF capacitor as close as possible between this pin and VSS_1.
18	14	10	VDD_1	P	—	—	Voltage for digital I/O
19	15	11	VSS_1	P	—	—	Ground reference for digital I/O
20	16	12	nRST	I(BK)	33V_PU	—	External reset pin and external wakeup pin in the Power-Down mode
21	17		VBAT	P	—	—	Battery power input for the backup domain
22	18	13	PB10(4)	AI/O(BK)	33V	< 2 mA	X32KIN
23	19	14	PB11(4)	AI/O(BK)	33V	< 2 mA	X32KOUT
24	20	15	PB12(4)	I/O(BK)	33V	< 2 mA	RTCOUT
25	—		PD0	I/O	33V	4/8/12/16 mA	PD0
26	21	16	PB13	AI/O	33V	4/8/12/16 mA	XTALIN
27	22	17	PB14	AI/O	33V	4/8/12/16 mA	XTALOUT
28	23		PB15	I/O	33V	4/8/12/16 mA	PB15
29	24		PC0	I/O	33V	4/8/12/16 mA	PC0
30	—		PC10	I/O	33V	4/8/12/16 mA	PC10
31	—		PC11	I/O	33V	4/8/12/16 mA	PC11
32	—		PC12	I/O	33V	4/8/12/16 mA	PC12
33	—		PC13	I/O	33V	4/8/12/16 mA	PC13
34	25		PA8	I/O	33V_PU	4/8/12/16 mA	PA8

Pin Number			Pin Name	Type (Note1)	I/O Structure (Note2)	Output Driving	Description
64LQFP	48LQFP	33QFN					Default Function (AF0)
35	26	18	PA9	I/O	33V_PU	4/8/12/16 mA	PA9_BOOT
36	27		PA10	I/O	33V	4/8/12/16 mA	PA10
37	28		PA11	I/O	33V	4/8/12/16 mA	PA11
38	29	19	PA12	I/O	33V_PU	4/8/12/16 mA	SWCLK
39	30	20	PA13	I/O	33V_PU	4/8/12/16 mA	SWDIO
40	31	21	PA14	I/O	33V	4/8/12/16 mA	PA14
41	32	22	PA15	I/O	33V	4/8/12/16 mA	PA15
42	—		VDD_2	P	—	—	Voltage for digital I/O
43	—		VSS_2	P	—	—	Ground reference for digital I/O
44	33	23	PB0	I/O	33V	4/8/12/16 mA	PB0
45	34	24	PB1	I/O	33V	4/8/12/16 mA	PB1
46	—		PD1	I/O	33V	4/8/12/16 mA	PD1
47	—		PD2	I/O	33V	4/8/12/16 mA	PD2
48	—		PD3	I/O	33V	4/8/12/16 mA	PD3
—	35		VDD_2	P	—	—	Voltage for digital I/O
—	36	33	VSS_2	P	—	—	Ground reference for digital I/O
49	37	25	PB2	I/O	33V	4/8/12/16 mA	PB2
50	38	26	PB3	I/O	33V	4/8/12/16 mA	PB3
51	39	27	PB4	I/O	33V	4/8/12/16 mA	PB4
52	40	28	PB5	I/O	33V	4/8/12/16 mA	PB5
53	—		PC14	I/O	33V	4/8/12/16 mA	PC14
54	—		PC15	I/O	33V	4/8/12/16 mA	PC15
55	—		VDD_3	P	—	—	Voltage for digital I/O
56	—		VSS_3	P	—	—	Ground reference for digital I/O
57	41		PC1	AI/O	33V	4/8/12/16 mA	PC1
58	42		PC2	AI/O	33V	4/8/12/16 mA	PC2
59	43		PC3	AI/O	33V	4/8/12/16 mA	PC3
60	44		PB6	AI/O	33V	4/8/12/16 mA	PB6
61	45	29	PB7	AI/O	33V	4/8/12/16 mA	PB7
62	46	30	PB8	AI/O	33V	4/8/12/16 mA	PB8
63	47	31	VDDA	P	—	—	Analog voltage for ADC and Comparator64
64	48	32	VSSA	P	—	—	Ground reference for the ADC and Comparator

Note: 1. I = input, O = output, A = Analog port, P = power supply, PU = pull-up, BK = Back-up domain

2. 33V = 3.3 V tolerant.

3. The GPIOs are in an AF0 state after a V_{DD15} power on reset (POR) except for the RTCOUT pin in the Backup Domain I/O. The RTCOUT pin is reset by the Backup Domain power-on-reset (PORB) or by the Backup Domain software reset (BAK_RST bit in BAK_CR register).

4. The backup domain of the I/O pins have a source current capability limitation of < 2 mA @ $V_{DD} = 3.3$ V. The typical sink current is 4/8 mA configurable @ $V_{DD} = 3.3$ V.

5 Electrical Characteristics

Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}	External main supply voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External analog supply voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{BAT}	External battery supply voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{IN}	Input voltage on I/O	V_{SS} - 0.3	V_{DD} + 0.3	V
T_A	Ambient operating temperature range	-40	+85	°C
T_{STG}	Storage temperature range	-55	+150	°C
T_J	Maximum junction temperature	—	125	°C
P_D	Total power dissipation	—	500	mW
V_{ESD}	Electrostatic discharge voltage - human body mode	-4000	+4000	V

Recommended DC Operating Conditions

Table 6. Recommended DC Operating Conditions

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	I/O operating voltage		2.0	3.3	3.6	V
V_{DDA}	Analog operating voltage		2.5	3.3	3.6	V
V_{BAT}	Battery supply operating voltage		2.0	3.3	3.6	V

On-Chip LDO Voltage Regulator Characteristics

Table 7. LDO Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LDO}	Internal regulator output voltage	V_{DD} ≥ 2.0 V Regulator input @ I_{LDO} = 35 mA and voltage variant = ±5 %, after trimming.	1.425	1.5	1.57	V
I_{LDO}	Output current	V_{DD} = 2.0 V Regulator input @ V_{LDO} = 1.5 V	—	35	—	mA
C_{LDO}	External filter capacitor value for internal core power supply	The capacitor value is dependent upon the core power current consumption	—	2.2	—	μF

Power Consumption

Table 8. Power Consumption Characteristics

Symbol	Parameter	Conditions	Typ	Max		Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	
I_{DD}	Supply current (Run mode)	V_{DD} = V_{BAT} = 3.3 V, HSI = 8 MHz, PLL = 48 MHz, f_{CPU} = 48 MHz, f_{BUS} = 48 MHz, all peripherals enabled	20	22.1	—	mA
		V_{DD} = V_{BAT} = 3.3 V, HSI = 8 MHz, PLL = 48 MHz, f_{CPU} = 48 MHz, f_{BUS} = 48 MHz, all peripherals disabled	10.1	11.6	—	
		V_{DD} = V_{BAT} = 3.3 V, HSI off, PLL off, LSI on, f_{CPU} = 32 kHz, f_{BUS} = 32 kHz, all peripherals enabled	44	55	—	µA
		V_{DD} = V_{BAT} = 3.3 V, HSI off, PLL off, LSI on, f_{CPU} = 32 kHz, f_{BUS} = 32 kHz, all peripherals disabled	40	51	—	
	Supply current (Sleep mode)	V_{DD} = V_{BAT} = 3.3 V, HSI = 8 MHz, PLL = 48 MHz, f_{CPU} = 0 MHz, f_{BUS} = 48 MHz, all peripherals enabled	12	13.8	—	mA
		V_{DD} = V_{BAT} = 3.3 V, HSI = 8 MHz, PLL = 48 MHz, f_{CPU} = 0 MHz, f_{BUS} = 48 MHz, all peripherals disabled	2	2.3	—	
	Supply current (Deep-Sleep1 mode)	V_{DD} = V_{BAT} = 3.3 V, All clock off (HSE/ HSI/PLL/LSE), LDO in low power mode, LSI on, RTC on	34	43.8	—	µA
	Supply current (Deep-Sleep2 mode)	V_{DD} = V_{BAT} = 3.3 V, All clock off (HSE/ HSI/PLL/LSE), LDO off, DMOS on, LSI on, RTC on	5	12	—	
	Supply current (Power-Down mode)	V_{DD} = V_{BAT} = 3.3 V, LDO off, DMOS off, LSE off, LSI on, RTC on	1.85	2.75	—	
		V_{DD} = V_{BAT} = 3.3 V, LDO off, DOMS off, LSE off, LSI on, RTC off	1.80	2.67	—	
I_{BAT}	Battery supply current (Power-Down mode)	V_{DD} not present, V_{BAT} = 3.3 V, LDO off, DMOS off, LSE off, LSI on, RTC on	1.36	2	—	
		V_{DD} not present, V_{BAT} = 3.3 V, LDO off, DMOS off, LSE off, LSI on, RTC off	1.36	2	—	

Note: 1. HSE means high speed external oscillator. HSI means 8 MHz high speed internal oscillator.
2. LSE means 32.768 kHz low speed external oscillator. LSI means 32 kHz low speed internal oscillator.
3. RTC means real time clock.
4. Code = while (1) { 208 NOP } executed in Flash.
5. f_{BUS} means f_{HCLK} and f_{PCLK}.

Reset and Supply Monitor Characteristics

Table 9. V_{DD} Power Reset Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{POR}	Power on reset threshold (Rising Voltage on V_{DD})	T_A = -40 °C~ +85 °C	1.66	1.79	1.90	V
V_{PDR}	Power down reset threshold (Falling Voltage on V_{DD})		1.49	1.64	1.78	V
$V_{PORHYST}$	POR hysteresis	—	—	150	—	mV
t_{POR}	Reset delay time	V_{DD} = 3.3 V	—	0.1	0.2	ms

Note: 1. Data based on characterisation results only, not tested in production.
2. Guaranteed by design, not tested in production.
3. If the LDO is turned on, the VDD POR has to be in the de-assertion condition. When the VDD POR is in the assertion state then the LDO will be turned off.

Table 10. LVD/BOD Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BOD}	Voltage of Brown Out Detection	T_A = -40 °C~ 85 °C After factory-trimmed (V_{DD} Falling edge)		2.02	2.1	2.18	V
V_{LVD}	Voltage of Low Voltage Detection	T_A = -40 °C~ 85 °C (V_{DD} Falling edge)	LVDS = 000	2.17	2.25	2.33	V
			LVDS = 001	2.32	2.4	2.48	V
			LVDS = 010	2.47	2.55	2.63	V
			LVDS = 011	2.62	2.7	2.78	V
			LVDS = 100	2.77	2.85	2.93	V
			LVDS = 101	2.92	3.0	3.08	V
			LVDS = 110	3.07	3.15	3.23	V
			LVDS = 111	3.22	3.3	3.38	V
$V_{LVDHTST}$	LVD hysteresis	V_{DD} = 3.3 V	—	—	100	—	mV
t_{suLVD}	LVD Setup time	V_{DD} = 3.3 V	—	—	—	5	μs
t_{atLVD}	LVD active delay time	V_{DD} = 3.3 V	—	—	—	—	μs
I_{DDLVD}	Operation current NOTE3	V_{DD} = 3.3 V	—	—	5	15	μA

Note: 1. Data based on characterisation results only, not tested in production.
2. Guaranteed by design, not tested in production.
3. Bandgap current is not included.
4. LVDS field is in the PWRCU LVDCSR register

External Clock Characteristics

Table 11. High Speed External Clock (HSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Operation Range	—	2.0	—	3.6	V
f_{HSE}	High Speed External oscillator frequency (HSE)	—	4	—	16	MHz
C_{LHSE}	Load capacitance	V_{DD} = 3.3 V, R_{ESR} = 100 Ω @ 16 MHz	—	—	22	pF
R_{FHSE}	Internal feedback resistor between XTALIN and XTALOUT pins	—	—	1	—	MΩ
R_{ESR}	Equivalent Series Resistance*	V_{DD} = 3.3 V, C_L = 12 pF @ 16 MHz, HSEDR = 0	—	—	160	Ω
		V_{DD} = 2.4 V, C_L = 12 pF @ 16 MHz, HSEDR = 1				
D_{HSE}	HSE oscillator Duty cycle	—	40	—	60	%
I_{DDHSE}	HSE oscillator current consumption	V_{DD} = 3.3 V @ 16 MHz	—	TBD	—	mA
I_{PWDHSE}	HSE oscillator power down current	V_{DD} = 3.3 V	—	—	0.01	μA
t_{SUHSE}	HSE oscillator startup time	V_{DD} = 3.3 V	—	—	4	ms

Table 12. Low Speed External Clock (LSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAK}	Operation Range	—	2.0	—	3.6	V
f_{CK_LSE}	LSE Frequency	V_{BAK} = 2.0 V ~ 3.6 V	—	32.768	—	kHz
R_F	Internal feedback resistor	—	—	10	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{BAK} = 3.3 V	30	—	TBD	KΩ
C_L	Recommended load capacitances	V_{BAK} = 3.3 V	6	—	TBD	pF
I_{DDLSE}	Oscillator supply current (High current mode)	f_{CK_LSE} = 32.768 kHz, R_{ESR} = 50 kΩ, C_L ≥ 7 pF, V_{BAK} = 2.0 V ~ 2.7 V, T_A = -40 °C ~ +85 °C	—	3.3	6.3	μA
	Oscillator supply current (Low current mode)	f_{CK_LSE} = 32.768 kHz, R_{ESR} = 50 kΩ, C_L < 7 pF, V_{BAK} = 2.0 V ~ 3.6 V, T_A = -40 °C ~ +85 °C	—	1.8	3.3	μA
	Power down current	—	—	—	0.01	μA
t_{suLSE}	Startup time (Low current mode)	f_{CK_LSI} = 32.768 kHz, V_{BAK} = 2.0 V ~ 3.6 V	500	—	—	ms

Note: The following guidelines are recommended to increase the stability of the crystal circuit of the HSE / LSE clock in the PCB layout:

1. The crystal oscillator should be located as close as possible to the MCU to keep the trace lengths as short as possible to reduce any parasitic capacitance.
2. Shield lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
3. Keep any high frequencysignal lines away from the crystal area to prevent any crosstalk adverse effects.

Internal Clock Characteristics

Table 13. High Speed Internal Clock (HSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Operation Range		2.0		3.6	V
f_{HSI}	HSI Frequency	V_{DD} = 3.3 V @ 25 °C	—	8	—	MHz
ACC_{HSI}	Factory calibrated HSI oscillator frequency accuracy	V_{DD} = 3.3 V, T_A = 25 °C	-2	—	2	%
		V_{DD} = 2.5 V ~ 3.6 V, T_A = -40 °C ~ +85 °C	-3	—	3	%
		V_{DD} = 2.0 V ~ 3.6 V T_A = -40 °C ~ +85 °C	-4	—	4	%
Duty	Duty cycle	f_{HSI} = 8 MHz	35	—	65	%
I_{DDHSI}	Oscillator supply current	f_{HSI} = 8 MHz	—	300	500	μA
	Power down current		—	—	0.05	μA
t_{suHSI}	Startup time	f_{HSI} = 8 MHz	—	—	10	μs

Table 14. Low Speed Internal Clock (LSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Low Speed Internal Oscillator Frequency (LSI)	V_{DD} = 3.3 V, T_A = -40 °C ~ +85 °C	21	32	43	kHz
ACC_{LSI}	LSI Frequency accuracy	After factory-trimmed, V_{DD} = 3.3 V, T_A = 25 °C	-10	—	+10	%
I_{DDLSI}	LSI Oscillator Operating current	V_{DD} = 3.3 V, T_A = 25 °C	—	0.4	0.8	μA
t_{SULSI}	LSI Oscillator startup time	V_{DD} = 3.3 V, T_A = 25 °C	—	—	100	μs

PLL Characteristics

Table 15. PLL Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}	PLL input clock	—	4	—	16	MHz
f_{CK_PLL}	PLL output clock	—	16	—	48	MHz
t_{LOCK}	PLL lock time	—	—	200	—	μs

Memory Characteristics

Table 16. Flash Memory Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{ENDU}	Number of guaranteed program/erase cycles before failure. (Endurance)	T_A = -40 °C ~ +85 °C	10	—	—	K cycles
t_{RET}	Data retention time	T_A = -40 °C ~ +85 °C	10	—	—	Years
t_{PROG}	Word programming time	T_A = -40 °C ~ +85 °C	20	—	—	μs
t_{ERASE}	Page erase time	T_A = -40 °C ~ +85 °C	2	—	—	ms
t_{MERASE}	Mass erase time	T_A = -40 °C ~ +85 °C	10	—	—	ms

I/O Port Characteristics

Table 17. I/O Port Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{IL}	Low level input current	3.3 V I/O	V_I = V_{SS}, On-chip pull-up resister disabled.	—	—	3	μA
		Reset pin		—	—	3	μA
I_{IH}	High level input current	3.3 V I/O	V_I = V_{DD}, On-chip pull-down resister disabled.	—	—	3	μA
		Reset pin		—	—	3	μA
V_{IL}	Low level input voltage	3.3 V I/O		-0.5	—	V_{DD} × 0.35	V
		Reset pin		-0.5	—	V_{DD} × 0.35	V
V_{IH}	High level input voltage	3.3 V I/O		V_{DD} × 0.65	—	V_{DD} + 0.5	V
		Reset pin		V_{DD} × 0.65	—	V_{DD} + 0.5	V
V_{HYS}	Schmitt trigger input voltage hysteresis	3.3 V I/O		—	0.12 × V_{DD}	—	mV
		Reset pin		—	0.12 × V_{DD}	—	mV

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{OL}	Low level output current (GPIO Sink current)	3.3 V I/O 4 mA drive, V_{OL} = 0.4 V		4	—	—	mA
		3.3 V I/O 8 mA drive, V_{OL} = 0.4 V		8	—	—	mA
		3.3 V I/O 12 mA drive, V_{OL} = 0.4 V		12	—	—	mA
		3.3 V I/O 16 mA drive, V_{OL} = 0.4 V		16	—	—	mA
		Backup Domain I/O drive @ V_{DD} = 3.3 V, V_{OL} = 0.4 V, PB10, PB11, PB12		4	—	—	mA
I_{OH}	High level output current (GPIO Source current)	3.3 V I/O 4 mA drive, V_{OH} = V_{DD} - 0.4 V		4	—	—	mA
		3.3 V I/O 8 mA drive, V_{OH} = V_{DD} - 0.4 V		8	—	—	mA
		3.3 V I/O 12 mA drive, V_{OH} = V_{DD} - 0.4 V		12	—	—	mA
		3.3 V I/O 16 mA drive, V_{OH} = V_{DD} - 0.4 V		16	—	—	mA
		Backup Domain I/O drive @ V_{DD} = 3.3 V, V_{OL} = V_{DD} - 0.4 V, PB10, PB11, PB12.		—	—	2	mA
V_{OL}	Low level output voltage	3.3 V 4 mA drive I/O, I_{OL} = 4 mA		—	—	0.4	V
		3.3 V 8 mA drive I/O, I_{OL} = 8 mA		—	—	0.4	V
		3.3 V 12 mA drive I/O, I_{OL} = 12 mA		—	—	0.4	V
		3.3 V 16 mA drive I/O, I_{OL} = 16 mA		—	—	0.4	V
		Backup Domain I/O Sink Current = 4 mA (Low driving strength)	V_{DD} = 2.7 V~3.6 V	—	—	0.4	V
			V_{DD} = 2.0 V~2.7 V	—	—	0.6	V
		Backup Domain I/O Sink Current = 8 mA (High driving strength)	V_{DD} = 2.7 V~3.6 V	—	—	0.4	V
			V_{DD} = 2.0 V~2.7 V	—	—	0.6	V
V_{OH}	High level output voltage	3.3 V 4 mA drive I/O, I_{OH} = 4 mA		V_{DD} - 0.4	—	—	V
		3.3 V 8 mA drive I/O, I_{OH} = 8 mA		V_{DD} - 0.4	—	—	V
		3.3 V 12 mA drive I/O, I_{OL} = 12 mA		V_{DD} - 0.4	—	—	V
		3.3 V 16 mA drive I/O, I_{OL} = 16 mA		V_{DD} - 0.4	—	—	V
		Backup Domain I/O Source Current = 2mA	V_{DD} = 2.7 V~3.6 V	2.4	—	—	V
		Backup Domain I/O Source Current = 1mA	V_{DD} = 2.0 V~2.7 V	V_{DD} - 0.4	—	—	V
R_{PU}	Internal pull-up resistor	3.3 V I/O		—	46	—	kΩ
R_{PD}	Internal pull-down resistor	3.3 V I/O		—	46	—	kΩ

ADC Characteristics

Table 18. ADC Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	—	2.5	3.3	3.6	V
V_{ADCIN}	A/D Converter input voltage range	—	0	—	V_{REF+}	V
V_{REF+}	A/D Converter Reference voltage	—	—	V_{DDA}	V_{DDA}	V
I_{ADC}	Current consumption	V_{DDA} = 3.3 V	—	1	TBD	mA
I_{ADC_DN}	Power down current consumption	V_{DDA} = 3.3 V	—	—	0.1	μA
f_{ADC}	A/D Converter clock	—	0.7	—	16	MHz
f_S	Sampling rate	—	0.05	—	1	MHz
t_{DL}	Data latency	—	—	12.5	—	$1/f_{ADC}$ Cycles
$t_{S\&H}$	Sampling & hold time	—	—	3.5	—	$1/f_{ADC}$ Cycles
$t_{ADCCONV}$	A/D Converter conversion time	—	—	16	—	$1/f_{ADC}$ Cycles
R_I	Input sampling switch resistance	—	—	—	1	kΩ
C_I	Input sampling capacitance	No pin/pad capacitance included	—	16	—	pF
t_{SU}	Startup up time	—	—	—	1	μs
N	Resolution	—	—	12	—	bits
INL	Integral Non-linearity error	f_S = 750 kHz, V_{DDA} = 3.3 V	—	±2	±5	LSB
DNL	Differential Non-linearity error	f_S = 750 kHz, V_{DDA} = 3.3 V	—	±1		LSB
E_O	Offset error	—	—	—	±10	LSB
E_G	Gain error	—	—	—	±10	LSB

Note: 1. Guaranteed by design, not tested in production.

2. The figure below shows the equivalent circuit of the A/D Converter Sample-and-Hold input stage where C_I is the storage capacitor, R_I is the resistance of the sampling switch and R_S is the output impedance of the signal source V_S. Normally the sampling phase duration is approximately, $3.5/f_{ADC}$. The capacitance, C_I, must be charged within this time frame and it must be ensured that the voltage at its terminals becomes sufficiently close to V_S for accuracy. To guarantee this, R_S is not allowed to have an arbitrarily large value.

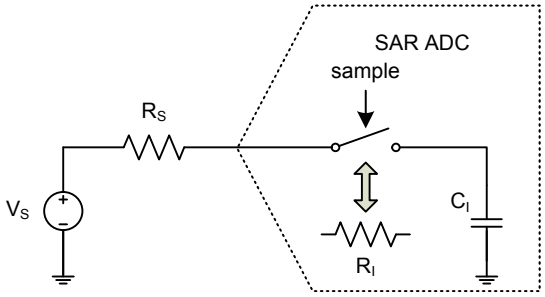


Figure 7. ADC Sampling Network Model

The worst case occurs when the extremities of the input range (0V and V_{REF}) are sampled consecutively. In this situation a sampling error below ¼ LSB is ensured by using the following equation:

$$R_S < \frac{3.5}{f_{ADC} C_I \ln(2^{N+2})} - R_I$$

Where f_{ADC} is the ADC clock frequency and N is the ADC resolution (N = 12 in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model.

If, in a system where the A/D Converter is used, there are no rail-to-rail input voltage variations between consecutive sampling phases, R_S may be larger than the value indicated by the equation above.

Comparator Characteristics

Table 19. Comparator Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Operating voltage	Comparator mode		2.4	3.3	3.6	V
V_{IN}	Input Common Mode Voltage Range	CP or CN		V_{SSA}	—	V_{DDA}	V
V_{IOS}	Input offset voltage(1)	T_A = 25 °C		-15	—	15	mV
V_{hys}	Input Hysteresis	No hysteresis (CMPnHM [1:0] = 00)		—	0	—	mV
		Low hysteresis (CMPnHM [1:0] = 01)		—	30	—	mV
		Middle hysteresis (CMPnHM [1:0] = 10)		—	70	—	mV
		High hysteresis (CMPnHM [1:0] = 11)		—	100	—	mV
t_{RT}	Response time Input Overdrive = ±100mV	High Speed mode	$V_{DDA} \geq 2.7$ V	—	50	100	ns
			$V_{DDA} < 2.7$ V	—	100	250	
		Low Speed mode		—	2	5	µs
I_{CMP}	Current Consumption V_{DDA} = 3.3 V	High Speed mode		—	130	—	µA
		Low Speed mode		—	30	—	µA
t_{CMPST}	Comparator Startup Time	Comparator enabled to output valid.		—	—	50	µs
I_{CMP_DN}	Power Down Supply Current	CMPEN = 0 CVREFEN = 0 CVREFOE=0		—	—	0.1	µA
Comparator Voltage Reference (CVR)							
V_{CVR}	Output Range			V_{SSA}	—	V_{DDA}	V
N_{Bits}	CVR Scaler Resolution				6		bits
t_{CVRST}	Setting Time	CVR scaler setting time from CVREF = “000000” to “111111”		—	—	100	µs
I_{CVR}	Current Consumption V_{DDA} = 3.3 V	CVREFEN=1, CMPREFOE=0		—	65	—	µA
		CVREFEN=1, CVREFOE=1		—	80	110	µA

Note: Guaranteed by design, not tested in production.

SCTM/GPTM/MCTM Characteristics

Table 20. SCTM/GPTM/MCTM Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{TM}	Timer clock source for GPTM and MCTM	—	—	—	48	MHz
t_{RES}	Timer resolution time	—	1	—	—	f_{TM}
f_{EXT}	External single frequency on channel 1 ~ 4	—	—	—	1/2	f_{TM}
RES	Timer resolution	—	—	—	16	bits

I²C Characteristics

Table 21. I²C Characteristics

Symbol	Parameter	Standard mode		Fast mode		Fast mode plus		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	—	100	—	400	—	1000	kHz
$t_{SCL(H)}$	SCL clock high time	4.5	—	1.125	—	0.45	—	μs
$t_{SCL(L)}$	SCL clock low time	4.5	—	1.125	—	0.45	—	μs
t_{FALL}	SCL and SDA fall time	—	1.3	—	0.34	—	0.135	μs
t_{RISE}	SCL and SDA rise time	—	1.3	—	0.34	—	0.135	μs
$t_{SU(SDA)}$	SDA data setup time	500	—	125	—	50	—	ns
$t_{H(SDA)}$	SDA data hold time (5)	0	—	0	—	0	—	ns
	SDA data hold time (6)	100	—	100	—	100	—	ns
$t_{VD(SDA)}$	SDA data valid time	—	1.6	—	0.475	—	0.25	μs
$t_{SU(STA)}$	START condition setup time	500	—	125	—	50	—	ns
$t_{H(STA)}$	START condition hold time	0	—	0	—	0	—	ns
$t_{SU(STO)}$	STOP condition setup time	500	—	125	—	50	—	ns

Note: 1. Guaranteed by design, not tested in production.
2. To achieve 100 kHz standard mode, the peripheral clock frequency must be higher than 2 MHz.
3. To achieve 400 kHz fast mode, the peripheral clock frequency must be higher than 8 MHz.
4. To achieve 1 MHz fast mode plus, the peripheral clock frequency must be higher than 20 MHz.
5. The above characteristic parameters of the I²C bus timing are based on: COMB_FILTER_En = 0 and SEQ_FILTER = 00.
6. The above characteristic parameters of the I²C bus timing are based on: COMB_FILTER_En = 1 and SEQ_FILTER = 00.

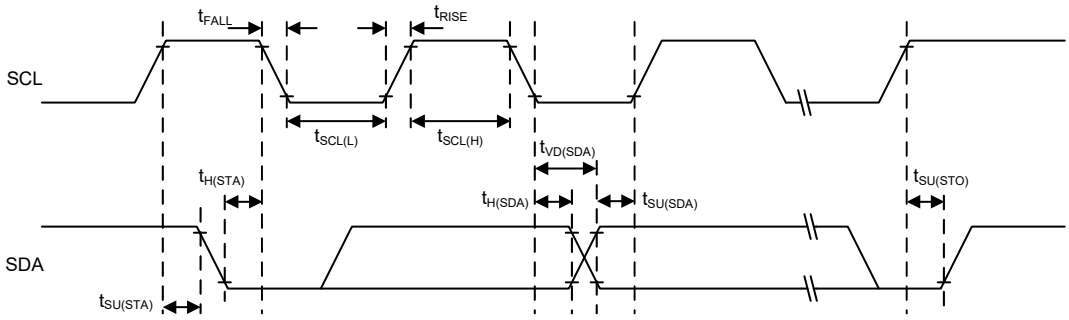


Figure 8. I²C Timing Diagrams

SPI Characteristics

Table 22. SPI Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	—	—	—	$f_{PCLK}/2$	MHz
$t_{SCK(H)}$	SCK clock high time	—	$f_{PCLK}/8$	—	—	ns
$t_{SCK(L)}$	SCK clock low time	—	$f_{PCLK}/8$	—	—	ns
SPI Master mode						
$t_{V(MO)}$	Data output valid time	—	—	—	5	ns
$t_{H(MO)}$	Data output hold time	—	2	—	—	ns
$t_{SU(MI)}$	Data input setup time	—	5	—	—	ns
$t_{H(MI)}$	Data input hold time	—	5	—	—	ns
SPI Slave mode						
$t_{SU(SEL)}$	SEL enable setup time	—	4 t_{PCLK}	—	—	ns
$t_{H(SEL)}$	SEL enable hold time	—	2 t_{PCLK}	—	—	ns
$t_{A(SO)}$	Data output access time	—	—	—	3 t_{PCLK}	ns
$t_{DIS(SO)}$	Data output disable time	—	—	—	10	ns
$t_{V(SO)}$	Data output valid time	—	—	—	25	ns
$t_{H(SO)}$	Data output hold time	—	15	—	—	ns
$t_{SU(SI)}$	Data input setup time	—	5	—	—	ns
$t_{H(SI)}$	Data input hold time	—	4	—	—	ns

Note: $t_{SCK} = 1/f_{SCK}$; $t_{PCLK} = 1/f_{PCLK}$. SPI output (input) clock frequency f_{SCK}; SPI peripheral clock frequency f_{PCLK}.

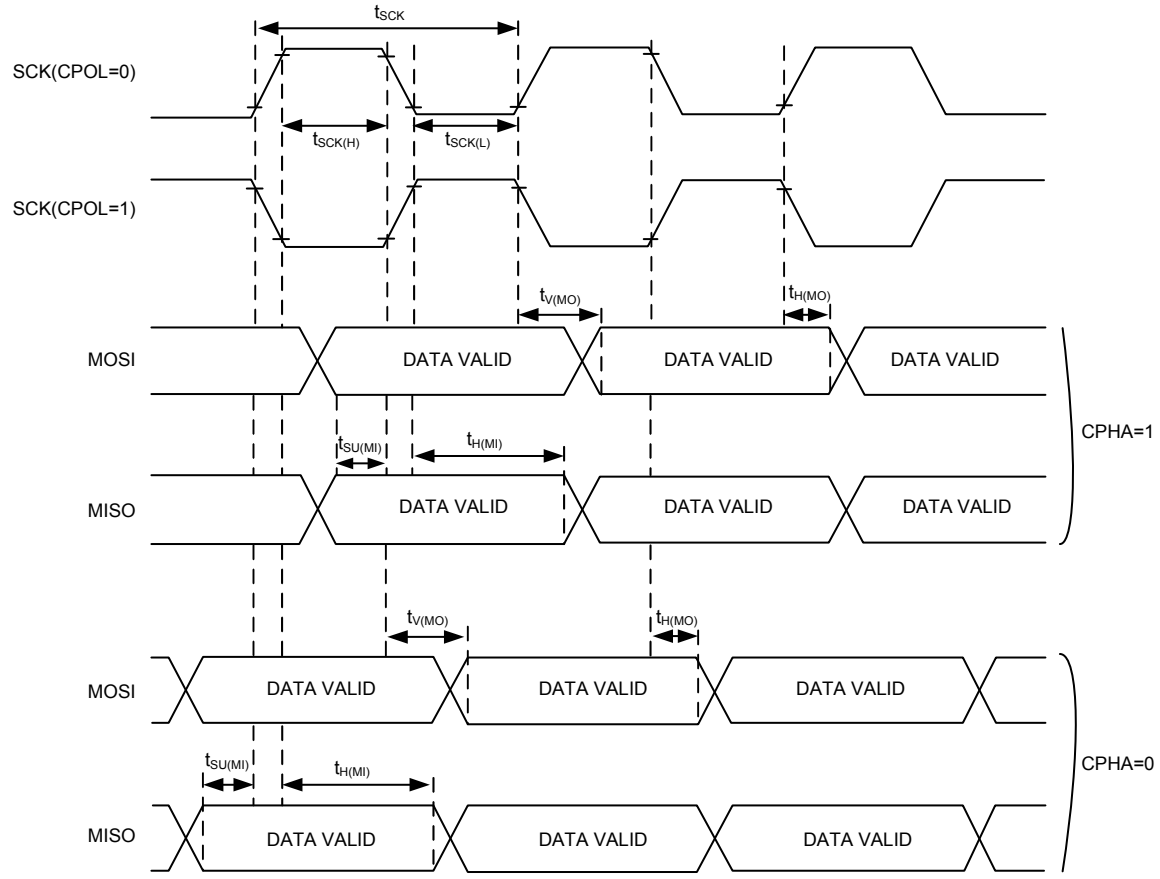


Figure 9. SPI Timing Diagrams – SPI Master Mode

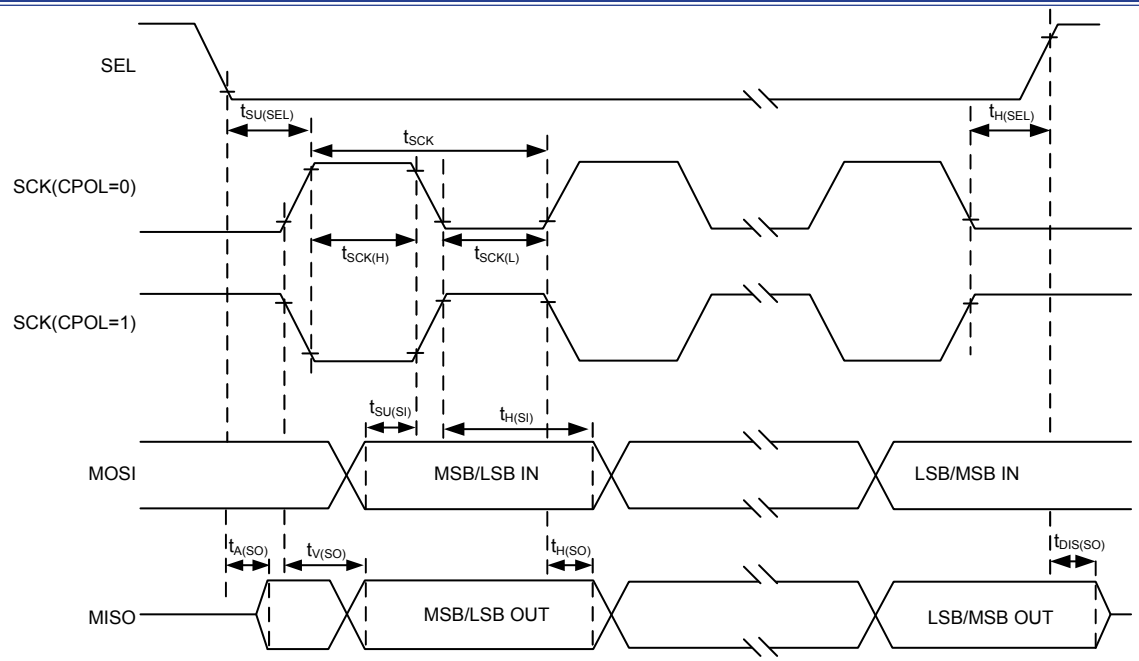


Figure 10. SPI Timing Diagrams – SPI Slave Mode with CPHA=1

I²S Characteristics

Table 23. I²S Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I²S Master mode						
$t_{WSD(MO)}$	WS output to BCLK delay	—	—	TBD	—	ns
$t_{DOD(MO)}$	Data output to BCLK delay	—	—	TBD	—	ns
$t_{DIS(MI)}$	Data input setup time	—	—	TBD	—	ns
$t_{DIH(MI)}$	Data input hold time	—	—	TBD	—	ns
I²S Slave mode						
$t_{BCH(SI)}$	BCLK high pulse width	—	—	TBD	—	ns
$t_{BCL(SI)}$	BCLK low pulse width	—	—	TBD	—	ns
$t_{WSS(SI)}$	WS input setup time	—	—	TBD	—	ns
$t_{DOD(SO)}$	Data output to BCLK delay	—	—	TBD	—	ns
$t_{DIS(SI)}$	Data input setup time	—	—	TBD	—	ns
$t_{DIH(SI)}$	Data input hold time	—	—	TBD	—	ns

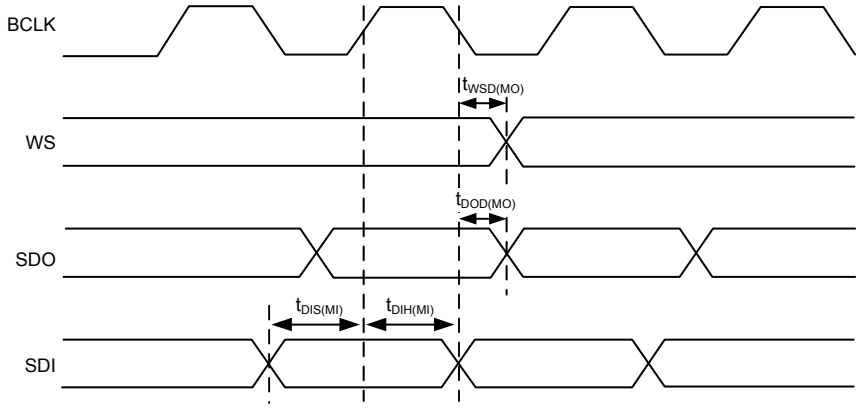


Figure 11. Timing of I²S Master Mode

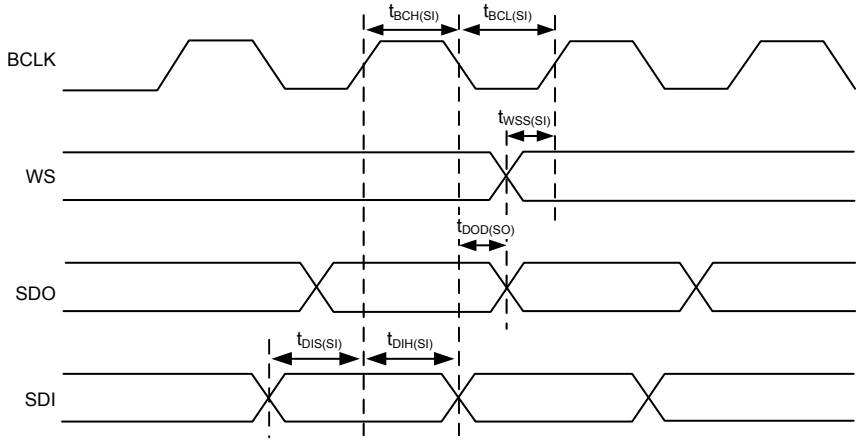


Figure 12. Timing of I²S Slave Mode

USB Characteristics

The USB interface is USB-IF certified - Full Speed.

Table 24. USB DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	USB operating voltage	—	3.0	—	3.6	V
V_{DI}	Differential input sensitivity	|USBDP-USBDM|	0.2	—	—	V
V_{CM}	Common mode voltage range	—	0.8	—	2.5	V
V_{SE}	Single-ended receiver threshold	—	0.8	—	2.0	V
V_{OL}	Pad output low voltage	R_L of 1.5 kΩ to V_{DD33}	0	—	0.3	V
V_{OH}	Pad output high voltage		2.8	—	3.6	V
V_{CRS}	Differential output signal cross-point voltage		1.3	—	2.0	V
Z_{DRV}	Driver output resistance	—	—	10	—	Ω
C_{IN}	Transceiver pad capacitance	—	—	—	20	pF

Note: 1. Guaranteed by design, not tested in production.
2. The USB functionality is ensured down to 2.7 V but not for the full USB electrical characteristics which will experience degradation in the 2.7 V to 3.0 V V_{DD} voltage range.
3. RL is the load connected to the USB driver USBDP.

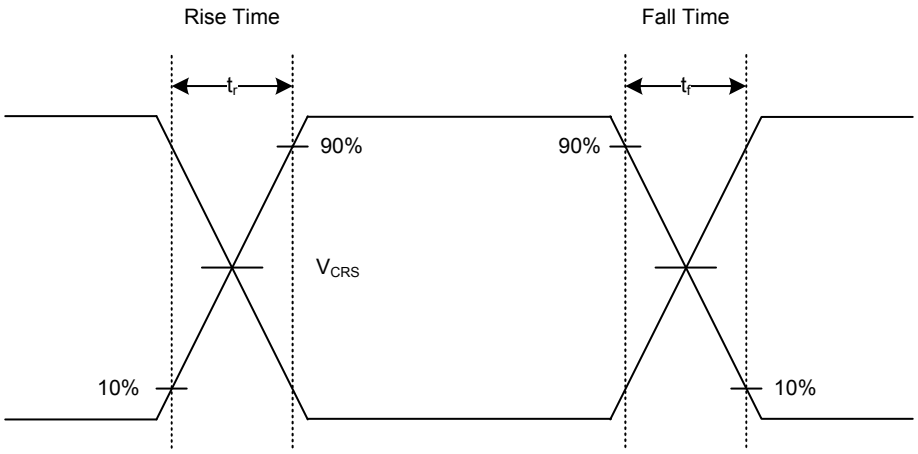


Figure 13. USB Signal Rise Time and Fall Time and Cross-Point Voltage (V_{CRS}) Definition

Table 25. USB AC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	Rise time	C_L = 50 pF	4	—	20	ns
t_f	Fall time	C_L = 50 pF	4	—	20	ns
$t_{r/f}$	Rise time / fall time matching	$t_{r/f} = t_r / t_f$	90	—	110	%

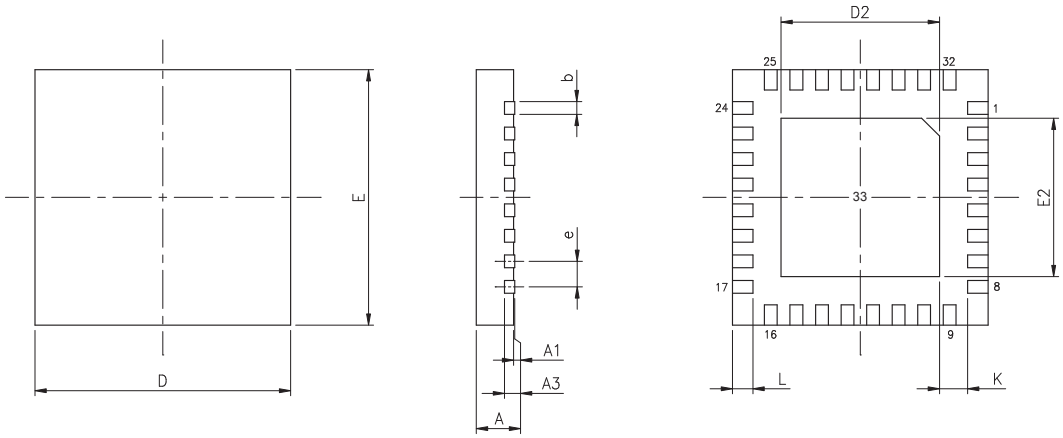
6 Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

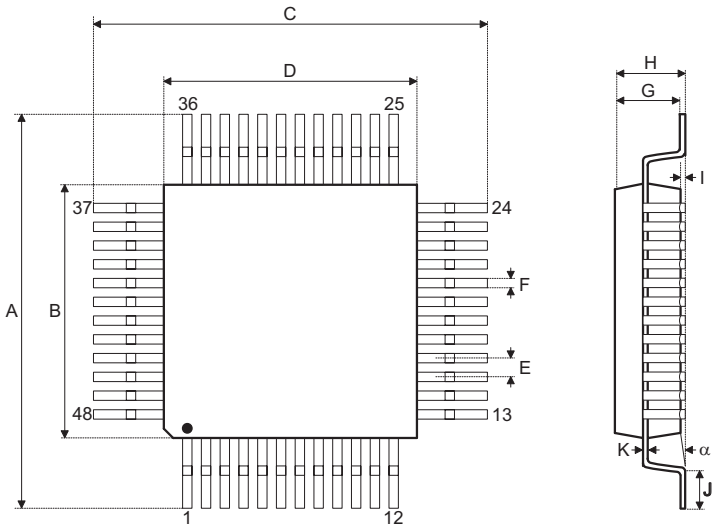
SAW Type 33-pin QFN (4mm×4mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3	—	0.008 BSC	—
b	0.006	0.008	0.010
D	—	0.157 BSC	—
E	—	0.157 BSC	—
e	—	0.016 BSC	—
D2	0.104	0.106	0.108
E2	0.104	0.106	0.108
L	0.014	0.016	0.018
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	—	0.203 BSC	—
b	0.15	0.20	0.25
D	—	4.00 BSC	—
E	—	4.00 BSC	—
e	—	0.40 BSC	—
D2	2.65	2.70	2.75
E2	2.65	2.70	2.75
L	0.35	0.40	0.45
K	0.20	—	—

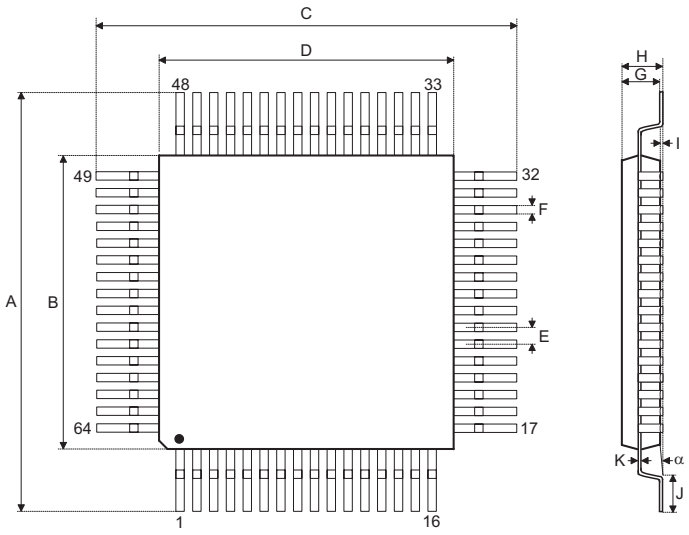
48-pin LQFP (7mm×7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.020 BSC	—
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.000 BSC	—
B	—	7.000 BSC	—
C	—	9.000 BSC	—
D	—	7.000 BSC	—
E	—	0.500 BSC	—
F	0.170	0.220	0.270
G	1.350	1.400	1.450
H	—	—	1.600
I	0.050	—	0.150
J	0.450	0.600	0.750
K	0.090	—	0.200
α	0°	—	7°

64-pin LQFP (7mm×7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.016 BSC	—
F	0.005	0.007	0.009
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.0 BSC	—
B	—	7.0 BSC	—
C	—	9.0 BSC	—
D	—	7.0 BSC	—
E	—	0.4 BSC	—
F	0.13	0.18	0.23
G	1.35	1.4	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°