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# HT32F52243/HT32F52253 Datasheet

**32-Bit Arm<sup>®</sup> Cortex<sup>®</sup>-M0+ Microcontroller,  
up to 128 KB Flash and 16 KB SRAM with 1 MSPS ADC,  
DIV, PDMA, USART, UART, SPI, I<sup>2</sup>C, MCTM,  
GPTM, SCTM, BFTM, CRC, RTC and WDT**

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# 1 General Description

The HOLTEK HT32F52243/52253 devices are high performance, low power consumption 32-bit microcontrollers based around an Arm® Cortex®-M0+ processor core. The Cortex™-M0+ is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer and including advanced debug support.

The devices operate at a frequency of up to 40 MHz for HT32F52243/52253 with a Flash accelerator to obtain maximum efficiency. It provides up to 128 KB of embedded Flash memory for code/data storage and 16 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as ADC, DIV, PDMA, I<sup>2</sup>C, USART, UART, SPI, MCTM, GPTM, SCTM, CRC-16/32, RTC, WDT, SW-DP (Serial Wire Debug Port), etc., are also implemented in the device series. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features ensure that the devices are suitable for use in a wide range of applications, especially in areas such as white goods application control, power monitors, alarm systems, consumer products, handheld equipment, data logging applications, motor control and so on.

**arm** CORTEX

## 2 Features

### Core

- 32-bit Arm® Cortex®-M0+ processor core
- Up to 40 MHz operating frequency for HT32F52243/52253
- Single-cycle multiplication
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex™-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized, low-power processor. The processor is based on the ARMv6-M architecture and supports Thumb® instruction sets; single-cycle I/O port; hardware multiplier and low latency interrupt respond time.

### On-chip Memory

- Up to 128 KB on-chip Flash memory for instruction/data and options storage
- 16 KB on-chip SRAM
- Supports multiple boot modes

The Arm® Cortex®-M0+ processor accesses and debug accesses share the single external interface to external AHB peripheral. The processor accesses take priority over debug accesses. The maximum address range of the Cortex™-M0+ is 4 GB since it has a 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex™-M0+ processor to reduce the software complexity of repeated implementation by different device vendors. However, some regions are used by the Arm® Cortex®-M0+ system peripherals. Refer to the Arm® Cortex®-M0+ Technical Reference Manual for more information. Figure 2 shows the memory map of the HT32F52243/52253 series of devices, including code, SRAM, peripheral, and other pre-defined regions.

### Flash Memory Controller – FMC

- Flash accelerator for maximum efficiency
- 32-bit word programming with In System Programming Interface (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions and pre-fetch buffer for the embedded on-chip Flash Memory. Since the access speed of the Flash Memory is slower than the CPU, a wide access interface with a pre-fetch buffer and cache are provided for the Flash Memory in order to reduce the CPU waiting time which will cause CPU instruction execution delays. Flash Memory word program/page erase functions are also provided.

## Reset Control Unit – RSTCU

- Supply supervisor
  - Power On Reset / Power Down Reset – POR/PDR
  - Brown-out Detector – BOD
  - Programmable Low Voltage Detector – LVD

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by an external signal, internal events and the reset generators.

## Clock Control Unit – CKCU

- External 4 to 16 MHz crystal oscillator
- External 32,768 Hz crystal oscillator
- Internal 8 MHz RC oscillator trimmed to  $\pm 2$  % accuracy at 3.3 V operating voltage and 25 °C operating temperature
- Internal 32 kHz RC oscillator
- Integrated system clock PLL
- Independent clock divider and gating bits for peripheral clock sources

The Clock Control unit, CKCU, provides a range of oscillator and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), a Phase Lock Loop (PLL), a HSE clock monitor, clock prescalers, clock multiplexers, APB clock divider and gating circuitry. The AHB, APB and Cortex®-M0+ clocks are derived from the system clock (CK\_SYS) which can come from the LSI, LSE, HSI, HSE or PLL. The Watchdog Timer and Real Time Clock (RTC) use either the LSI or LSE as their clock source.

## Power Management – PWRCU

- Single  $V_{DD}$  power supply: 2.0 V to 3.6 V
- Integrated 1.5 V LDO regulator for CPU core, peripherals and memories power supply
- $V_{DD}$  power supply for RTC
- Two power domains:  $V_{DD}$ , 1.5 V
- Four power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2, Power-Down

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in these devices provides many types of power saving modes such as Sleep, Deep-Sleep1, Deep-Sleep2 and Power-Down mode. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.



## External Interrupt/Event Controller – EXTI

- Up to 16 EXTI lines with configurable trigger source and type
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge or both edge
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

The External Interrupt/Event Controller, EXTI, comprises 16 edge detectors which can generate a wake-up event or interrupt requests independently. Each EXTI line can also be masked independently.

## Analog to Digital Converter – ADC

- 12-bit SAR ADC engine
- Up to 1 Msps conversion rate
- Up to 12 external analog input channels

A 12-bit multi-channel ADC is integrated in the device. There are multiplexed channels, which include 12 external analog signal channels and 2 internal channels which can be measured. If the input voltage is required to remain within a specific threshold window, an Analog Watchdog function will monitor and detect these signals. An interrupt will then be generated to inform the device that the input voltage is not within the preset threshold levels. There are three conversion modes to convert an analog signal to digital data. The ADC can be operated in one shot, continuous and discontinuous conversion modes.

## I/O Ports – GPIO

- Up to 52 GPIOs
- Port A, B, C, D are mapped as 16 external interrupts – EXTI
- Almost all I/O pins have a configurable output driving current.

There are up to 52 General Purpose I/O pins, GPIO, named from PA0 ~ PA15 to PD0 ~ PD3 for the implementation of logic input/output functions. Each of the GPIO ports has a series of related control and configuration registers to maximize flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

## Motor Control Timer – MCTM

- 16-bit up/down auto-reload counter
- 16-bit programmable prescaler allowing counter clock frequency division by any factor between 1 and 65536
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output
- Complementary Outputs with programmable dead-time insertion
- Supports 3-phase motor control and hall sensor interface
- Break input to force the timer's output signals into a reset or fixed condition

The Motor Control Timer consists of a single 16-bit up/down counter; four 16-bit CCRs (Capture/Compare Registers), single 16-bit counter-reload register (CRR), single 8-bit repetition counter and several control/status registers. It can be used for a variety of purposes including measuring the pulse widths of input signals or generating output waveforms such as compare match outputs, PWM outputs or complementary PWM outputs with dead-time insertion. The MCTM is capable of offering full functional support for motor control, hall sensor interfacing and break input.

## PWM Generation and Capture Timers – GPTM

- 16-bit up/down auto-reload counter
- 16-bit programmable prescaler allowing counter clock frequency division by any factor between 1 and 65536
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder

The General Purpose Timer consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR) and several control/status registers. They can be used for a variety of purposes including general time measurement, input signal pulse width measurement, output waveform generation such as single pulse generation or PWM output generation. The GPTM supports an Encoder Interface using a decoder with two inputs.

## Single Channel Generation and Capture Timers – SCTM

- 16-bit up and auto-reload counter
- One channel for each timer
- 16-bit programmable prescaler allowing counter clock frequency division by any factor between 1 and 65536
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned
- Single Pulse Mode Output

The Single-Channel Timer consists of one 16-bit up-counter, one 16-bit Capture/Compare Register (CCR), one 16-bit Counter-Reload Register (CRR) and several control/status registers. It can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as single pulse generation or PWM output.

## Basic Function Timer – BFTM

- 32-bit compare / match count-up counter – no I/O control features
- One shot mode – counting stops after a match condition
- Repetitive mode – restart counter after a match condition

The Basic Function Timer is a simple count-up 32-bit counter designed to measure time intervals and generate a one shot or repetitive interrupts. The BFTM operates in two functional modes, repetitive or one shot mode. In the repetitive mode the BFTM restarts the counter when a compare match event occurs. The BFTM also supports a one shot mode which forces the counter to stop counting when a compare match event occurs.

## Watchdog Timer – WDT

- 12-bit down counter with 3-bit prescaler
- Reset event for the system
- Programmable watchdog timer window function
- Register write protection function

The Watchdog Timer is a hardware timing circuit that can be used to detect system failures due to software malfunctions. It includes a 12-bit count-down counter, a prescaler, a WDT delta value register, WDT operation control circuitry and a WDT protection mechanism. If the software does not reload the counter value before a Watchdog Timer underflow occurs, a reset will be generated when the counter underflows. In addition, a reset is also generated if the software reloads the counter when the counter value is greater than the WDT delta value. This means the counter must be reloaded within a limited timing window using a specific method. The Watchdog Timer counter can be stopped while the processor is in the debug mode. There is a register write protect function which can be enabled to prevent it from changing the Watchdog Timer configuration unexpectedly.

## Real Time Clock – RTC

- 24-bit up-counter with a programmable prescaler
- Alarm function
- Interrupt and Wake-up event

The Real Time Clock, RTC, includes an APB interface, a 24-bit count-up counter, a control register, a prescaler, a compare register and a status register. Most of the RTC circuits are located in the Backup Domain except for the APB interface. The APB interface is located in the  $V_{DD15}$  power domain. Therefore, it is necessary to be isolated from the ISO signal that comes from the power control unit when the  $V_{DD15}$  power domain is powered off, that is when the device enters the Power-Down mode. The RTC counter is used as a wakeup timer to generate a system resume signal from the Power-Down mode.

## Inter-integrated Circuit – I<sup>2</sup>C

- Supports both master and slave modes with a frequency of up to 1 MHz
- Provide an arbitration function and clock synchronization
- Supports 7-bit and 10-bit addressing modes and general call addressing
- Supports slave multi-addressing mode with maskable address

The I<sup>2</sup>C is an internal circuit allowing communication with an external I<sup>2</sup>C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I<sup>2</sup>C module provides three data transfer rates: (1) 100 kHz in the Standard mode, (2) 400 kHz in the Fast mode and (3) 1 MHz in the Fast plus mode. The SCL period generation register is used to setup different kinds of duty cycle implementations for the SCL pulse.

The SDA line which is connected directly to the I<sup>2</sup>C bus is a bi-directional data line between the master and slave devices and is used for data transmission and reception. The I<sup>2</sup>C also has an arbitration detect function and clock synchronization to prevent situations where more than one master attempts to transmit data to the I<sup>2</sup>C bus at the same time.

## Serial Peripheral Interface – SPI

- Supports both master and slave mode
- Frequency of up to ( $f_{PCLK}/2$ ) MHz for the master mode and ( $f_{PCLK}/3$ ) MHz for the slave mode
- FIFO Depth: 8 levels
- Multi-master and multi-slave operation

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive function in both master and slave mode. The SPI interface uses 4 pins, which are the serial data input and output lines MISO and MOSI, the clock line, SCK, and the slave select line, SEL. One SPI device acts as a master device which controls the data flow using the SEL and SCK signals to indicate the start of data communication and the data sampling rate. To receive a data byte, the streamed data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but in a reverse sequence. The mode fault detection provides a capability for multi-master applications.

## Universal Synchronous Asynchronous Receiver Transmitter – USART

- Supports both asynchronous and clocked synchronous serial communication modes
- Asynchronous operating baud rate up to ( $f_{\text{CLK}}/16$ ) MHz and synchronous operating rate up to ( $f_{\text{CLK}}/8$ ) MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error
- Auto hardware flow control mode – RTS, CTS
- IrDA SIR encoder and decoder
- RS485 mode with output enable control
- FIFO Depth: 8-level for both receiver and transmitter

The Universal Synchronous Asynchronous Receiver Transceiver, USART, provides a flexible full duplex data exchange using synchronous or asynchronous data transfer. The USART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The USART peripheral function supports four types of interrupt including Line Status Interrupt, Transmitter FIFO Empty Interrupt, Receiver Threshold Level Reaching Interrupt and Time Out Interrupt. The USART module includes a transmitter FIFO (TX FIFO) and receiver FIFO (RX FIFO). The software can detect a USART error status by reading the Line Status Register, LSR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

## Universal Asynchronous Receiver Transmitter – UART

- Asynchronous serial communication operating baud-rate up to ( $f_{\text{CLK}}/16$ ) MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports Line Status Interrupt. The software can detect a UART error status by reading the Line Status Register, LSR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

## Cyclic Redundancy Check – CRC

- Support CRC16 polynomial: 0x8005,  
 $X^{16}+X^{15}+X^2+1$
- Support CCITT CRC16 polynomial: 0x1021,  
 $X^{16}+X^{12}+X^5+1$
- Support IEEE-802.3 CRC32 polynomial: 0x04C11DB7,  
 $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^8+X^7+X^5+X^4+X^2+X+1$
- Supports 1's complement, byte reverse & bit reverse operation on data and checksum
- Supports byte, half-word & word data size
- Programmable CRC initial seed value
- CRC computation executed in 1 AHB clock cycle for 8-bit data and 4 AHB clock cycles for 32-bit data
- Supports PDMA to complete a CRC computation of a block of memory

The CRC calculation unit is an error detection technique test algorithm which is used to verify data transmission or storage data correctness. A CRC calculation takes a data stream or a block of data as its input and generates a 16-bit or 32-bit output remainder. Ordinarily, a data stream is suffixed by a CRC code and used as a checksum when being sent or stored. Therefore, the received or restored data stream is calculated by the same generator polynomial as described above. If the new CRC code result does not match the one calculated earlier, that means the data stream contains a data error.

## Peripheral Direct Memory Access – PDMA

- 6 channels with trigger source grouping
- 8-/16-/32-bit width data transfer
- Supports Address increment, decrement or fixed mode
- 4-level programmable channel priority
- Auto reload mode
- Supports trigger source: ADC, SPI, USART, UART, I<sup>2</sup>C, GPTM, MCTM and software request

The Peripheral Direct Memory Access controller, PDMA, moves data between the peripherals and the system memory on the AHB bus. Each PDMA channel has a source address, destination address, block length and transfer count. The PDMA can exclude the CPU intervention and avoid interrupt service routine execution. It improves system performance as the software does not need to connect each data movement operation.

## Hardware Divider – DIV

- Signed/unsigned 32-bit divider
- Operation in 8 clock cycles, Load in 1 clock cycle
- Divide by zero error Flag

The divider is the truncated division and need software trigger start single by control register “START” bit , after 8 clock cycles, the divider calculate complete flag will be set to 1, and if divisor register data is zero, divide zero error flag will be set to 1.

## Debug Support

- Serial Wire Debug Port – SW-DP
- 4 comparators for hardware breakpoint or code / literal patch
- 2 comparators for hardware watchpoints

## Package and Operation Temperature

- 33/46-pin QFN, 48/64-pin LQFP package
- Operation temperature range: -40 °C to +85 °C

# 3 Overview

## Device Information

**Table 1. Features and Peripheral List**

Peripherals		HT32F52243	HT32F52253
Main Flash (KB)		64	127
Option Bytes Flash (KB)		1	1
SRAM (KB)		8	16
Timers	MCTM		1
	GPTM		1
	SCTM		4
	BFTM		2
	RTC		1
	WDT		1
Communication	SPI		2
	USART		2
	UART		4
	I <sup>2</sup> C		3
PDMA			6 channels
Hardware Divider			1
CRC-16/32			1
EXTI			16
12-bit ADC			1
Number of channels			12 Channels
GPIO			Up to 52
CPU frequency			Up to 40 MHz
Operating voltage			2.0 V ~ 3.6 V
Operating temperature			-40 °C ~ +85 °C
Package		33/46-pin QFN, 48/64-pin LQFP	



## Block Diagram

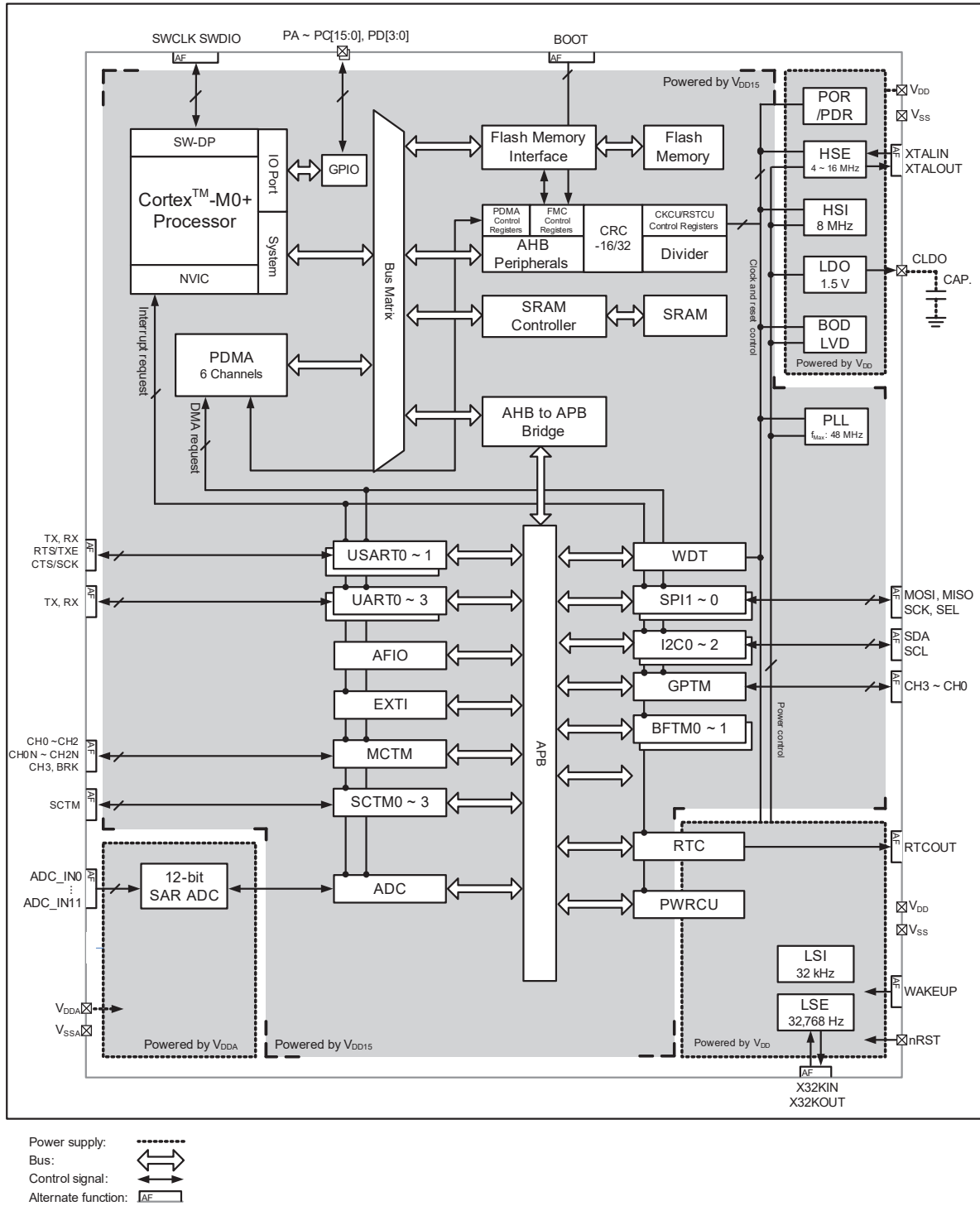


Figure 1. Block Diagram

## Memory Map

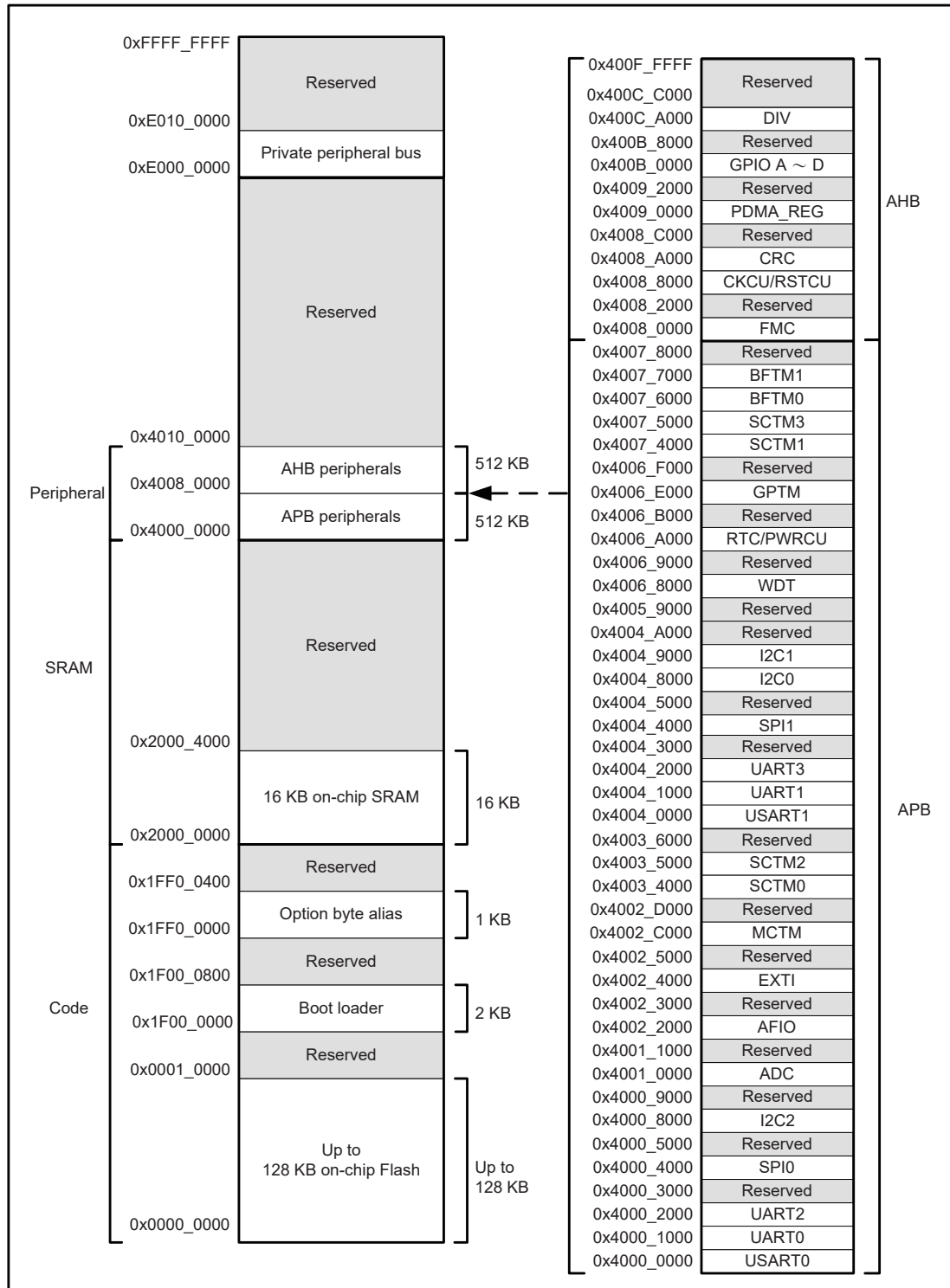


Figure 2. Memory Map

**Table 2. Register Map**

Start Address	End Address	Peripheral	Bus
0x4000_0000	0x4000_0FFF	USART0	APB
0x4000_1000	0x4000_1FFF	UART0	
0x4000_2000	0x4000_2FFF	UART2	
0x4000_3000	0x4000_3FFF	Reserved	
0x4000_4000	0x4000_4FFF	SPI0	
0x4000_5000	0x4000_7FFF	Reserved	
0x4000_8000	0x4000_8FFF	I2C2	
0x4000_9000	0x4000_FFFF	Reserved	
0x4001_0000	0x4001_0FFF	ADC	
0x4001_1000	0x4002_1FFF	Reserved	
0x4002_2000	0x4002_2FFF	AFIO	
0x4002_3000	0x4002_3FFF	Reserved	
0x4002_4000	0x4002_4FFF	EXTI	
0x4002_5000	0x4002_BFFF	Reserved	
0x4002_C000	0x4002_CFFF	MCTM	
0x4002_D000	0x4003_3FFF	Reserved	
0x4003_4000	0x4003_4FFF	SCTM0	
0x4003_5000	0x4003_5FFF	SCTM2	
0x4003_6000	0x4003_FFFF	Reserved	
0x4004_0000	0x4004_0FFF	USART1	
0x4004_1000	0x4004_1FFF	UART1	
0x4004_2000	0x4004_2FFF	UART3	
0x4004_3000	0x4004_3FFF	Reserved	
0x4004_4000	0x4004_4FFF	SPI1	
0x4004_5000	0x4004_7FFF	Reserved	
0x4004_8000	0x4004_8FFF	I2C0	
0x4004_9000	0x4004_9FFF	I2C1	
0x4004_A000	0x4006_7FFF	Reserved	
0x4006_8000	0x4006_8FFF	WDT	
0x4006_9000	0x4006_9FFF	Reserved	
0x4006_A000	0x4006_AFFF	RTC/PWRCU	
0x4006_B000	0x4006_DFFF	Reserved	
0x4006_E000	0x4006_EFFF	GPTM	
0x4006_F000	0x4007_3FFF	Reserved	
0x4007_4000	0x4007_4FFF	SCTM1	
0x4007_5000	0x4007_5FFF	SCTM3	
0x4007_6000	0x4007_6FFF	BFTM0	
0x4007_7000	0x4007_7FFF	BFTM1	
0x4007_8000	0x4007_FFFF	Reserved	

Start Address	End Address	Peripheral	Bus
0x4008_0000	0x4008_1FFF	FMC	AHB
0x4008_2000	0x4008_7FFF	Reserved	
0x4008_8000	0x4008_9FFF	CKCU/RSTCU	
0x4008_A000	0x4008_BFFF	CRC	
0x4008_C000	0x4008_FFFF	Reserved	
0x4009_0000	0x4009_1FFF	PDMA_REG	
0x4009_2000	0x400A_FFFF	Reserved	
0x400B_0000	0x400B_1FFF	GPIOA	
0x400B_2000	0x400B_3FFF	GPIOB	
0x400B_4000	0x400B_5FFF	GPIOC	
0x400B_6000	0x400B_7FFF	GPIOD	
0x400B_8000	0x400C_9FFF	Reserved	
0x400C_A000	0x400C_BFFF	DIV	
0x400C_C000	0x400F_FFFF	Reserved	

## Clock Structure

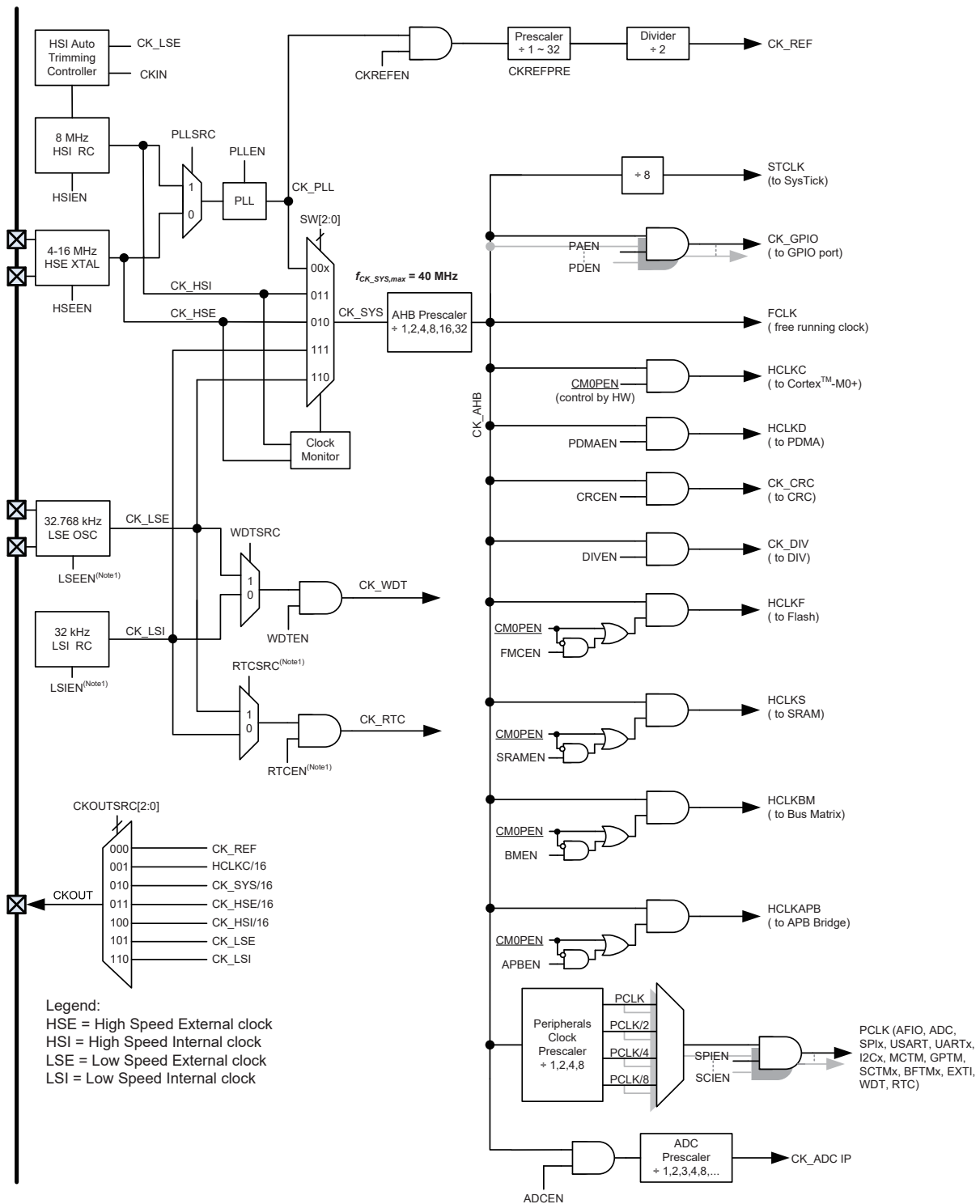


Figure 3. Clock Structure

# 4 Pin Assignment

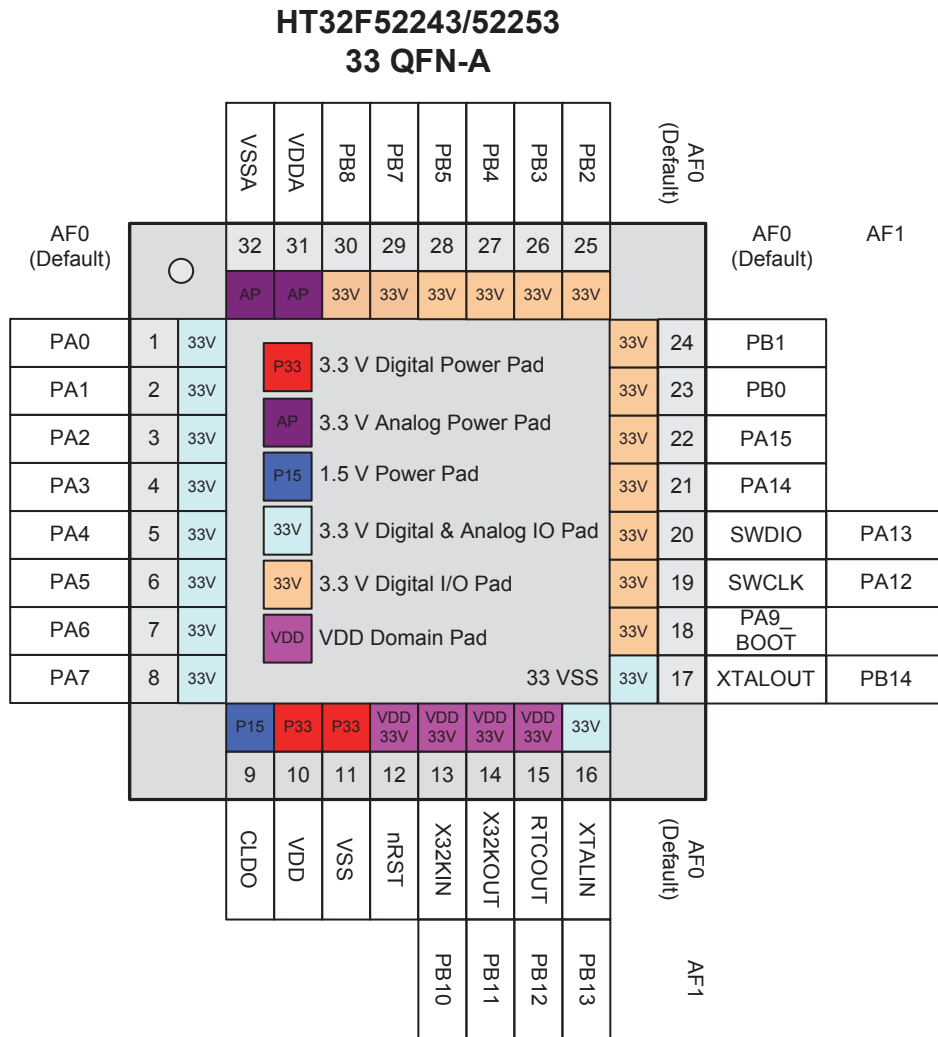


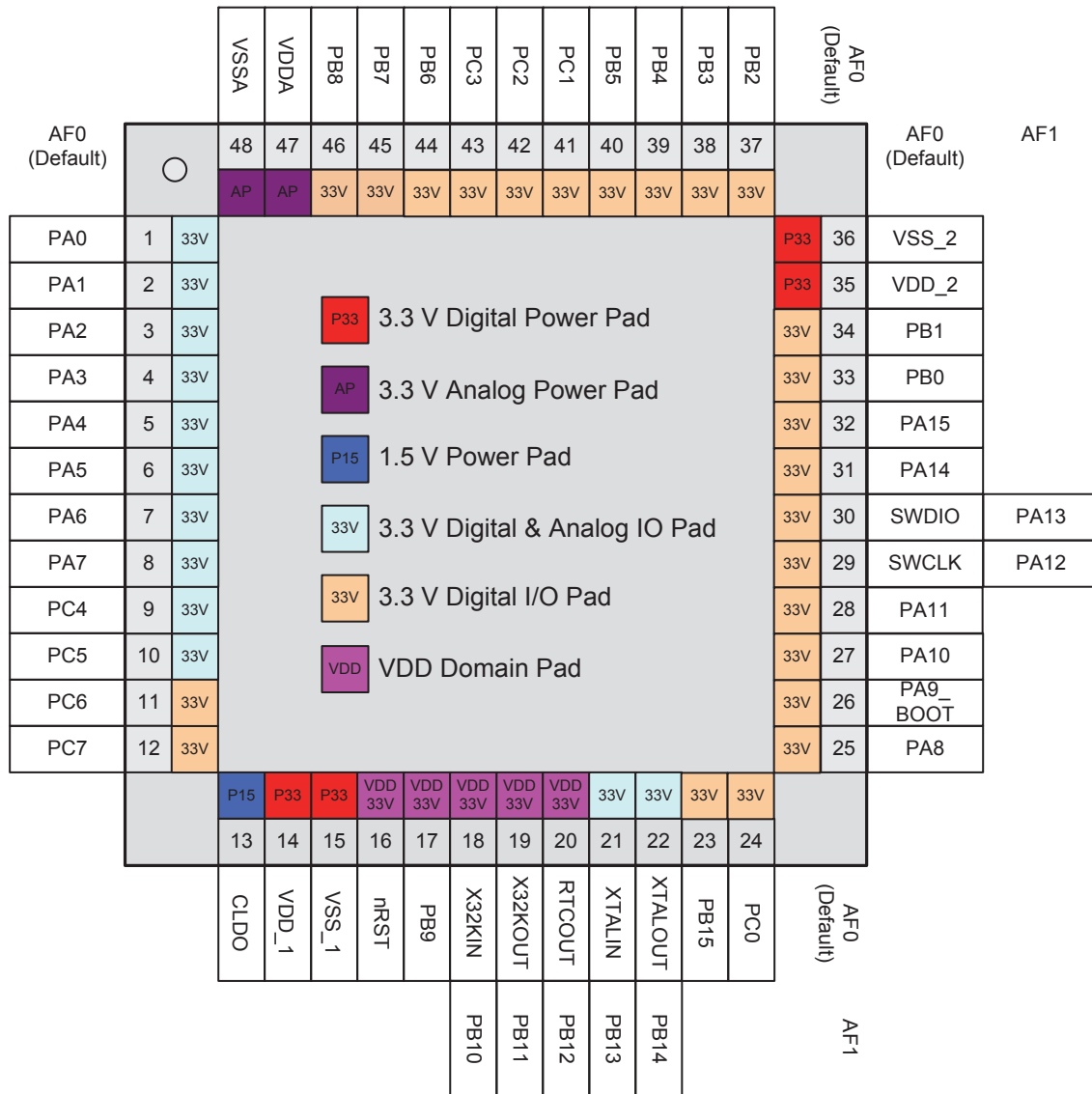
Figure 4. HT32F52243/52253 33-pin QFN Pin Assignment

**HT32F52243/52253  
46 QFN-A**

		(Default) AF0													AF0 (Default)				AF1		
		PA0 VSSA VDDA PB8 PB7 PB6 PC3 PC2 PC1 PB5 PB4 PB3 PB2 VSS_2													P33				AF0 (Default)		
○		46	45	44	43	42	41	40	39	38	37	36	35	34	33	P33				AF0 (Default)	
		33V	AP	AP	33V	33V	33V	33V	33V	33V	33V	33V	33V	33V	33V	P33				AF1	
PA1	1	33V														P33	32	VDD_2			
PA2	2	33V														33V	31	PB1			
PA3	3	33V														AP	30	PB0			
PA4	4	33V														P15	29	PA15			
PA5	5	33V														33V	28	PA14			
PA6	6	33V														33V	27	SWDIO	PA13		
PA7	7	33V														33V	26	SWCLK	PA12		
PC6	8	33V														33V	25	PA11			
PC7	9	33V														VDD	24	PA10			
		EP: VSS													33V				AF0 (Default)		
		P15	P33	P33	VDD 33V	VDD 33V	VDD 33V	VDD 33V	VDD 33V	33V	33V	33V	33V	33V	33V	33V				AF1	
		10	11	12	13	14	15	16	17	18	19	20	21	22	23				AF1		
		CLDO	VDD_1	VSS_1	nRST	PB9	X32KIN	X32KOUT	RTCOUT	XTALIN	XTALOUT	PB15	PC0	PA8	PA9_BOOT				AF1		
															PB10	PB11	PB12	PB13	PB14		

**Figure 5. HT32F52243/52253 46-pin QFN Pin Assignment**

**HT32F52243/52253  
 48 LQFP-A**

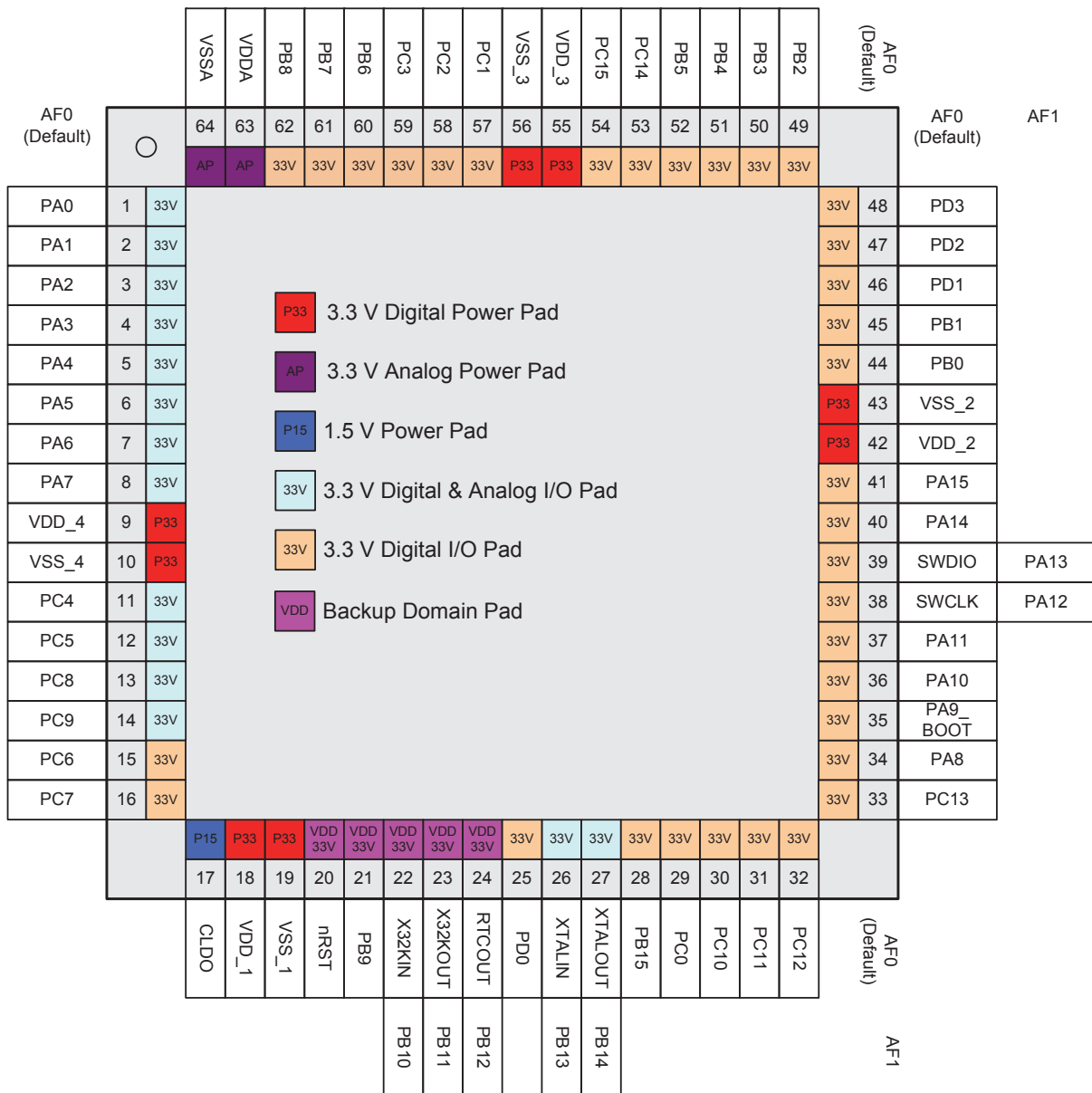


4 Pin Assignment

**Figure 6. HT32F52243/52253 48-pin LQFP Pin Assignment**



**HT32F52243/52253  
 64 LQFP-A**



**Figure 7. HT32F52243/52253 64-pin LQFP Pin Assignment**

**Table 3. HT32F52243/52253 Series Pin Assignment for 33/46-pin QFN, 48/64-pin LQFP Package**

Package				HT32F52243/52253 Alternate function number															
64 LQFP	48 LQFP	46 QFN	33 QFN	AF0 System Default	AF1 GPIO	AF2 ADC	AF3 N/A	AF4 MCTM /GPTM	AF5 SPI	AF6 USART /UART	AF7 I <sup>2</sup> C	AF8 N/A	AF9 N/A	AF10 N/A	AF11 N/A	AF12 N/A	AF13 SCTM	AF14 N/A	AF15 System Other
1	1	46	1	PA0		ADC_IN0		GT_CH0	SPI1_SCK	USR0_RTS	I2C1_SCL								
2	2	1	2	PA1		ADC_IN1		GT_CH1	SPI1_MOSI	USR0_CTS	I2C1_SDA								
3	3	2	3	PA2		ADC_IN2		GT_CH2	SPI1_MISO	USR0_TX									
4	4	3	4	PA3		ADC_IN3		GT_CH3	SPI1_SEL	USR0_RX							SCTM2		
5	5	4	5	PA4		ADC_IN4		GT_CH0	SPI0_SCK	USR1_TX	I2C0_SCL								
6	6	5	6	PA5		ADC_IN5		GT_CH1	SPI0_MOSI	USR1_RX	I2C0_SDA								
7	7	6	7	PA6		ADC_IN6		GT_CH2	SPI0_MISO	USR1_RTS									
8	8	7	8	PA7		ADC_IN7		GT_CH3	SPI0_SEL	USR1_CTS							SCTM3		
9				VDD_4															
10		EP*		VSS_4															
11	9			PC4		ADC_IN8		GT_CH0	SPI1_SEL	USR0_TX	I2C1_SCL						SCTM0		
12	10			PC5		ADC_IN9		GT_CH1	SPI1_SCK	USR0_RX	I2C1_SDA						SCTM1		
13				PC8		ADC_IN10		GT_CH2	SPI1_MOSI	UR1_TX							SCTM2		
14				PC9		ADC_IN11		GT_CH3	SPI1_MISO	UR1_RX							SCTM3		
15	11	8		PC6				MT_CH2		UR0_TX	I2C0_SCL								
16	12	9		PC7				MT_CH2N		UR0_RX	I2C0_SDA								
17	13	10	9	CLDO															
18	14	11	10	VDD_1															
19	15	12	11	VSS_1															
20	16	13	12	nRST															
21	17	14		PB9				MT_CH3		UR0_TX							SCTM1		
22	18	15	13	X32KIN	PB10			GT_CH0	SPI1_SEL	USR1_TX	I2C2_SCL						SCTM2		
23	19	16	14	X32KOUT	PB11			GT_CH1	SPI1_SCK	USR1_RX	I2C2_SDA						SCTM3		
24	20	17	15	RTCOUT	PB12				SPI0_MISO	UR0_RX									WAKEUP
25				PD0							I2C2_SDA						SCTM2		
26	21	18	16	XTALIN	PB13					UR3_TX	I2C0_SCL								
27	22	19	17	XTALOUT	PB14					UR3_RX	I2C0_SDA								
28	23	20		PB15				MT_CH0	SPI0_SEL	USR1_TX	I2C1_SCL								
29	24	21		PC0				MT_CH0N	SPI0_SCK	USR1_RX	I2C1_SDA						SCTM3		
30				PC10				GT_CH0	SPI1_SEL	UR2_TX									
31				PC11				GT_CH1	SPI1_SCK	UR2_RX									
32				PC12				GT_CH2	SPI1_MOSI	UR1_TX	I2C2_SCL								
33				PC13				GT_CH3	SPI1_MISO	UR1_RX	I2C2_SDA								
34	25	22		PA8						USR0_TX							SCTM2		
35	26	23	18	PA9_BOOT					SPI0_MOSI	UR3_TX							SCTM3		CKOUT
36	27	24		PA10				MT_CH1	SPI0_MOSI	USR0_RX	I2C2_SCL								
37	28	25		PA11				MT_CH1N	SPI0_MISO	UR3_RX	I2C2_SDA						SCTM0		
38	29	26	19	SWCLK	PA12														
39	30	27	20	SWDIO	PA13														
40	31	28	21	PA14				MT_CH0	SPI1_SEL	USR0_RTS	I2C1_SCL								
41	32	29	22	PA15				MT_CH0N	SPI1_SCK	USR0_CTS	I2C1_SDA						SCTM1		
42				VDD_2															
43				VSS_2															
44	33	30	23	PB0				MT_CH1	SPI1_MOSI	USR0_TX	I2C0_SCL								
45	34	31	24	PB1				MT_CH1N	SPI1_MISO	USR0_RX	I2C0_SDA						SCTM2		
46				PD1				MT_CH2		USR1_RTS									
47				PD2				MT_CH2N		USR1_CTS									
48				PD3				MT_CH3											
	35	32		VDD_2															
	36	33	33	VSS_2															
49	37	34	25	PB2				MT_CH2	SPI0_SEL	UR2_TX									CKIN
50	38	35	26	PB3				MT_CH2N	SPI0_SCK	UR2_RX							SCTM1		
51	39	36	27	PB4				MT_BRK	SPI0_MOSI	UR1_TX							SCTM0		
52	40	37	28	PB5				GT_CH2	SPI0_MISO	UR1_RX									
53				PC14				MT_CH3		UR3_TX	I2C2_SCL						SCTM2		
54				PC15						UR3_RX	I2C2_SDA						SCTM3		
55				VDD_3															
56				VSS_3															
57	41	38		PC1				MT_CH0	SPI1_SEL	UR1_TX									

Package				HT32F52243/52253 Alternate function number														
				AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14
58	42	39		PC2				MT_CH0N	SPI1_SCK	UR2_RX								
59	43	40		PC3				MT_BRK	SPI1_MOSI	UR1_RX	I2C2_SCL							
60	44	41		PB6				GT_CH3	SPI1_MISO	UR2_TX	I2C2_SDA							
61	45	42	29	PB7				MT_CH1	SPI0_MISO	UR0_TX	I2C1_SCL							
62	46	43	30	PB8				MT_CH1N	SPI0_SEL	UR0_RX	I2C1_SDA							
63	47	44	31	VDDA														
64	48	45	32	VSSA														

Note: 1. The EP is meant the exposed pad of the QFN package.  
2. The pin number 33 of the QFN33 is located at the exposed pad of the QFN package.

**Table 4. HT32F52243/52253 Pin Description**

Pin number				Pin Name	Type <sup>(1)</sup>	IO Structure <sup>(2)</sup>	Output Driving	Description	
64 LQFP	48 LQFP	46 QFN	33 QFN					Default function (AF0)	
1	1	46	1	PA0	A/I/O	33V	4/8/12/16 mA	PA0	
2	2	1	2	PA1	A/I/O	33V	4/8/12/16 mA	PA1	
3	3	2	3	PA2	A/I/O	33V	4/8/12/16 mA	PA2	
4	4	3	4	PA3	A/I/O	33V	4/8/12/16 mA	PA3	
5	5	4	5	PA4	A/I/O	33V	4/8/12/16 mA	PA4	
6	6	5	6	PA5	A/I/O	33V	4/8/12/16 mA	PA5	
7	7	6	7	PA6	A/I/O	33V	4/8/12/16 mA	PA6	
8	8	7	8	PA7	A/I/O	33V	4/8/12/16 mA	PA7	
9				VDD_4	P	—	—	Voltage for digital I/O	
10		EP		VSS_4	P	—	—	Ground reference for digital I/O	
11	9			PC4	A/I/O	33V	4/8/12/16 mA	PC4	
12	10			PC5	A/I/O	33V	4/8/12/16 mA	PC5	
13				PC8	A/I/O	33V	4/8/12/16 mA	PC8	
14				PC9	A/I/O	33V	4/8/12/16 mA	PC9	
15	11	8		PC6	I/O	33V	4/8/12/16 mA	PC6	
16	12	9		PC7	I/O	33V	4/8/12/16 mA	PC7	
17	13	10	9	CLDO	P	—	—	Core power LDO 1.5 V output. It must be connected a 2.2 μF capacitor as close as possible between this pin and VSS_1.	
18	14	11	10	VDD_1	P	—	—	Voltage for digital I/O	
19	15	12	11	VSS_1	P	—	—	Ground reference for digital I/O	
20	16	13	12	nRST <sup>(3)</sup>	I	33V_PU	—	External reset pin and external wakeup pin in the Power-Down mode	
21	17	14		PB9 <sup>(3)</sup>	I/O (V <sub>DD</sub> )	33V	4/8/12/16 mA	PB9	
22	18	15	13	PB10 <sup>(3)</sup>	A/I/O (V <sub>DD</sub> )	33V	4/8/12/16 mA	X32KIN	
23	19	16	14	PB11 <sup>(3)</sup>	A/I/O (V <sub>DD</sub> )	33V	4/8/12/16 mA	X32KOUT	
24	20	17	15	PB12 <sup>(3)</sup>	I/O (V <sub>DD</sub> )	33V	4/8/12/16 mA	RTCOUT	
25				PD0	I/O	33V	4/8/12/16 mA	PD0	
26	21	18	16	PB13	A/I/O	33V	4/8/12/16 mA	XTALIN	
27	22	19	17	PB14	A/I/O	33V	4/8/12/16 mA	XTALOUT	
28	23	20		PB15	I/O	33V	4/8/12/16 mA	PB15	
29	24	21		PC0	I/O	33V	4/8/12/16 mA	PC0	
30				PC10	I/O	33V	4/8/12/16 mA	PC10	
31				PC11	I/O	33V	4/8/12/16 mA	PC11	
32				PC12	I/O	33V	4/8/12/16 mA	PC12	
33				PC13	I/O	33V	4/8/12/16 mA	PC13	

Pin number				Pin Name	Type <sup>(1)</sup>	IO Structure <sup>(2)</sup>	Output Driving	Description
64 LQFP	48 LQFP	46 QFN	33 QFN					Default function (AF0)
34	25	22		PA8	I/O	33V	4/8/12/16 mA	PA8
35	26	23	18	PA9	I/O	33V_PU	4/8/12/16 mA	PA9_BOOT
36	27	24		PA10	I/O	33V	4/8/12/16 mA	PA10
37	28	25		PA11	I/O	33V	4/8/12/16 mA	PA11
38	29	26	19	PA12	I/O	33V_PU	4/8/12/16 mA	SWCLK
39	30	27	20	PA13	I/O	33V_PU	4/8/12/16 mA	SWDIO
40	31	28	21	PA14	I/O	33V	4/8/12/16 mA	PA14
41	32	29	22	PA15	I/O	33V	4/8/12/16 mA	PA15
42				VDD_2	P	—	—	Voltage for digital I/O
43			33	VSS_2	P	—	—	Ground reference for digital I/O
44	33	30	23	PB0	I/O	33V	4/8/12/16 mA	PB0
45	34	31	24	PB1	I/O	33V	4/8/12/16 mA	PB1
46				PD1	I/O	33V	4/8/12/16 mA	PD1
47				PD2	I/O	33V	4/8/12/16 mA	PD2
48				PD3	I/O	33V	4/8/12/16 mA	PD3
	35	32		VDD_2	P	—	—	Voltage for digital I/O
	36	33	33	VSS_2	P	—	—	Ground reference for digital I/O
49	37	34	25	PB2	I/O	33V	4/8/12/16 mA	PB2
50	38	35	26	PB3	I/O	33V	4/8/12/16 mA	PB3
51	39	36	27	PB4	I/O	33V	4/8/12/16 mA	PB4
52	40	37	28	PB5	I/O	33V	4/8/12/16 mA	PB5
53				PC14	I/O	33V	4/8/12/16 mA	PC14
54				PC15	I/O	33V	4/8/12/16 mA	PC15
55				VDD_3	P	—	—	Voltage for digital I/O
56				VSS_3	P	—	—	Ground reference for digital I/O
57	41	38		PC1	AI/O	33V	4/8/12/16 mA	PC1
58	42	39		PC2	AI/O	33V	4/8/12/16 mA	PC2
59	43	40		PC3	AI/O	33V	4/8/12/16 mA	PC3
60	44	41		PB6	AI/O	33V	4/8/12/16 mA	PB6
61	45	42	29	PB7	AI/O	33V	4/8/12/16 mA	PB7
62	46	43	30	PB8	AI/O	33V	4/8/12/16 mA	PB8
63	47	44	31	VDDA	P	—	—	Analog voltage for ADC and Comparator
64	48	45	32	VSSA	P	—	—	Ground reference for the ADC and Comparator

Note: 1. I = input, O = output, A = Analog port, P = power supply, PU = pull-up, VDD = V<sub>DD</sub> Power, EP = Exposed Pad.  
 2. 33V = 2.0 V ~ 3.6 V tolerant.  
 3. These pins are located at the V<sub>DD</sub> power domain.  
 4. The pin number 33 of the QFN33 is located at the exposed pad of the QFN package.

# 5 Electrical Characteristics

## Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**Table 5. Absolute Maximum Ratings**

Symbol	Parameter	Min.	Max.	Unit
V <sub>DD</sub>	External Main Supply Voltage	V <sub>SS</sub> - 0.3	V <sub>SS</sub> + 3.6	V
V <sub>DDA</sub>	External Analog Supply Voltage	V <sub>SSA</sub> - 0.3	V <sub>SSA</sub> + 3.6	V
V <sub>IN</sub>	Input Voltage on I/O	V <sub>SS</sub> - 0.3	V <sub>DD</sub> + 0.3	V
T <sub>A</sub>	Ambient Operating Temperature Range	-40	+85	°C
T <sub>STG</sub>	Storage Temperature Range	-55	+150	°C
T <sub>J</sub>	Maximum Junction Temperature	—	+125	°C
P <sub>D</sub>	Total Power Dissipation	—	500	mW
V <sub>ESD</sub>	Electrostatic Discharge Voltage – Human Body Mode	-4000	+4000	V

## Recommended DC Operating Conditions

**Table 6. Recommended DC Operating Conditions**

T<sub>A</sub> = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Main & I/O Operating Voltage	T <sub>A</sub> = -40 °C ~ +85 °C	2.0	3.3	3.6	V
V <sub>DDA</sub>	Analog Operating Voltage	T <sub>A</sub> = -40 °C ~ +85 °C	2.5	3.3	3.6	V

## On-Chip LDO Voltage Regulator Characteristics

**Table 7. LDO Characteristics**

T<sub>A</sub> = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>LDO</sub>	Internal Regulator Output Voltage	V <sub>DD</sub> ≥ 2.0 V Regulator input @ I <sub>LDO</sub> = 35 mA and voltage variant = ±5 %, After trimming.	1.425	1.5	1.57	V
I <sub>LDO</sub>	Output Current	V <sub>DD</sub> = 2.0 V Regulator input @ V <sub>LDO</sub> = 1.5 V	—	30	35	mA
C <sub>LDO</sub>	External Filter Capacitor Value for Internal Core Power Supply	The capacitor value is dependent on the core power current consumption	—	1	—	μF

## Power Consumption

**Table 8. HT32F52243/52253 Power Consumption Characteristics**

Symbol	Parameter	Conditions	Typ. Max.			Unit
			T <sub>A</sub> = 25 °C	T <sub>A</sub> = 25 °C	T <sub>A</sub> = 85 °C	
I <sub>DD</sub>	Supply Current (Run Mode)	V <sub>DD</sub> = 3.3 V, HSI = 8 MHz, PLL = 40 MHz, f <sub>CPU</sub> = 40 MHz, f <sub>BUS</sub> = 40 MHz, all peripherals enabled	12.8	14.6	—	mA
		V <sub>DD</sub> = 3.3 V, HSI = 8 MHz, PLL = 40 MHz, f <sub>CPU</sub> = 40 MHz, f <sub>BUS</sub> = 40 MHz, all peripherals disabled	6.7	7.6	—	mA
		V <sub>DD</sub> = 3.3 V, HSI off, PLL off, LSI on, f <sub>CPU</sub> = 32 kHz, f <sub>BUS</sub> = 32 kHz, all peripherals enabled	45	60	—	μA
		V <sub>DD</sub> = 3.3 V, HSI off, PLL off, LSI on, f <sub>CPU</sub> = 32 kHz, f <sub>BUS</sub> = 32 kHz, all peripherals disabled	40	53	—	μA
	Supply Current (Sleep Mode)	V <sub>DD</sub> = 3.3 V, HSI = 8 MHz, PLL = 40 MHz, f <sub>CPU</sub> = 0 MHz, f <sub>BUS</sub> = 40 MHz, all peripherals enabled	8.2	9.4	—	mA
		V <sub>DD</sub> = 3.3 V, HSI = 8 MHz, PLL = 40 MHz, f <sub>CPU</sub> = 0 MHz, f <sub>BUS</sub> = 40 MHz, all peripherals disabled	1.25	1.45	—	mA
	Supply Current (Deep-Sleep1 Mode)	V <sub>DD</sub> = 3.3 V, All clock off (HSE/HSI/PLL/LSE), LDO in low power mode, LSI on, RTC on	33.2	50.8	—	μA
	Supply Current (Deep-Sleep2 Mode)	V <sub>DD</sub> = 3.3 V, All clock off (HSE/HSI/PLL/LSE), LDO off, DMOS on, LSI on, RTC on	4.6	7.0	—	μA
	Supply Current (Power-Down Mode)	V <sub>DD</sub> = 3.3 V, LDO off, DMOS off, LSE off, LSI on, RTC on	1.40	2.15	—	μA
		V <sub>DD</sub> = 3.3 V, LDO off, DMOS off, LSE off, LSI on, RTC off	1.35	2.10	—	μA

- Note: 1. HSE means high speed external oscillator. HSI means 8 MHz high speed internal oscillator.  
 2. LSE means 32.768 kHz low speed external oscillator. LSI means 32 kHz low speed internal oscillator.  
 3. RTC means real time clock.  
 4. Code = while (1) { 208 NOP } executed in Flash.  
 5. f<sub>BUS</sub> means f<sub>HCLK</sub> and f<sub>PCLK</sub>.

## Reset and Supply Monitor Characteristics

**Table 9. V<sub>DD</sub> Power Reset Characteristics**

T<sub>A</sub> = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>POR</sub>	Power On Reset Threshold (Rising Voltage on V <sub>DD</sub> )	T <sub>A</sub> = -40 °C ~ +85 °C	1.66	1.79	1.90	V
V <sub>PDR</sub>	Power Down Reset Threshold (Falling Voltage on V <sub>DD</sub> )		1.49	1.64	1.78	V
V <sub>PORHYST</sub>	POR Hysteresis	—	—	150	—	mV
t <sub>POR</sub>	Reset Delay Time	V <sub>DD</sub> = 3.3 V	—	0.1	0.2	ms

- Note: 1. Data based on characterization results only, not tested in production.  
 2. Guaranteed by design, not tested in production.  
 3. If the LDO is turned on, the V<sub>DD</sub> POR has to be in the de-assertion condition. When the V<sub>DD</sub> POR is in the assertion state then the LDO will be turned off.

**Table 10. LVD/BOD Characteristics**

T<sub>A</sub> = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	
V <sub>BOD</sub>	Voltage of Brown Out Detection	T <sub>A</sub> = -40 °C ~ 85 °C After factory-trimmed (V <sub>DD</sub> Falling edge)	2.02	2.1	2.18	V	
V <sub>LVD</sub>	Voltage of Low Voltage Detection	T <sub>A</sub> = -40 °C ~ 85 °C (V <sub>DD</sub> Falling edge)	LVDS = 000	2.17	2.25	2.33	V
			LVDS = 001	2.32	2.4	2.48	V
			LVDS = 010	2.47	2.55	2.63	V
			LVDS = 011	2.62	2.7	2.78	V
			LVDS = 100	2.77	2.85	2.93	V
			LVDS = 101	2.92	3.0	3.08	V
			LVDS = 110	3.07	3.15	3.23	V
			LVDS = 111	3.22	3.3	3.38	V
V <sub>LVDHTST</sub>	LVD Hysteresis	V <sub>DD</sub> = 3.3 V	—	—	100	mV	
t <sub>suLVD</sub>	LVD Setup Time	V <sub>DD</sub> = 3.3 V	—	—	—	5 μs	
t <sub>atLVD</sub>	LVD Active Delay Time	V <sub>DD</sub> = 3.3 V	—	—	—	μs	
I <sub>DDLVD</sub>	Operation Current <sup>(3)</sup>	V <sub>DD</sub> = 3.3 V	—	—	5	15 μA	

- Note: 1. Data based on characterization results only, not tested in production.  
 2. Guaranteed by design, not tested in production.  
 3. Bandgap current is not included.  
 4. LVDS field is in the PWRCU LVDCSR register

## External Clock Characteristics

**Table 11. High Speed External Clock (HSE) Characteristics**

T<sub>A</sub> = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Operation Range	—	2.0	—	3.6	V
f <sub>HSE</sub>	High Speed External Oscillator Frequency (HSE)	—	4	—	16	MHz
C <sub>LHSE</sub>	Load Capacitance	V <sub>DD</sub> = 3.3 V, R <sub>ESR</sub> = 100 Ω @ 16 MHz	—	—	22	pF
R <sub>FHSE</sub>	Internal Feedback Resistor between XTALIN and XTALOUT Pins	—	—	1	—	MΩ
R <sub>ESR</sub>	Equivalent Series Resistance*	V <sub>DD</sub> = 3.3 V, C <sub>L</sub> = 12 pF @ 16 MHz, HSEDR = 0	—	—	160	Ω
		V <sub>DD</sub> = 2.4 V, C <sub>L</sub> = 12 pF @ 16 MHz, HSEDR = 1	—	—	—	—
D <sub>HSE</sub>	HSE Oscillator Duty Cycle	—	40	—	60	%
I <sub>DDHSE</sub>	HSE Oscillator Current Consumption	V <sub>DD</sub> = 3.3 V @ 16 MHz	—	TBD	—	mA
I <sub>PWDHSE</sub>	HSE Oscillator Power Down Current	V <sub>DD</sub> = 3.3 V	—	—	0.01	μA
t <sub>SUHSE</sub>	HSE Oscillator Startup Time	V <sub>DD</sub> = 3.3 V	—	—	4	ms

**Table 12. Low Speed External Clock (LSE) Characteristics**

$T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{DD}$	Operation Range	—	2.0	—	3.6	V
$f_{CK\_LSE}$	LSE Frequency	$V_{DD} = 2.0\text{ V} \sim 3.6\text{ V}$	—	32.768	—	kHz
$R_F$	Internal Feedback Resistor	—	—	10	—	M $\Omega$
$R_{ESR}$	Equivalent Series Resistance	$V_{DD} = 3.3\text{ V}$	30	—	TBD	k $\Omega$
$C_L$	Recommended Load Capacitances	$V_{DD} = 3.3\text{ V}$	6	—	TBD	pF
$I_{DDLSE}$	Oscillator Supply Current (High Current Mode)	$f_{CK\_LSE} = 32.768\text{ kHz}$ , $R_{ESR} = 50\text{ k}\Omega$ , $C_L \geq 7\text{ pF}$ $V_{DD} = 2.0\text{ V} \sim 2.7\text{ V}$ $T_A = -40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$	—	3.3	6.3	$\mu\text{A}$
	Oscillator Supply Current (Low Current Mode)	$f_{CK\_LSE} = 32.768\text{ kHz}$ , $R_{ESR} = 50\text{ k}\Omega$ , $C_L < 7\text{ pF}$ $V_{DD} = 2.0\text{ V} \sim 3.6\text{ V}$ $T_A = -40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$	—	1.8	3.3	$\mu\text{A}$
	Power Down Current	—	—	—	0.01	$\mu\text{A}$
$t_{suLSE}$	Startup Time (Low Current Mode)	$f_{CK\_LSI} = 32.768\text{ kHz}$ , $V_{DD} = 2.0\text{ V} \sim 3.6\text{ V}$	500	—	—	ms

Note: The following guidelines are recommended to increase the stability of the crystal circuit of the HSE / LSE clock in the PCB layout:

- The crystal oscillator should be located as close as possible to the MCU to keep the trace lengths as short as possible to reduce any parasitic capacitance.
- Shield lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
- Keep any high frequency signal lines away from the crystal area to prevent any crosstalk adverse effects.

## Internal Clock Characteristics

**Table 13. High Speed Internal Clock (HSI) Characteristics**

$T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{DD}$	Operation Range	—	2.0	—	3.6	V
$f_{HSI}$	HSI Frequency	$V_{DD} = 3.3\text{ V} @ 25\text{ }^\circ\text{C}$	—	8	—	MHz
$ACC_{HSI}$	Factory Calibrated HSI Oscillator Frequency Accuracy	$V_{DD} = 3.3\text{ V}$ , $T_A = 25\text{ }^\circ\text{C}$	-2	—	2	%
		$V_{DD} = 2.5\text{ V} \sim 3.6\text{ V}$ , $T_A = -40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$	-3	—	3	%
		$V_{DD} = 2.0\text{ V} \sim 3.6\text{ V}$ , $T_A = -40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$	-4	—	4	%
Duty	Duty Cycle	$f_{HSI} = 8\text{ MHz}$	35	—	65	%
$I_{DDHSI}$	Oscillator Supply Current	$f_{HSI} = 8\text{ MHz}$	—	300	500	$\mu\text{A}$
	Power Down Current		—	—	0.05	$\mu\text{A}$
$t_{suHSI}$	Startup Tme	$f_{HSI} = 8\text{ MHz}$	—	—	10	$\mu\text{s}$



**Table 14. Low Speed Internal Clock (LSI) Characteristics**

$T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$f_{LSI}$	Low Speed Internal Oscillator Frequency (LSI)	$V_{DD} = 3.3\text{ V}$ , $T_A = -40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$	21	32	43	kHz
$ACC_{LSI}$	LSI Frequency Accuracy	After factory-trimmed, $V_{DD} = 3.3\text{ V}$ , $T_A = 25\text{ }^\circ\text{C}$	-10	—	+10	%
$I_{DDLSI}$	LSI Oscillator Operating Current	$V_{DD} = 3.3\text{ V}$ , $T_A = 25\text{ }^\circ\text{C}$	—	0.4	0.8	$\mu\text{A}$
$t_{SULSI}$	LSI Oscillator Startup Time	$V_{DD} = 3.3\text{ V}$ , $T_A = 25\text{ }^\circ\text{C}$	—	—	100	$\mu\text{s}$

## PLL Characteristics

**Table 15. PLL Characteristics**

$T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$f_{PLLIN}$	PLL Input Clock	—	4	—	16	MHz
$f_{CK\_PLL}$	PLL Output Clock	—	16	—	48	MHz
$t_{LOCK}$	PLL Lock Time	—	—	200	—	$\mu\text{s}$

## Memory Characteristics

**Table 16. Flash Memory Characteristics**

$T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$N_{ENDU}$	Number of Guaranteed Program/erase Cycles before Failure. (Endurance)	$T_A = -40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$	10	—	—	K cycles
$t_{RET}$	Data Retention Time	$T_A = -40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$	10	—	—	Years
$t_{PROG}$	Word Programming Time	$T_A = -40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$	20	—	—	$\mu\text{s}$
$t_{ERASE}$	Page Erase Time	$T_A = -40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$	2	—	—	ms
$t_{MERASE}$	Mass Erase Time	$T_A = -40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$	10	—	—	ms

## I/O Port Characteristics

**Table 17. I/O Port Characteristics**

$T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	
$I_{IL}$	Low Level Input Current	3.3 V I/O	$V_I = V_{SS}$ , On-chip pull-up resistor disabled.	—	—	3	$\mu\text{A}$
		Reset pin		—	—	3	$\mu\text{A}$
$I_{IH}$	High Level Input Current	3.3 V I/O	$V_I = V_{DD}$ , On-chip pull-down resistor disabled.	—	—	3	$\mu\text{A}$
		Reset pin		—	—	3	$\mu\text{A}$
$V_{IL}$	Low Level Input Voltage	3.3 V I/O	—	—	$V_{DD} \times 0.35$	V	
		Reset pin	—	—	$V_{DD} \times 0.35$	V	
$V_{IH}$	High Level Input Voltage	3.3 V I/O	$V_{DD} \times 0.65$	—	$V_{DD} + 0.5$	V	
		Reset pin	$V_{DD} \times 0.65$	—	$V_{DD} + 0.5$	V	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>HYS</sub>	Schmitt Trigger Input Voltage Hysteresis	3.3 V I/O	—	0.12 × V <sub>DD</sub>	—	mV
		Reset pin	—	0.12 × V <sub>DD</sub>	—	mV
I <sub>OL</sub>	Low Level Output Current (GPIO Sink Current)	3.3 V I/O 4 mA drive, V <sub>OL</sub> = 0.4 V	4	—	—	mA
		3.3 V I/O 8 mA drive, V <sub>OL</sub> = 0.4 V	8	—	—	mA
		3.3 V I/O 12 mA drive, V <sub>OL</sub> = 0.4 V	12	—	—	mA
		3.3 V I/O 16 mA drive, V <sub>OL</sub> = 0.4 V	16	—	—	mA
I <sub>OH</sub>	High Level Output Current (GPIO Source Current)	3.3 V I/O 4 mA drive, V <sub>OH</sub> = V <sub>DD</sub> - 0.4 V	4	—	—	mA
		3.3 V I/O 8 mA drive, V <sub>OH</sub> = V <sub>DD</sub> - 0.4 V	8	—	—	mA
		3.3 V I/O 12 mA drive, V <sub>OH</sub> = V <sub>DD</sub> - 0.4 V	12	—	—	mA
		3.3 V I/O 16 mA drive, V <sub>OH</sub> = V <sub>DD</sub> - 0.4 V	16	—	—	mA
V <sub>OL</sub>	Low Level Output Voltage	3.3 V 4 mA drive I/O, I <sub>OL</sub> = 4 mA	—	—	0.4	V
		3.3 V 8 mA drive I/O, I <sub>OL</sub> = 8 mA	—	—	0.4	V
		3.3 V 12 mA drive I/O, I <sub>OL</sub> = 12 mA	—	—	0.4	V
		3.3 V 16 mA drive I/O, I <sub>OL</sub> = 16 mA	—	—	0.4	V
V <sub>OH</sub>	High Level Output Voltage	3.3 V 4 mA drive I/O, I <sub>OH</sub> = 4 mA	V <sub>DD</sub> - 0.4	—	—	V
		3.3 V 8 mA drive I/O, I <sub>OH</sub> = 8 mA	V <sub>DD</sub> - 0.4	—	—	V
		3.3 V 12 mA drive I/O, I <sub>OL</sub> = 12 mA	V <sub>DD</sub> - 0.4	—	—	V
		3.3 V 16 mA drive I/O, I <sub>OL</sub> = 16 mA	V <sub>DD</sub> - 0.4	—	—	V
R <sub>PU</sub>	Internal Pull-up Resistor	3.3 V I/O	—	46	—	kΩ
R <sub>PD</sub>	Internal Pull-down Resistor	3.3 V I/O	—	46	—	kΩ

## ADC Characteristics

Table 18. ADC Characteristics

T<sub>A</sub> = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>DDA</sub>	Operating Voltage	—	2.5	3.3	3.6	V
V <sub>ADCIN</sub>	A/D Converter Input Voltage Range	—	0	—	V <sub>REF+</sub>	V
V <sub>REF+</sub>	A/D Converter Reference voltage	—	—	V <sub>DDA</sub>	V <sub>DDA</sub>	V
I <sub>ADC</sub>	Current consumption	V <sub>DDA</sub> = 3.3 V	—	1	TBD	mA
I <sub>ADC_DN</sub>	Power down current consumption	V <sub>DDA</sub> = 3.3 V	—	—	0.1	µA
f <sub>ADC</sub>	A/D Converter clock	—	0.7	—	16	MHz
f <sub>s</sub>	Sampling rate	—	0.05	—	1	MHz
t <sub>DL</sub>	Data latency	—	—	12.5	—	1/f <sub>ADC</sub> Cycles
t <sub>S&amp;H</sub>	Sampling & hold time	—	—	3.5	—	1/f <sub>ADC</sub> Cycles
t <sub>ADCCONV</sub>	A/D Converter conversion time	—	—	16	—	1/f <sub>ADC</sub> Cycles
R <sub>I</sub>	Input sampling switch resistance	—	—	—	1	kΩ
C <sub>I</sub>	Input sampling capacitance	No pin/pad capacitance included	—	16	—	pF
t <sub>SU</sub>	Startup time	—	—	—	1	µs
N	Resolution	—	—	12	—	bits
INL	Integral Non-linearity error	f <sub>s</sub> = 750 kHz, V <sub>DDA</sub> = 3.3 V	—	±2	±5	LSB
DNL	Differential Non-linearity error	f <sub>s</sub> = 750 kHz, V <sub>DDA</sub> = 3.3 V	—	±1	—	LSB
E <sub>O</sub>	Offset error	—	—	—	±10	LSB
E <sub>G</sub>	Gain error	—	—	—	±10	LSB

Note: 1. Guaranteed by design, not tested in production.

- Due to the A/D Converter input channel and GPIO pin-shared function design limitation, the V<sub>DDA</sub> supply power of the A/D Converter has to be equal to the V<sub>DD</sub> supply power of the MCU in the application circuit.
- The figure below shows the equivalent circuit of the A/D Converter Sample-and-Hold input stage where C<sub>I</sub> is the storage capacitor, R<sub>I</sub> is the resistance of the sampling switch and R<sub>S</sub> is the output impedance of the signal source V<sub>S</sub>. Normally the sampling phase duration is approximately, 3.5/f<sub>ADC</sub>. The capacitance, C<sub>I</sub>, must be charged within this time frame and it must be ensured that the voltage at its terminals becomes sufficiently close to V<sub>S</sub> for accuracy. To guarantee this, R<sub>S</sub> is not allowed to have an arbitrarily large value.

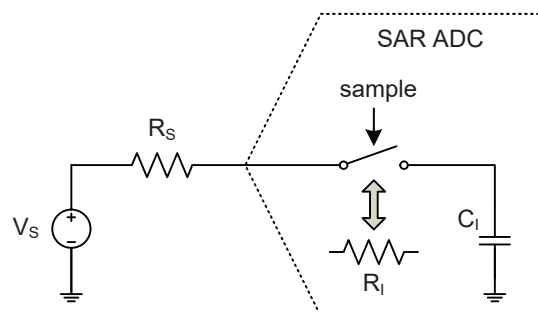


Figure 8. ADC Sampling Network Model

The worst case occurs when the extremities of the input range (0V and V<sub>REF</sub>) are sampled consecutively. In this situation a sampling error below ¼ LSB is ensured by using the following equation:

$$R_S < \frac{3.5}{f_{ADC} C_I \ln(2^{N+2})} - R_I$$

Where f<sub>ADC</sub> is the ADC clock frequency and N is the ADC resolution (N = 12 in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model.

If, in a system where the A/D Converter is used, there are no rail-to-rail input voltage variations between consecutive sampling phases, R<sub>S</sub> may be larger than the value indicated by the equation above.

## SCTM/GPTM/MCTM Characteristics

**Table 19. SCTM/GPTM/MCTM Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f <sub>TM</sub>	Timer clock source for GPTM and MCTM	—	—	—	40	MHz
t <sub>RES</sub>	Timer resolution time	—	1	—	—	f <sub>TM</sub>
f <sub>EXT</sub>	External single frequency on channel 1 ~ 4	—	—	—	1/2	f <sub>TM</sub>
RES	Timer resolution	—	—	—	16	bits

## I<sup>2</sup>C Characteristics

**Table 20. I<sup>2</sup>C Characteristics**

Symbol	Parameter	Standard mode		Fast mode		Fast mode plus		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f <sub>SCL</sub>	SCL clock frequency	—	100	—	400	—	1000	kHz
t <sub>SCL(H)</sub>	SCL clock high time	4.5	—	1.125	—	0.45	—	µs
t <sub>SCL(L)</sub>	SCL clock low time	4.5	—	1.125	—	0.45	—	µs
t <sub>FALL</sub>	SCL and SDA fall time	—	1.3	—	0.34	—	0.135	µs
t <sub>RISE</sub>	SCL and SDA rise time	—	1.3	—	0.34	—	0.135	µs
t <sub>SU(SDA)</sub>	SDA data setup time	500	—	125	—	50	—	ns
t <sub>H(SDA)</sub>	SDA data hold time <sup>(Note 5)</sup>	0	—	0	—	0	—	ns
	SDA data hold time <sup>(Note 6)</sup>	100	—	100	—	100	—	ns
t <sub>VD(SDA)</sub>	SDA data valid time	—	1.6	—	0.475	—	0.25	µs
t <sub>SU(STA)</sub>	START condition setup time	500	—	125	—	50	—	ns
t <sub>H(STA)</sub>	START condition hold time	0	—	0	—	0	—	ns
t <sub>SU(STO)</sub>	STOP condition setup time	500	—	125	—	50	—	ns

Note: 1. Guaranteed by design, not tested in production.

2. To achieve 100 kHz standard mode, the peripheral clock frequency must be higher than 2 MHz.

3. To achieve 400 kHz fast mode, the peripheral clock frequency must be higher than 8 MHz.

4. To achieve 1 MHz fast mode plus, the peripheral clock frequency must be higher than 20 MHz.

5. The above characteristic parameters of the I<sup>2</sup>C bus timing are based on: COMB\_FILTER\_En = 0 and SEQ\_FILTER = 00.

6. The above characteristic parameters of the I<sup>2</sup>C bus timing are based on: COMB\_FILTER\_En = 1 and SEQ\_FILTER = 00.

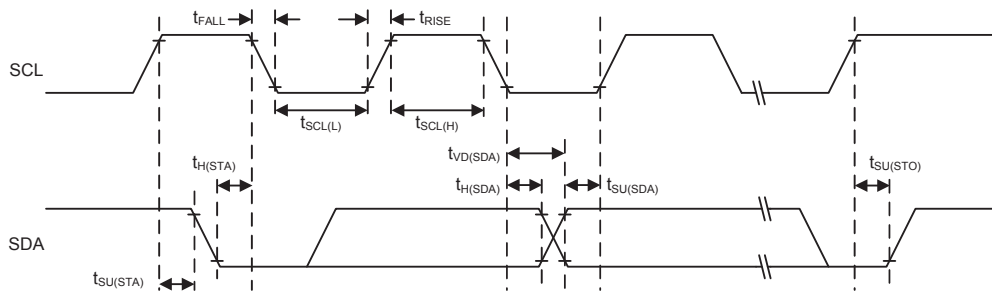


Figure 9. I<sup>2</sup>C Timing Diagrams

## SPI Characteristics

Table 21. SPI Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>SPI Master mode</b>						
$f_{SCK}$ ( $1/t_{SCK}$ )	SPI master output SCK clock frequency	Master mode SPI peripheral clock frequency $f_{PCLK}$	—	—	$f_{PCLK}/2$	MHz
$t_{SCK(H)}$ $t_{SCK(L)}$	SCK clock high and low time	—	$t_{SCK}/2 - 2$	—	$t_{SCK}/2 + 1$	ns
$t_{V(MO)}$	Data output valid time	—	—	—	5	ns
$t_{H(MO)}$	Data output hold time	—	2	—	—	ns
$t_{SU(MI)}$	Data input setup time	—	5	—	—	ns
$t_{H(MI)}$	Data input hold time	—	5	—	—	ns
<b>SPI Slave mode</b>						
$f_{SCK}$ ( $1/t_{SCK}$ )	SPI slave input SCK clock frequency	Slave mode SPI peripheral clock frequency $f_{PCLK}$	—	—	$f_{PCLK}/3$	MHz
Duty <sub>SCK</sub>	SPI slave input SCK clock duty cycle	—	30	—	70	%
$t_{SU(SEL)}$	SEL enable setup time	—	$3 \times t_{PCLK}$	—	—	ns
$t_{H(SEL)}$	SEL enable hold time	—	$2 \times t_{PCLK}$	—	—	ns
$t_{A(SO)}$	Data output access time	—	—	—	$3 \times t_{PCLK}$	ns
$t_{DIS(SO)}$	Data output disable time	—	—	—	10	ns
$t_{V(SO)}$	Data output valid time	—	—	—	25	ns
$t_{H(SO)}$	Data output hold time	—	15	—	—	ns
$t_{SU(SI)}$	Data input setup time	—	5	—	—	ns
$t_{H(SI)}$	Data input hold time	—	4	—	—	ns

Note:  $t_{SCK} = 1/f_{SCK}$ ;  $t_{PCLK} = 1/f_{PCLK}$ . SPI output (input) clock frequency  $f_{SCK}$ ; SPI peripheral clock frequency  $f_{PCLK}$ .

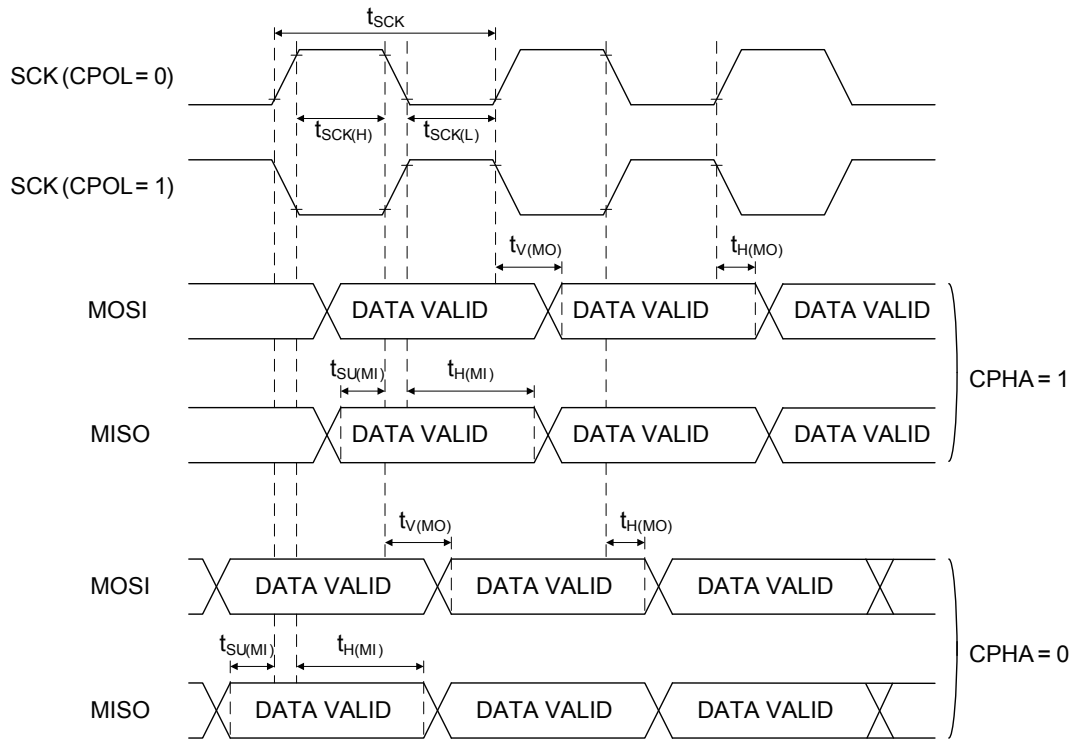


Figure 10. SPI Timing Diagrams – SPI Master Mode

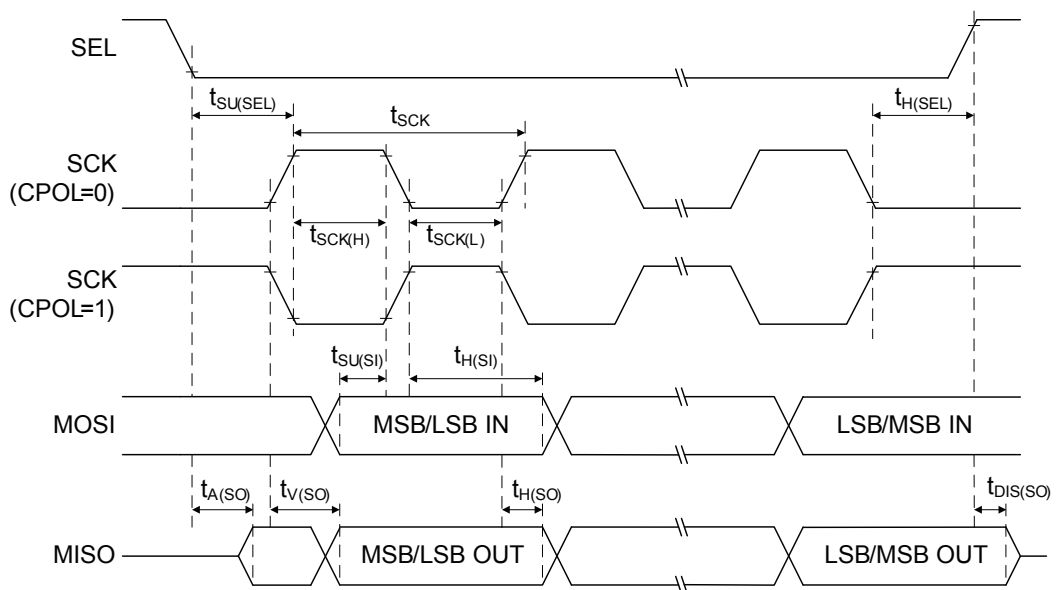


Figure 11. SPI Timing Diagrams – SPI Slave Mode with CPHA=1

## 6 Package Information

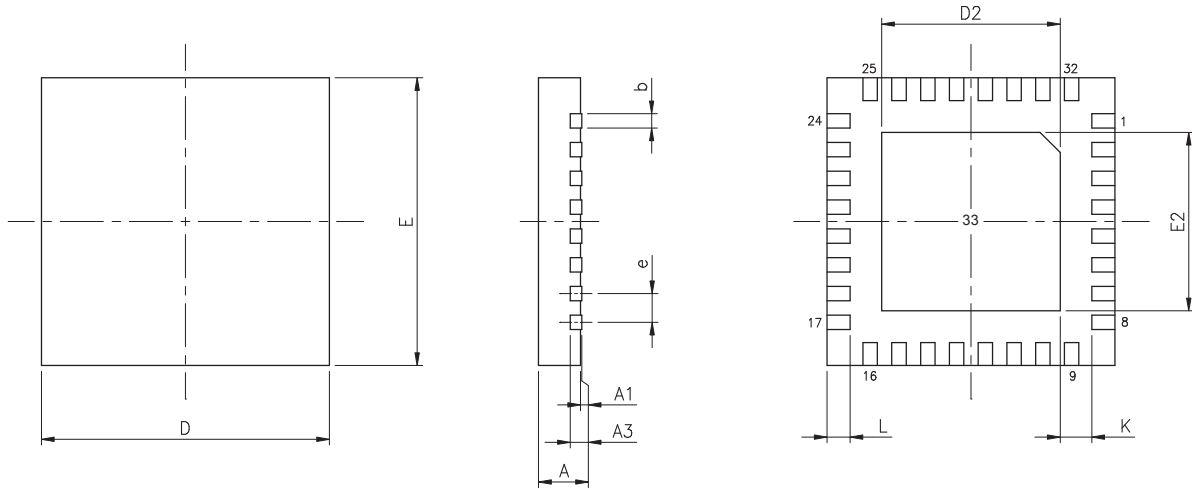
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Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the [Holtek website](#) for the latest version of the [Package/Carton Information](#).

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

## SAW Type 33-pin (4mm × 4mm) QFN Outline Dimensions

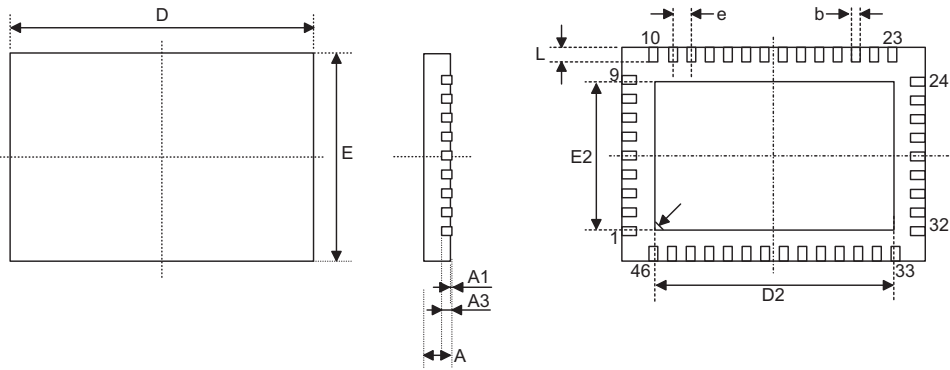


Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3	—	0.008 BSC	—
b	0.006	0.008	0.010
D	—	0.157 BSC	—
E	—	0.157 BSC	—
e	—	0.016 BSC	—
D2	0.104	0.106	0.108
E2	0.104	0.106	0.108
L	0.014	0.016	0.018
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
A3	—	0.203 BSC	—
b	0.150	0.200	0.250
D	—	4.000 BSC	—
E	—	4.000 BSC	—
e	—	0.400 BSC	—
D2	2.650	2.700	2.750
E2	2.650	2.700	2.750
L	0.350	0.400	0.450
K	0.200	—	—



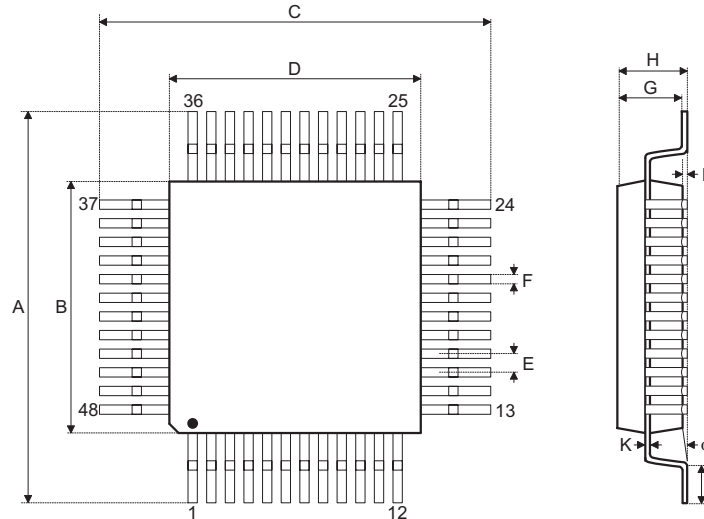
## SAW Type 46-pin (6.5mm × 4.5mm) QFN Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.031	0.033	0.035
A1	0.000	0.001	0.002
A3	—	0.008 BSC	—
b	0.006	0.008	0.010
D	0.254	0.256	0.258
E	0.175	0.177	0.179
e	—	0.016 BSC	—
D2	0.197	0.201	0.205
E2	0.118	0.122	0.126
L	0.012	0.016	0.020

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.800	0.850	0.900
A1	0.000	0.020	0.040
A3	—	0.200 BSC	—
b	0.150	0.200	0.250
D	6.450	6.500	6.550
E	4.450	4.500	4.550
e	—	0.40 BSC	—
D2	5.00	5.10	5.20
E2	3.00	3.10	3.20
L	0.30	0.40	0.50

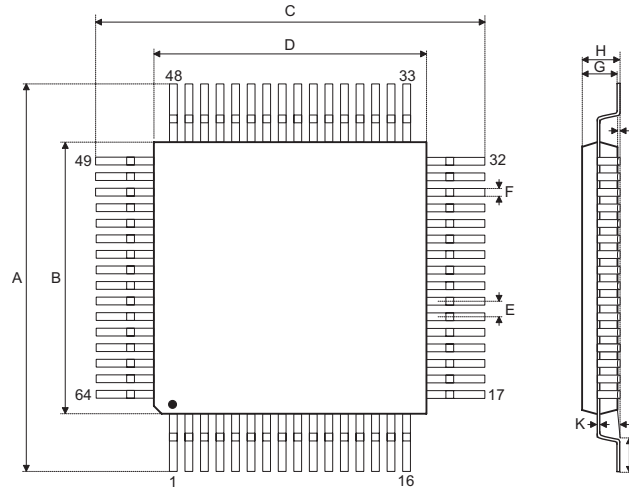
## 48-pin LQFP (7mm × 7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.020 BSC	—
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.00 BSC	—
B	—	7.00 BSC	—
C	—	9.00 BSC	—
D	—	7.00 BSC	—
E	—	0.50 BSC	—
F	0.17	0.22	0.27
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

## 64-pin LQFP (7mm × 7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.016 BSC	—
F	0.005	0.007	0.009
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.0 BSC	—
B	—	7.0 BSC	—
C	—	9.0 BSC	—
D	—	7.0 BSC	—
E	—	0.4 BSC	—
F	0.13	0.18	0.23
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

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