# HT32F50231/HT32F50241
# Datasheet

**32-Bit Arm® Cortex®-M0+ Microcontroller,**
**up to 64 KB Flash and 8 KB SRAM with 1 MSPS ADC,**
**DIV, USART, UART, SPI, I²C, MCTM, GPTM,**
**BFTM, PWM, CRC, RTC and WDT**

Revision: V1.30 Date: September 19, 2019

www.holtek.com

# Table of Contents

# List of Tables

# List of Figures

# 1 General Description

The Holtek HT32F50231/50241 devices are high performance, low power consumption 32-bit microcontrollers based around an Arm® Cortex®-M0+ processor core. The Cortex®-M0+ is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer, and including advanced debug support.

The devices operate at a frequency of up to 20 MHz with a Flash accelerator to obtain maximum efficiency. It provides up to 64 KB of embedded Flash memory for code/data storage and 8 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as Hardware Divider DIV, ADC, $I^2C$, USART, UART, SPI, MCTM, GPTM, PWM, BFTM, CRC-16/32, RTC, WDT, SW-DP (Serial Wire Debug Port), etc., are also implemented in the devices. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features ensure that the devices are suitable for use in a wide range of applications, especially in areas such as white goods application controllers, power monitors, alarm systems, consumer products, handheld equipment, data logging applications, motor controllers and so on.

# 2 Features



## Core

- 32-bit Arm® Cortex®-M0+ processor core
- Up to 20 MHz operating frequency
- Single-cycle multiplication
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized, low-power processor. The processor is based on the ARMv6-M architecture and supports Thumb® instruction sets, single-cycle I/O port, hardware multiplier and low latency interrupt respond time.

## On-chip Memory

- Up to 64 KB on-chip Flash memory for instruction/data and options storage
- Up to 8 KB on-chip SRAM
- Supports multiple boot modes

The Arm® Cortex®-M0+ processor accesses and debug accesses share the single external interface to external AHB peripherals. The processor accesses take priority over debug accesses. The maximum address range of the Cortex®-M0+ is 4 GB since it has a 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex®-M0+ processor to reduce the software complexity of repeated implementation by different device vendors. However, some regions are used by the Arm® Cortex®-M0+ system peripherals. Refer to the Arm® Cortex®-M0+ Technical Reference Manual for more information. Figure 2 in the Overview chapter shows the memory map of the HT32F50231/50241 series devices, including code, SRAM, peripheral and other pre-defined regions.

## Flash Memory Controller – FMC

- 32-bit word programming with In System Programming Interface (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions for the embedded on-chip Flash Memory. The word program/page erase functions are also provided.

## Reset Control Unit – RSTCU

- Supply supervisor:
  - Power on Reset / Power down Reset – POR / PDR
  - Brown-out Detector – BOD
  - Programmable Low Voltage Detector – LVD

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by external signals, internal events and the reset generators.

## Clock Control Unit – CKCU

- External 4 to 20 MHz crystal oscillator
- External 32.768 kHz crystal oscillator
- Internal 20 MHz RC oscillator trimmed to ±2 % accuracy at 25 °C operating temperature
- Internal 32 kHz RC oscillator
- Independent clock divider and gating bits for peripheral clock sources

The Clock Control Unit, CKCU, provides a range of oscillator and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), an HSE clock monitor, clock pre-scalers, clock multiplexers, APB clock divider and gating circuitry. The AHB, APB and Cortex®-M0+ clocks are derived from the system clock (CK_SYS) which can come from the HSI, HSE, LSI or LSE. The Watchdog Timer and Real Time Clock (RTC) use either the LSI or LSE as their clock source.

## Power Management Control Unit – PWRCU

- Flexible power supply: $V_{DD}$ power supply (2.5 V ~ 5.5 V), $V_{DDIO}$ for I/Os (1.8 V ~ 5.5 V)
- Integrated 1.5 V LDO regulator for CPU core, peripherals and memories power supply
- Three power domains: $V_{DD}$, $V_{DDIO}$ and 1.5 V
- Three power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in these devices provides many types of power saving modes such as Sleep, Deep-Sleep1 and Deep-Sleep2 mode. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.

## Real Time Clock – RTC

- 24-bit up-counter with a programmable prescaler
- Alarm function
- Interrupt and Wake-up event

The Real Time Clock, RTC, includes an APB interface, a 24-bit count-up counter, a control register, a prescaler, a compare register and a status register. The RTC circuits are located in the $V_{DD15}$ power domain. The RTC counter is used as a wakeup timer to generate a system resume or interrupt signal from the MCU power saving mode.

## External Interrupt/Event Controller – EXTI

- Up to 16 EXTI lines with configurable trigger source and type
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge, or both edges
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

The External Interrupt/Event Controller, EXTI, comprises 16 edge detectors which can generate a wake-up event or interrupt requests independently. Each EXTI line can also be masked independently.

## Hardware Divider – DIV

- Signed/unsigned 32-bit divider
- Operation in 8 clock cycles, load in 1 clock cycle
- Divide by zero error Flag

The divider is the truncated division and needs a software triggered start signal by using the control register "START" bit. After 8 clock cycles, the divider calculate complete flag will be set to 1, and if the divisor register data is zero, the divide by zero error flag will be set to 1.

## Analog to Digital Converter – ADC

- 12-bit SAR ADC engine
- Up to 1 Msps conversion rate
- Up to 12 external analog input channels

A 12-bit multi-channel ADC is integrated in these devices. There are multiplexed channels, which include 12 external analog signal channels and 2 internal channels which can be measured. If the input voltage is required to remain within a specific threshold window, an Analog Watchdog function will monitor and detect these signals. An interrupt will then be generated to inform the device that the input voltage is not within the preset threshold levels. There are three conversion modes to convert an analog signal to digital data. The ADC can be operated in one shot, continuous and discontinuous conversion modes.

## I/O Ports – GPIO

- Up to 40 GPIOs
- Port A, B, C are mapped as 16 external interrupts – EXTI
- Almost all I/O pins have configurable output driving current

There are up to 40 General Purpose I/O pins, GPIO, named PA0 ~ PA15, PB0 ~ PB15 and PC0 ~ PC7 for the implementation of logic input/output functions. Each of the GPIO ports has a series of related control and configuration registers to maximize flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

## Basic Function Timer – BFTM

- 32-bit compare match count-up counter – no I/O control features
- One shot mode – counting stops after compare match occurs
- Repetitive mode – restart counter when compare match occurs

The Basic Function Timer is a simple 32-bit up-counting counter designed to measure time intervals and generate a one shot or repetitive interrupts. The BFTM operates in two functional modes, repetitive and one shot modes. In the repetitive mode, the BFTM restarts the counter when a compare match event occurs. The BFTM also supports a one shot mode which forces the counter to stop counting when a compare match event occurs.

## Motor Control Timer – MCTM

- 16-bit up/down auto-reload counter
- 16-bit programmable prescaler allowing counter clock frequency divided by any factor between 1 and 65536
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output
- Complementary Outputs with programmable dead-time insertion
- Break input to force the timer's output signals into a reset or fixed condition

The Motor Control Timer consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR), one 8-bit repetition counter and several control/status registers. It can be used for a variety of purposes including measuring the pulse width of input signals or generating output waveforms such as compare match outputs, PWM outputs or complementary PWM outputs with dead-time insertion. The MCTM is capable of offering full functional support for motor control, hall sensor interfacing and break input.

## PWM Generation and Capture Timer – GPTM

- 16-bit up/down auto-reload counter
- Up to 4 independent channels for each timer
- 16-bit programmable prescaler allowing the counter clock frequency devided by any factor between 1 and 65536
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder

The General Purpose Timer consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR) and several control/status registers. They can be used for a variety of purposes including general time measurement, input signal pulse width measurement, output waveform generation such as single pulse generation or PWM output generation. The GPTM supports an Encoder Interface using a decoder with two inputs.

## Pulse Width Modulation – PWM

- 16-bit up/down auto-reload counter
- Up to 4 independent channels for each timer
- 16-bit programmable prescaler allowing counter clock frequency divided by any factor between 1 and 65536
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output

The Pulse Width Modulator consists of one 16-bit up/down-counter, four 16-bit Compare Registers (CRs), one 16-bit Counter-Reload Register (CRR) and several control/status registers. It can be used for a variety of purposes including general timer and output waveform generation such as single pulse generation or PWM output.

## Watchdog Timer – WDT

- 12-bit down counter with 3-bit prescaler
- Reset event for the system
- Programmable watchdog timer window function
- Register write protection function

The Watchdog Timer is a hardware timing circuit that can be used to detect system failures due to software malfunctions. It includes a 12-bit count-down counter, a prescaler, a WDT delta value register, WDT operation control circuitry and a WDT protection mechanism. If the software does not reload the counter value before a Watchdog Timer underflow occurs, a reset will be generated when the counter underflows. In addition, a reset is also generated if the software reloads the counter when the counter value is greater than the WDT delta value. This means the counter must be reloaded within a limited timing window using a specific method. The Watchdog Timer counter

can be stopped while the processor is in the debug mode. There is a register write protect function which can be enabled to prevent it from changing the Watchdog Timer configuration unexpectedly.

## Inter-integrated Circuit – I²C

- Supports both master and slave modes with a frequency of up to 1 MHz
- Provides an arbitration function and clock synchronization
- Supports 7-bit and 10-bit addressing modes and general call addressing
- Supports slave multi-addressing mode with address mask function

The I²C is an internal circuit allowing communication with an external I²C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I²C module provides three data transfer rates: 100 kHz in the Standard mode, 400 kHz in the Fast mode and 1 MHz in the Fast plus mode. The SCL period generation register is used to setup different kinds of duty cycle implementations for the SCL pulse.

The SDA line which is connected directly to the I²C bus is a bi-directional data line between the master and slave devices and is used for data transmission and reception. The I²C also has an arbitration detect function and clock synchronization to prevent situations where more than one master attempts to transmit data to the I²C bus at the same time.

## Serial Peripheral Interface– SPI

- Supports both master and slave modes
- Frequency of up to ($f_{PCLK}$/2) MHz for the master mode and ($f_{PCLK}$/3) MHz for the slave mode
- FIFO Depth: 8 levels
- Multi-master and multi-slave operation

The Serial Peripheral Interface, SPI, provides a SPI protocol data transmit and receive function in both master and slave modes. The SPI interface uses 4 pins, which are the serial data input and output lines MISO and MOSI, the clock line, SCK, and the slave select line, SEL. One SPI device acts as a master device which controls the data flow using the SEL and SCK signals to indicate the start of data communication and the data sampling rate. To receive a data byte, the streamed data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but in a reverse sequence. The mode fault detection provides a capability for multi-master applications.

## Universal Synchronous Asynchronous Receiver Transmitter – USART

- Supports both asynchronous and clocked synchronous serial communication modes
- Asynchronous operating baud-rate clock frequency up to ($f_{PCLK}$/16) MHz and synchronous operating clock frequency up to ($f_{PCLK}$/8) MHz
- Full duplex communication

- Fully programmable serial communication characteristics including:
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error
- Auto hardware flow control mode – RTS, CTS
- IrDA SIR encoder and decoder
- RS485 mode with output enable control
- FIFO Depth: 8 × 9 bits for both receiver and transmitter

The Universal Synchronous Asynchronous Receiver Transceiver, USART, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. The USART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The USART peripheral function supports four types of interrupt including Line Status Interrupt, Transmitter FIFO Empty Interrupt, Receiver Threshold Level Reaching Interrupt and Time Out Interrupt. The USART module includes a transmitter FIFO (TX_FIFO) and receiver FIFO (RX_FIFO). The software can detect a USART error status by reading the Line Status Register, LSR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

## Universal Asynchronous Receiver Transmitter – UART

- Asynchronous serial communication operating baud-rate clock frequency up to ($f_{PCLK}$/16) MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports Line Status Interrupt. The software can detect a UART error status by reading the Line Status Register, LSR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

## Cyclic Redundancy Check – CRC

- Support CRC16 polynomial: 0x8005,
  $X^{16}+X^{15}+X^{2}+1$
- Support CCITT CRC16 polynomial: 0x1021,
  $X^{16}+X^{12}+X^{5}+1$

- Support IEEE-802.3 CRC32 polynomial: 0x04C11DB7,
  $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^{8}+X^{7}+X^{5}+X^{4}+X^{2}+X+1$
- Supports 1's complement, byte reverse & bit reverse operation on data and checksum
- Supports byte, half-word & word data size
- Programmable CRC initial seed value
- CRC computation executed in 1 AHB clock cycle for 8-bit data and 4 AHB clock cycles for 32-bit data

The CRC calculation unit is an error detection technique test algorithm which is used to verify data transmission or storage data correctness. A CRC calculation takes a data stream or a block of data as its input and generates a 16-bit or 32-bit output remainder. Ordinarily, a data stream is suffixed by a CRC code and used as a checksum when being sent or stored. Therefore, the received or restored data stream is calculated by the same generator polynomial as described above. If the new CRC code result does not match the one calculated earlier, that means the data stream contains a data error.

## Debug Support

- Serial Wire Debug Port – SW-DP
- 4 comparators for hardware breakpoint or code / literal patch
- 2 comparators for hardware watch points

## Package and Operation Temperature

- 24/28-pin SSOP, 28-pin SOP, 24/33/46-pin QFN and 44/48-pin LQFP packages
- Operation temperature range: -40 °C to +85 °C

# 3 Overview

## Device Information

**Table 1. Features and Peripheral List**

| Peripherals | | HT32F50231 | HT32F50241 |
|---|---|---|---|
| Main Flash (KB) | | 32 | 63 |
| Option Bytes Flash (KB) | | 1 | 1 |
| SRAM (KB) | | 4 | 8 |
| Timers | MCTM | 1 | |
| | GPTM | 1 | |
| | PWM | 2 | |
| | BFTM | 2 | |
| | WDT | 1 | |
| | RTC | 1 | |
| Communication | SPI | 2 | |
| | USART | 1 | |
| | UART | 2 | |
| | $I^2C$ | 2 | |
| Hardware Divider | | 1 | |
| CRC-16/32 | | 1 | |
| EXTI | | 16 | |
| 12-bit ADC | | 1 | |
| Number of channels | | 12 Channels | |
| GPIO | | Up to 40 | |
| CPU frequency | | Up to 20 MHz | |
| Operating voltage | | 2.5 V ~ 5.5 V | |
| Operating temperature | | -40 °C ~ 85 °C | |
| Package | | 24/28-pin SSOP, 28-pin SOP, 24/33/46-pin QFN and 44/48-pin LQFP | |

## Block Diagram

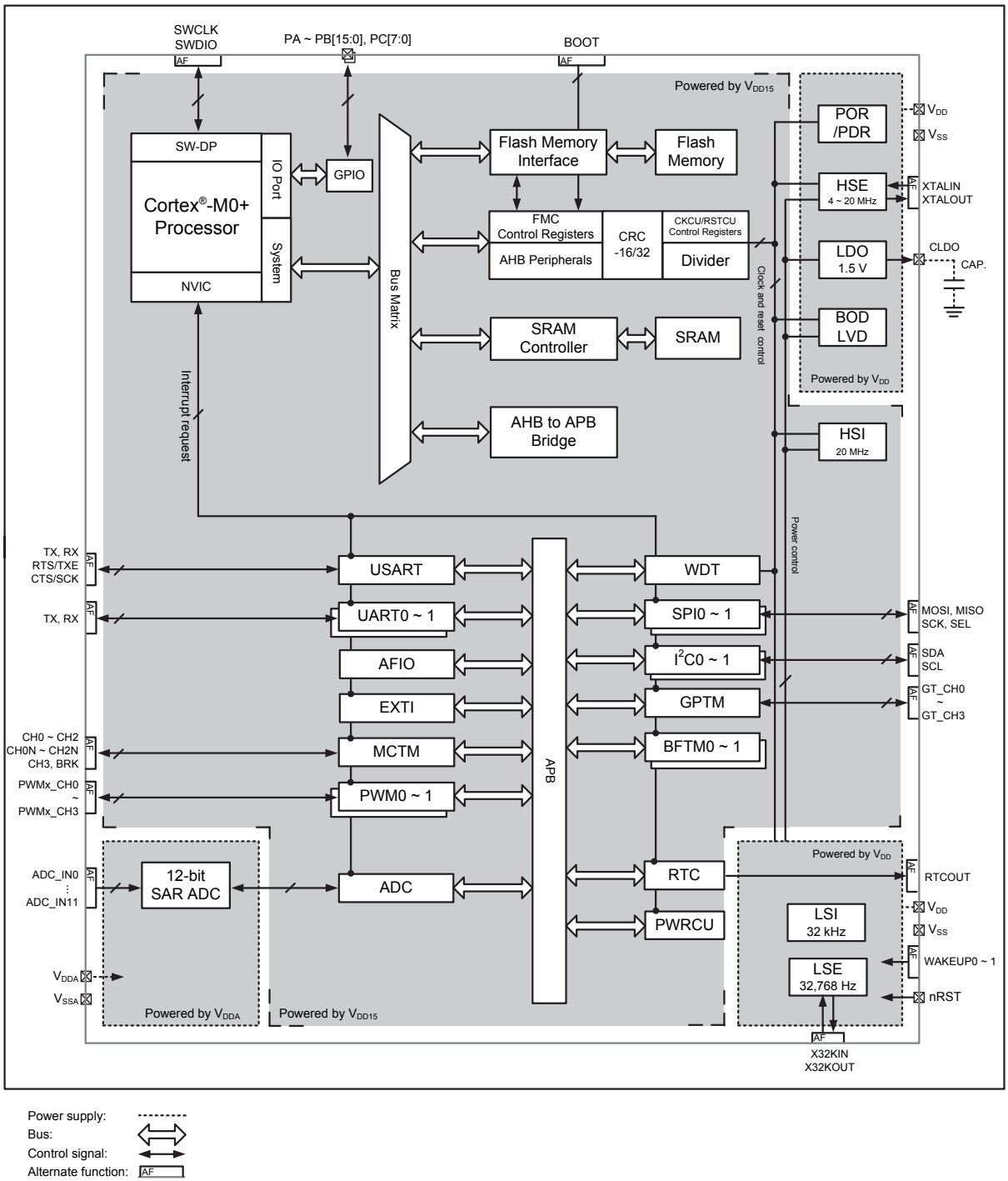



**Figure 1. Block Diagram**

## Memory Map

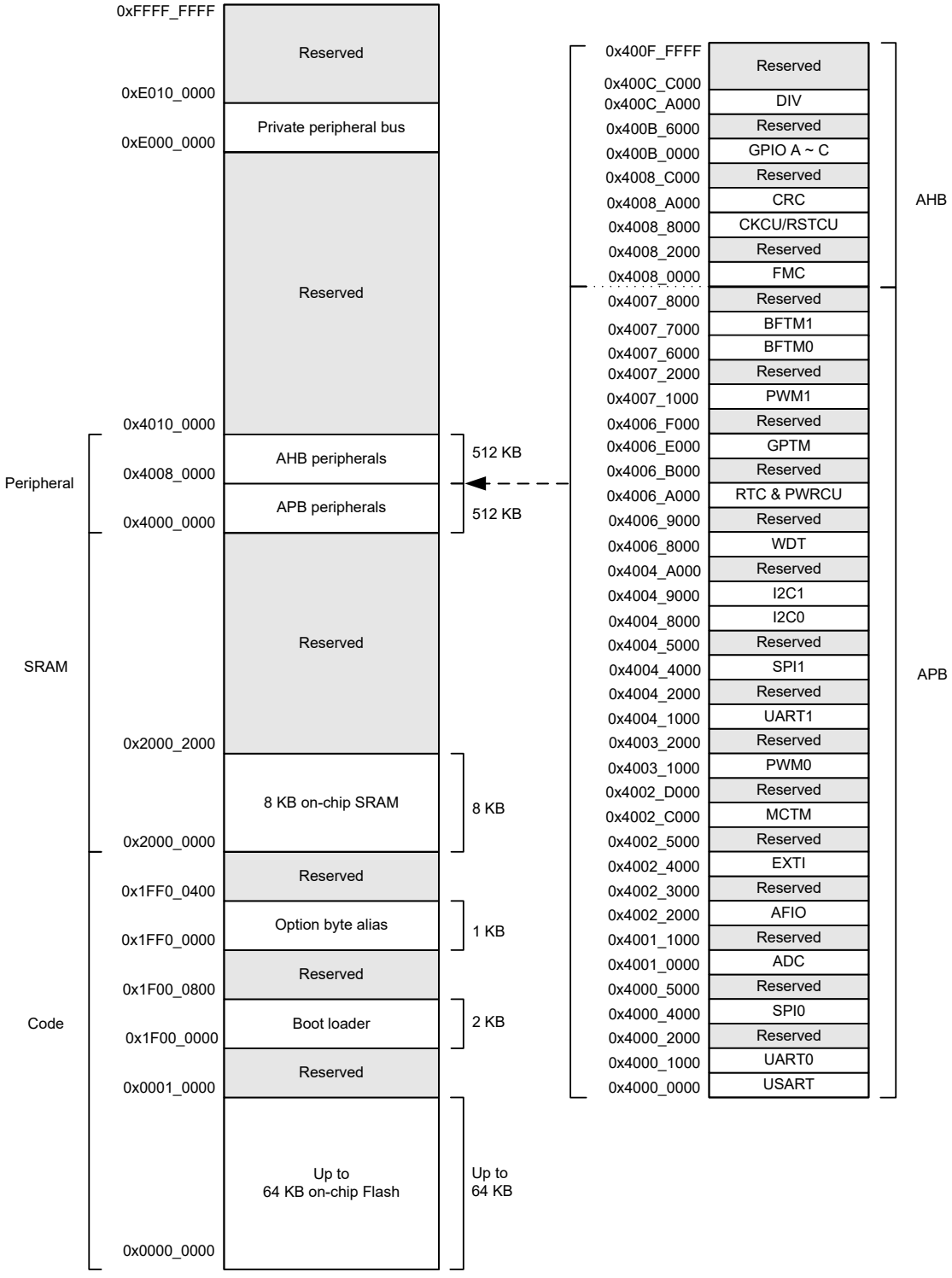



**Figure 2. Memory Map**

**Table 2. Register Map**

| Start Address | End Address | Peripheral | Bus |
|---|---|---|---|
| 0x4000_0000 | 0x4000_0FFF | USART | APB |
| 0x4000_1000 | 0x4000_1FFF | UART0 | |
| 0x4000_2000 | 0x4000_3FFF | Reserved | |
| 0x4000_4000 | 0x4000_4FFF | SPI0 | |
| 0x4000_5000 | 0x4000_FFFF | Reserved | |
| 0x4001_0000 | 0x4001_0FFF | ADC | |
| 0x4001_1000 | 0x4002_1FFF | Reserved | |
| 0x4002_2000 | 0x4002_2FFF | AFIO | |
| 0x4002_3000 | 0x4002_3FFF | Reserved | |
| 0x4002_4000 | 0x4002_4FFF | EXTI | |
| 0x4002_5000 | 0x4002_BFFF | Reserved | |
| 0x4002_C000 | 0x4002_CFFF | MCTM | |
| 0x4002_D000 | 0x4003_0FFF | Reserved | |
| 0x4003_1000 | 0x4003_1FFF | PWM0 | |
| 0x4003_2000 | 0x4004_0FFF | Reserved | |
| 0x4004_1000 | 0x4004_1FFF | UART1 | |
| 0x4004_2000 | 0x4004_3FFF | Reserved | |
| 0x4004_4000 | 0x4004_4FFF | SPI1 | |
| 0x4004_5000 | 0x4004_7FFF | Reserved | |
| 0x4004_8000 | 0x4004_8FFF | I2C0 | |
| 0x4004_9000 | 0x4004_9FFF | I2C1 | |
| 0x4004_A000 | 0x4006_7FFF | Reserved | |
| 0x4006_8000 | 0x4006_8FFF | WDT | |
| 0x4006_9000 | 0x4006_9FFF | Reserved | |
| 0x4006_A000 | 0x4006_AFFF | RTC & PWRCU | |
| 0x4006_B000 | 0x4006_DFFF | Reserved | |
| 0x4006_E000 | 0x4006_EFFF | GPTM | |
| 0x4006_F000 | 0x4007_0FFF | Reserved | |
| 0x4007_1000 | 0x4007_1FFF | PWM1 | |
| 0x4007_2000 | 0x4007_5FFF | Reserved | |
| 0x4007_6000 | 0x4007_6FFF | BFTM0 | |
| 0x4007_7000 | 0x4007_7FFF | BFTM1 | |
| 0x4007_8000 | 0x4007_FFFF | Reserved | |

| Start Address | End Address | Peripheral | Bus |
|---|---|---|---|
| 0x4008_0000 | 0x4008_1FFF | FMC | AHB |
| 0x4008_2000 | 0x4008_7FFF | Reserved | |
| 0x4008_8000 | 0x4008_9FFF | CKCU/RSTCU | |
| 0x4008_A000 | 0x4008_BFFF | CRC | |
| 0x4008_C000 | 0x400A_FFFF | Reserved | |
| 0x400B_0000 | 0x400B_1FFF | GPIOA | |
| 0x400B_2000 | 0x400B_3FFF | GPIOB | |
| 0x400B_4000 | 0x400B_5FFF | GPIOC | |
| 0x400B_6000 | 0x400C_9FFF | Reserved | |
| 0x400C_A000 | 0x400C_BFFF | DIV | |
| 0x400C_C000 | 0x400F_FFFF | Reserved | |

# Clock Structure

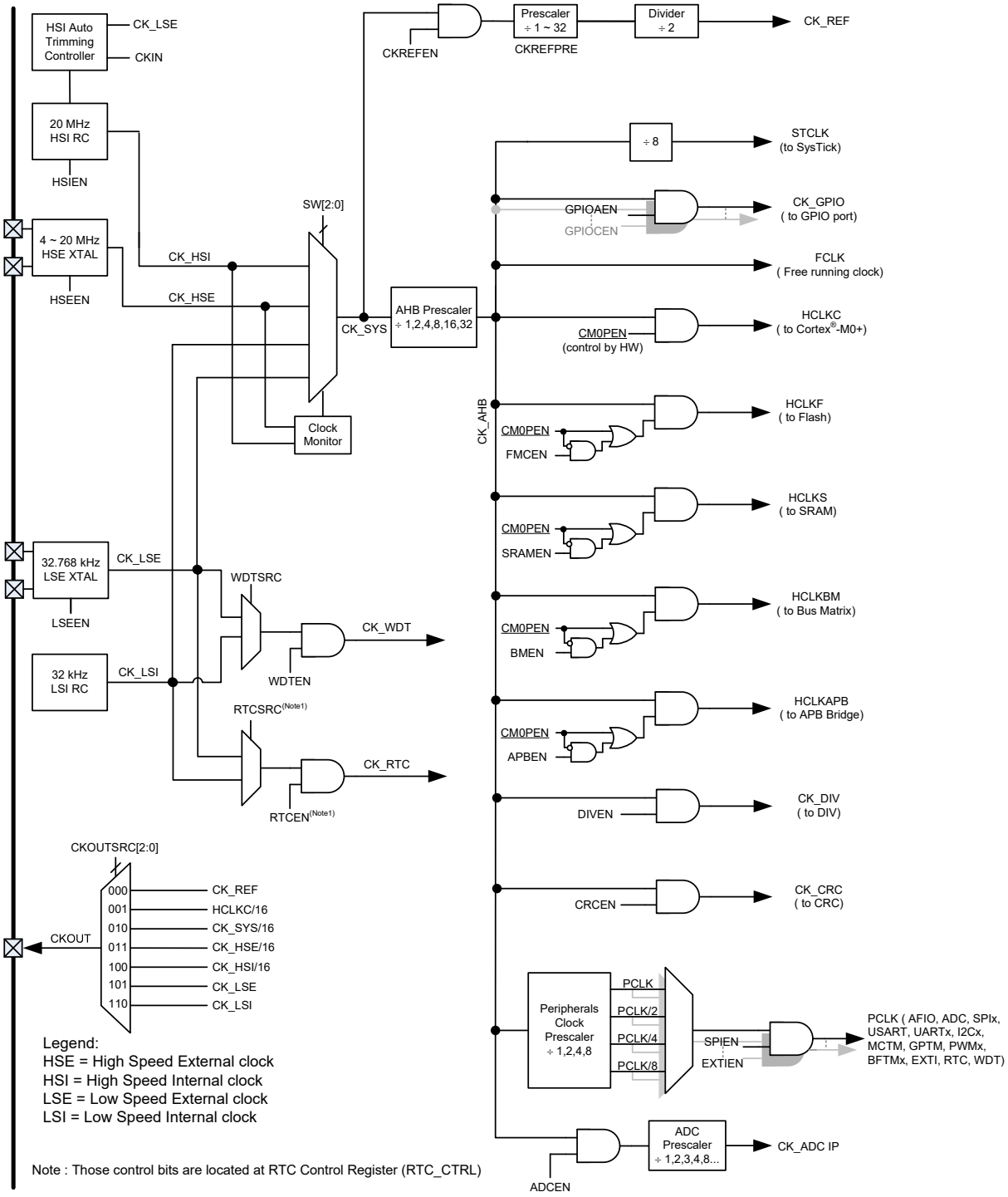



**Figure 3. Clock Structure**

# 4 Pin Assignment

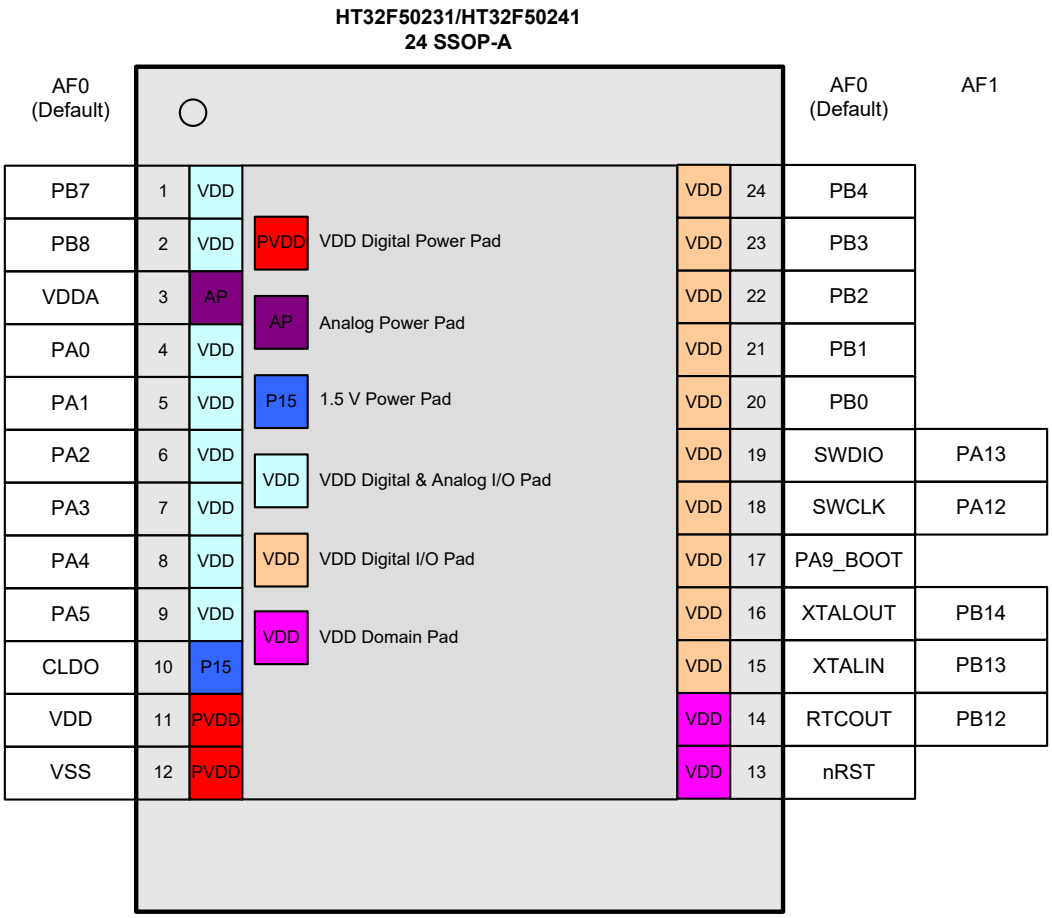



**Figure 4. 24-pin SSOP Pin Assignment**

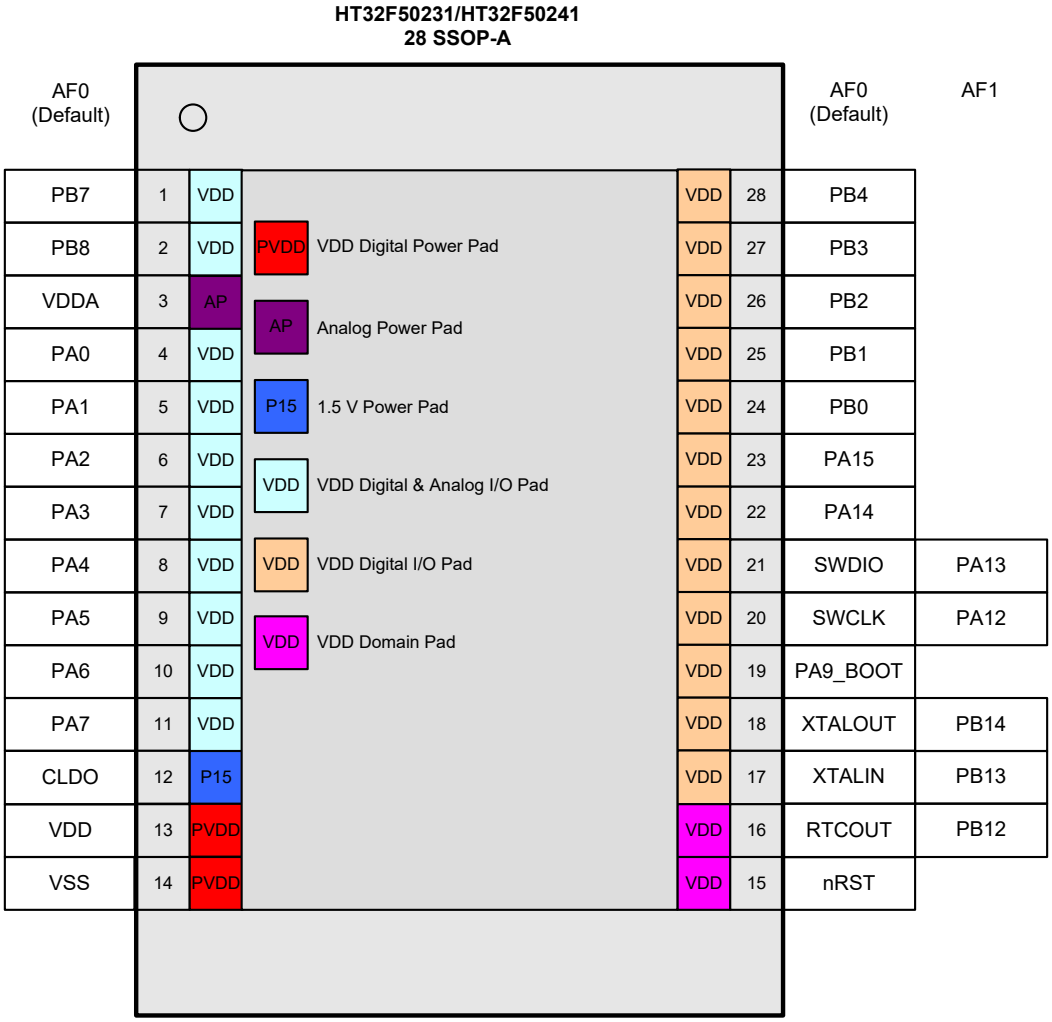



**Figure 5. 28-pin SSOP Pin Assignment**

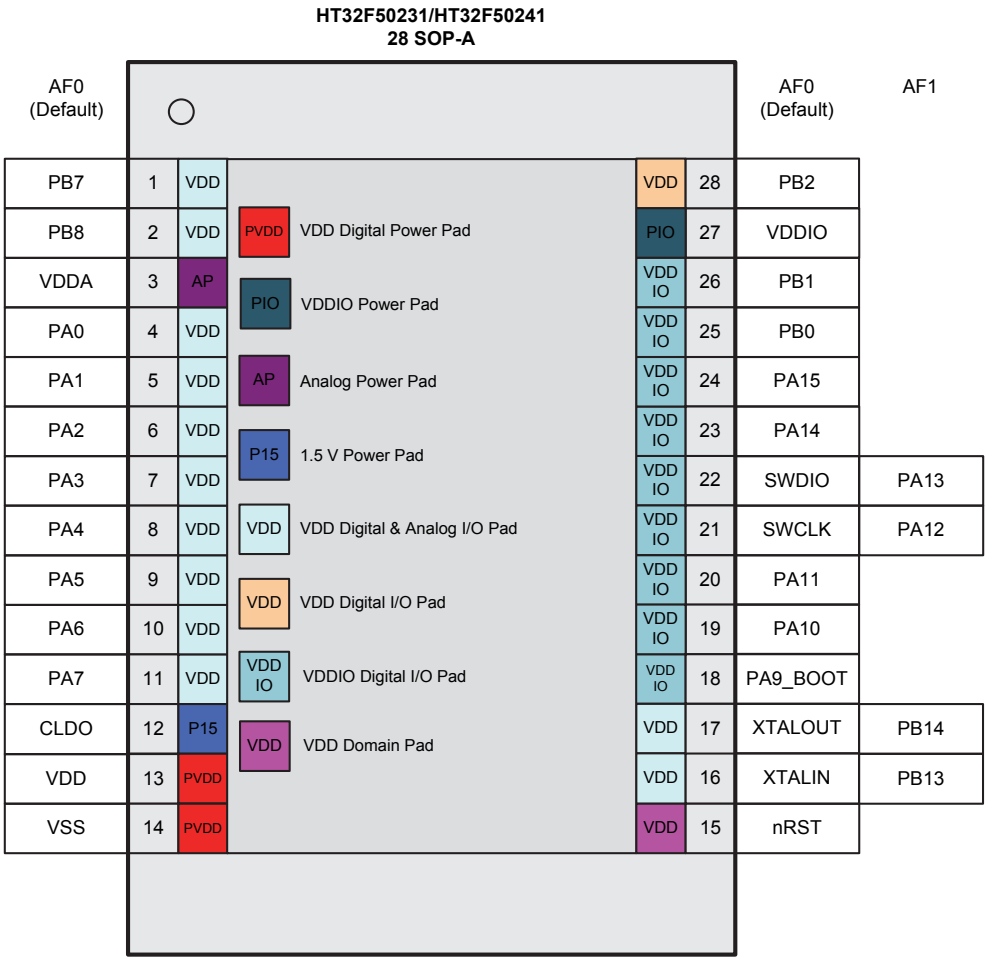



**Figure 6. 28-pin SOP Pin Assignment**

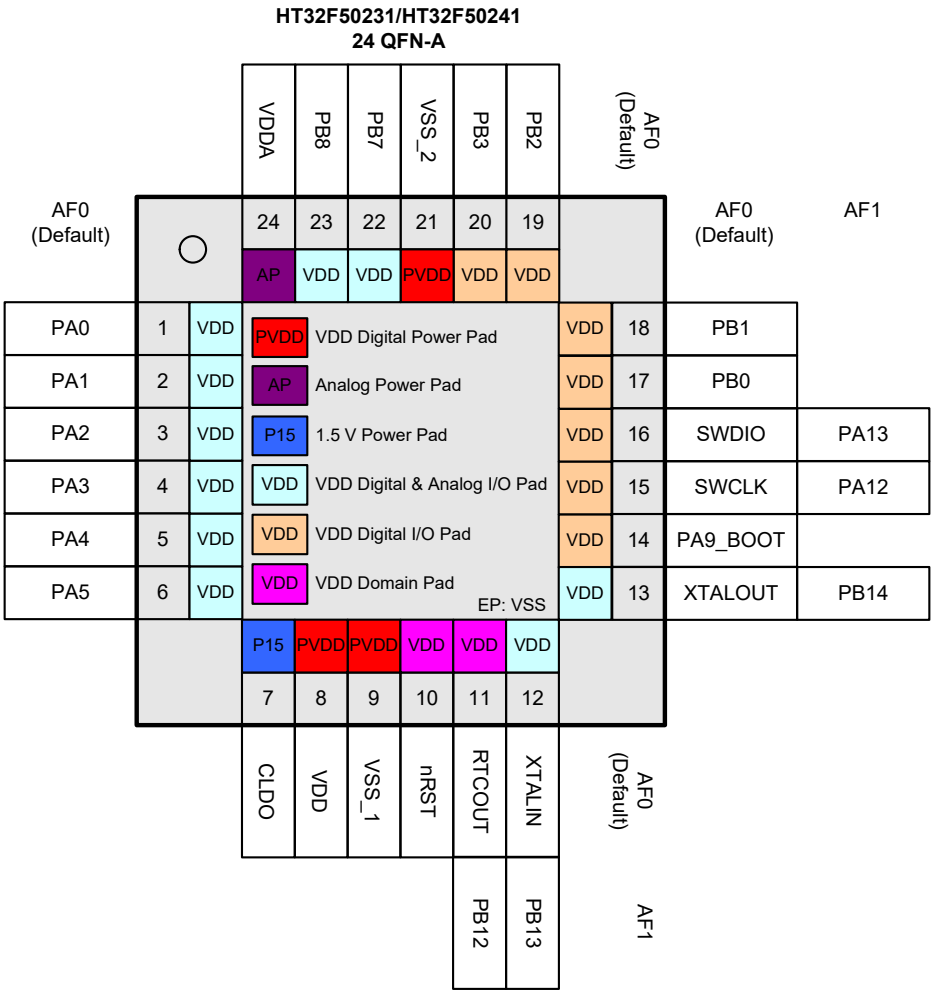



**Figure 7. 24-pin QFN Pin Assignment**

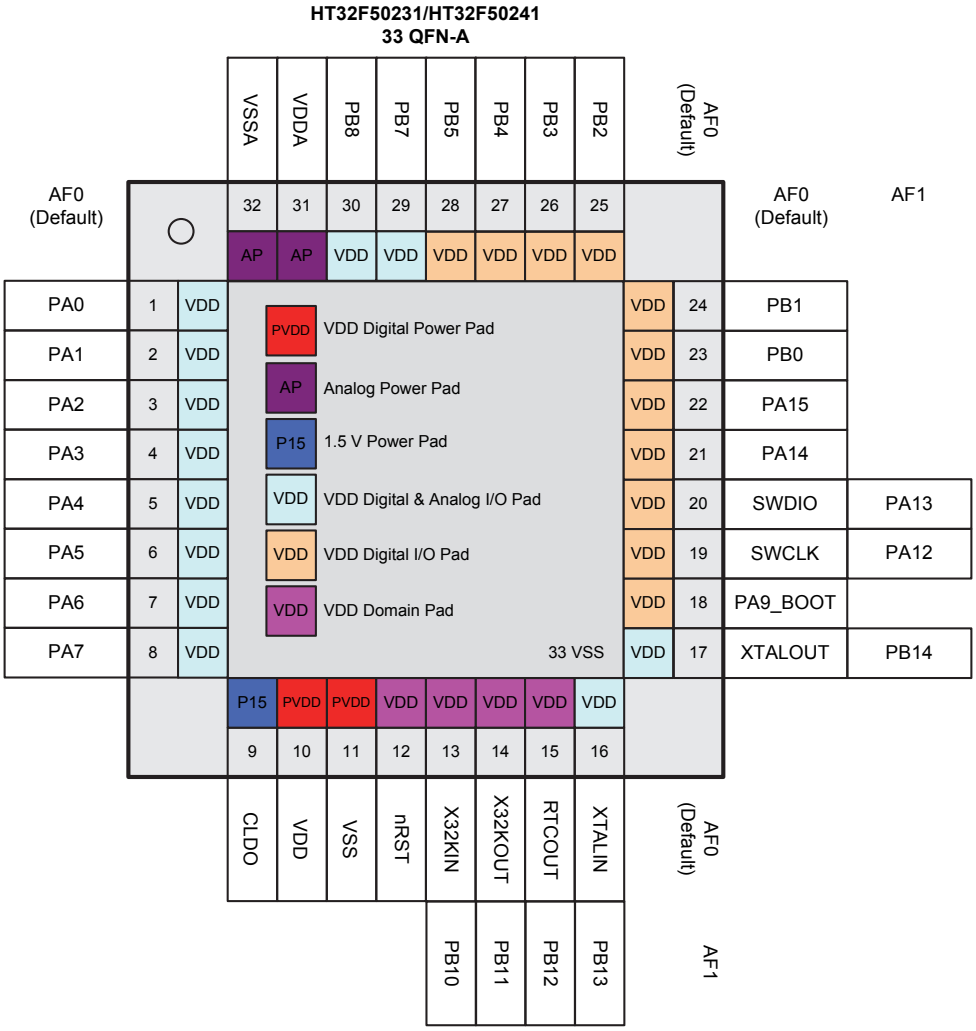



**Figure 8. 33-pin QFN Pin Assignment**

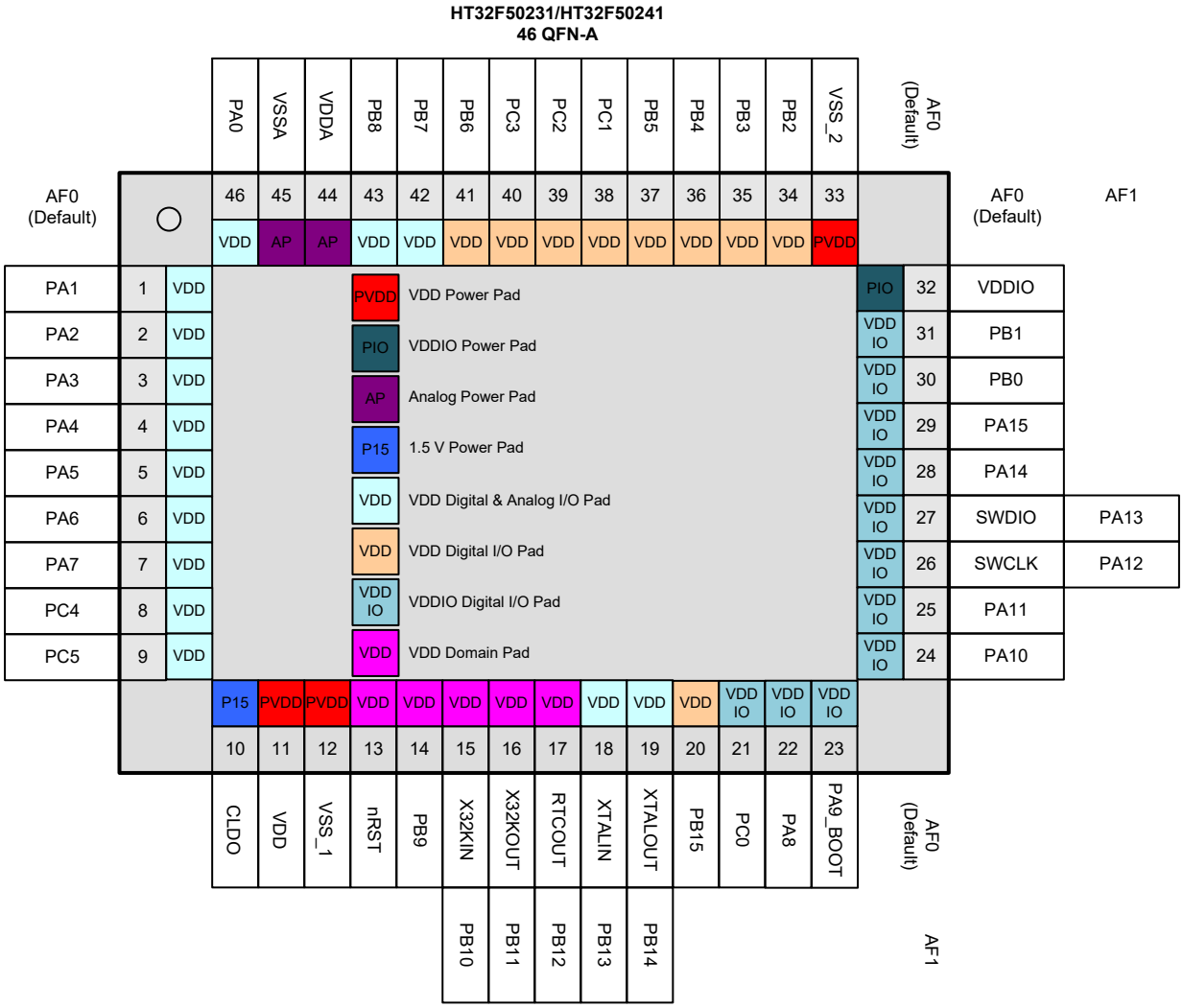



**Figure 9. 46-pin QFN Pin Assignment**

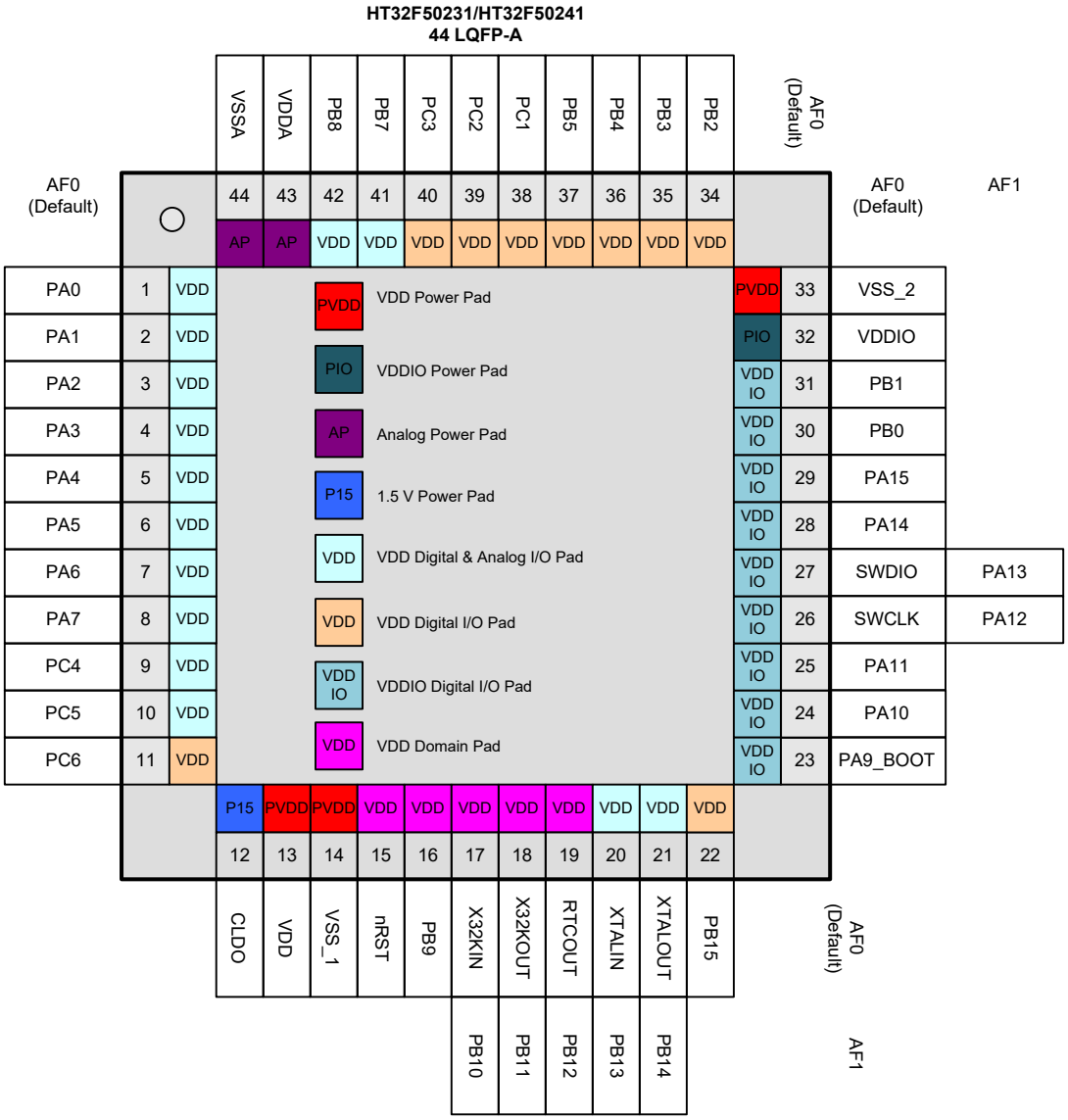



**Figure 10. 44-pin LQFP Pin Assignment**

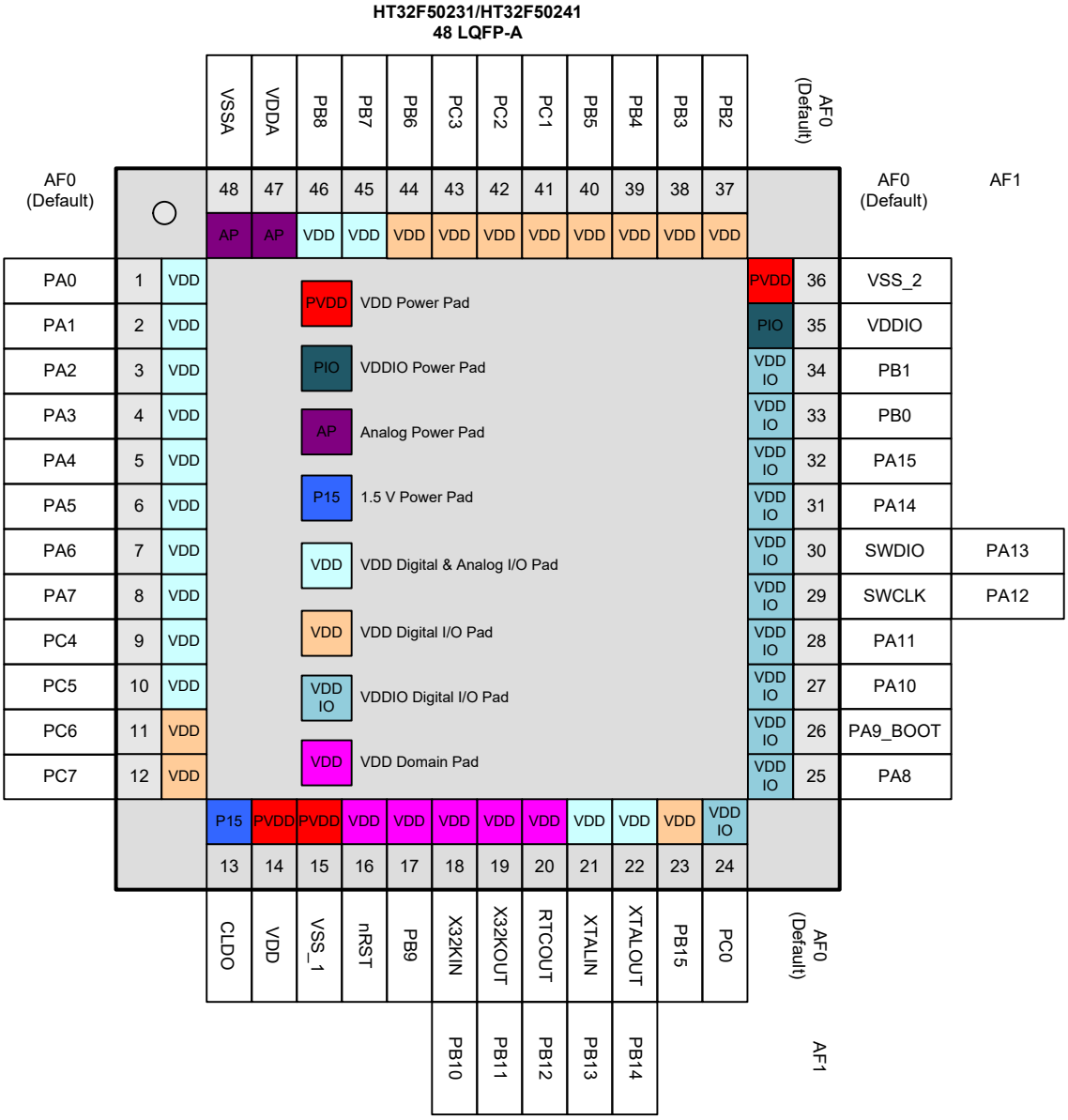



**Figure 11. 48-pin LQFP Pin Assignment**

## Table 3. Pin Assignment

| Packages | | | | | | | | Alternate Function Mapping | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
| 48 LQFP | 46 QFN | 44 LQFP | 33 QFN | 28 SOP | 28 SSOP | 24 SSOP | 24 QFN | System Default | GPIO | ADC | N/A | MCTM /GPTM | SPI | USART /UART | I2C | N/A | N/A | N/A | N/A | N/A | PWM | N/A | System Other |
| 1 | 46 | 1 | 1 | 4 | 4 | 4 | 1 | PA0 | | ADC_IN2 | | GT_CH0 | SPI1_SCK | USR_RTS | I2C1_SCL | | | | | | | | |
| 2 | 1 | 2 | 2 | 5 | 5 | 5 | 2 | PA1 | | ADC_IN3 | | GT_CH1 | SPI1_MOSI | USR_CTS | I2C1_SDA | | | | | | | | |
| 3 | 2 | 3 | 3 | 6 | 6 | 6 | 3 | PA2 | | ADC_IN4 | | GT_CH2 | SPI1_MISO | USR_TX | | | | | | | | | |
| 4 | 3 | 4 | 4 | 7 | 7 | 7 | 4 | PA3 | | ADC_IN5 | | GT_CH3 | SPI1_SEL | USR_RX | | | | | | | | | |
| 5 | 4 | 5 | 5 | 8 | 8 | 8 | 5 | PA4 | | ADC_IN6 | | GT_CH0 | SPI0_SCK | UR1_TX | I2C0_SCL | | | | | | | | |
| 6 | 5 | 6 | 6 | 9 | 9 | 9 | 6 | PA5 | | ADC_IN7 | | GT_CH1 | SPI0_MOSI | UR1_RX | I2C0_SDA | | | | | | | | |
| 7 | 6 | 7 | 7 | 10 | 10 | | | PA6 | | ADC_IN8 | | GT_CH2 | SPI0_MISO | | | | | | | | | | |
| 8 | 7 | 8 | 8 | 11 | 11 | | | PA7 | | ADC_IN9 | | GT_CH3 | SPI0_SEL | | | | | | | | | | |
| 9 | 8 | 9 | | | | | | PC4 | | ADC_IN10 | | | | USR_TX | | | | | | | PWM1_CH0 | | |
| 10 | 9 | 10 | | | | | | PC5 | | ADC_IN11 | | | | USR_RX | | | | | | | PWM1_CH1 | | |
| 11 | | 11 | | | | | | PC6 | | | | MT_CH2 | | UR0_TX | I2C0_SCL | | | | | | | | |
| 12 | | | | | | | | PC7 | | | | MT_CH2N | | UR0_RX | I2C0_SDA | | | | | | | | |
| 13 | 10 | 12 | 9 | 12 | 12 | 10 | 7 | CLDO | | | | | | | | | | | | | | | |
| 14 | 11 | 13 | 10 | 13 | 13 | 11 | 8 | VDD | | | | | | | | | | | | | | | |
| 15 | 12 | 14 | 11 | 14 | 14 | 12 | 9 | VSS_1 | | | | | | | | | | | | | | | |
| 16 | 13 | 15 | 12 | 15 | 15 | 13 | 10 | nRST | | | | | | | | | | | | | | | |
| 17 | 14 | 16 | | | | | | PB9 | | | | MT_CH3 | | | | | | | | | PWM1_CH2 | | WAKEUP1 |
| 18 | 15 | 17 | 13 | | | | | X32KIN | PB10 | | | GT_CH0 | SPI1_SEL | USR_TX | | | | | | | PWM1_CH3 | | |
| 19 | 16 | 18 | 14 | | | | | X32KOUT | PB11 | | | GT_CH1 | SPI1_SCK | USR_RX | | | | | | | PWM0_CH3 | | |
| 20 | 17 | 19 | 15 | | 16 | 14 | 11 | RTCOUT | PB12 | | | | SPI0_MISO | UR0_RX | | | | | | | PWM0_CH0 | | WAKEUP0 |
| 21 | 18 | 20 | 16 | 16 | 17 | 15 | 12 | XTALIN | PB13 | | | | | UR0_TX | I2C0_SCL | | | | | | | | |
| 22 | 19 | 21 | 17 | 17 | 18 | 16 | 13 | XTALOUT | PB14 | | | | | UR0_RX | I2C0_SDA | | | | | | | | |
| 23 | 20 | 22 | | | | | | PB15 | | | | MT_CH0 | SPI0_SEL | | I2C1_SCL | | | | | | PWM0_CH1 | | |
| 24 | 21 | | | | | | | PC0 | | | | MT_CH0N | SPI0_SCK | | I2C1_SDA | | | | | | PWM0_CH2 | | |
| 25 | 22 | | | | | | | PA8 | | | | | | USR_TX | | | | | | | PWM1_CH3 | | |
| 26 | 23 | 23 | 18 | 18 | 19 | 17 | 14 | PA9_BOOT | | | | | SPI0_MOSI | | | | | | | | PWM1_CH0 | | CKOUT |
| 27 | 24 | 24 | | 19 | | | | PA10 | | | | MT_CH1 | SPI0_MOSI | USR_RX | | | | | | | PWM0_CH1 | | |
| 28 | 25 | 25 | | 20 | | | | PA11 | | | | MT_CH1N | SPI0_MISO | | | | | | | | PWM0_CH2 | | |
| 29 | 26 | 26 | 19 | 21 | 20 | 18 | 15 | SWCLK | PA12 | | | | | | | | | | | | | | |
| 30 | 27 | 27 | 20 | 22 | 21 | 19 | 16 | SWDIO | PA13 | | | | | | | | | | | | | | |
| 31 | 28 | 28 | 21 | 23 | 22 | | | PA14 | | | | MT_CH0 | SPI1_SEL | UR1_TX | I2C1_SCL | | | | | | PWM0_CH0 | | |
| 32 | 29 | 29 | 22 | 24 | 23 | | | PA15 | | | | MT_CH0N | SPI1_SCK | UR1_RX | I2C1_SDA | | | | | | PWM1_CH2 | | |
| 33 | 30 | 30 | 23 | 25 | 24 | 20 | 17 | PB0 | | | | MT_CH1 | SPI1_MOSI | USR_TX | I2C0_SCL | | | | | | PWM0_CH1 | | |
| 34 | 31 | 31 | 24 | 26 | 25 | 21 | 18 | PB1 | | | | MT_CH1N | SPI1_MISO | USR_RX | I2C0_SDA | | | | | | PWM1_CH1 | | |
| 35 | 32 | 32 | | 27 | | | | VDDIO | | | | | | | | | | | | | | | |
| 36 | 33 | 33 | 33 | | | | 21 | VSS_2 | | | | | | | | | | | | | | | |

| Packages | | | | | | | | Alternate Function Mapping | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
| 48 LQFP | 46 QFN | 44 LQFP | 33 QFN | 28 SOP | 28 SSOP | 24 SSOP | 24 QFN | System Default | GPIO | ADC | N/A | MCTM /GPTM | SPI | USART /UART | I2C | N/A | N/A | N/A | N/A | N/A | PWM | N/A | System Other |
| 37 | 34 | 34 | 25 | 28 | 26 | 22 | 19 | PB2 | | | | MT_ CH2 | SPI0_ SEL | UR1_ TX | | | | | | | PWM0_ CH2 | | CKIN |
| 38 | 35 | 35 | 26 | | 27 | 23 | 20 | PB3 | | | | MT_ CH2N | SPI0_ SCK | UR1_ RX | | | | | | | PWM1_ CH2 | | |
| 39 | 36 | 36 | 27 | | 28 | 24 | | PB4 | | | | MT_ BRK | SPI0_ MOSI | UR1_ TX | | | | | | | PWM0_ CH3 | | |
| 40 | 37 | 37 | 28 | | | | | PB5 | | | | GT_ CH2 | SPI0_ MISO | UR1_ RX | | | | | | | | | |
| 41 | 38 | 38 | | | | | | PC1 | | | | MT_ CH0 | SPI1_ SEL | UR1_ TX | | | | | | | PWM0_ CH0 | | |
| 42 | 39 | 39 | | | | | | PC2 | | | | MT_ CH0N | SPI1_ SCK | | | | | | | | PWM1_ CH0 | | |
| 43 | 40 | 40 | | | | | | PC3 | | | | MT_ BRK | SPI1_ MOSI | UR1_ RX | | | | | | | PWM1_ CH1 | | |
| 44 | 41 | | | | | | | PB6 | | | | GT_ CH3 | SPI1_ MISO | UR0_ TX | | | | | | | | | |
| 45 | 42 | 41 | 29 | 1 | 1 | 1 | 22 | PB7 | | ADC_ IN0 | | MT_ CH1 | SPI0_ MISO | UR0_ TX | I2C1_ SCL | | | | | | PWM0_ CH3 | | |
| 46 | 43 | 42 | 30 | 2 | 2 | 2 | 23 | PB8 | | ADC_ IN1 | | MT_ CH1N | SPI0_ SEL | UR0_ RX | I2C1_ SDA | | | | | | PWM1_ CH3 | | |
| 47 | 44 | 43 | 31 | 3 | 3 | 3 | 24 | VDDA | | | | | | | | | | | | | | | |
| 48 | 45 | 44 | 32 | | | | | VSSA | | | | | | | | | | | | | | | |

Note: 1. For the 24QFN package, the EP VSS is internally connected to the pin number 21 and 9. The EP means the Exposed Pad of the QFN packages.

2. The pin number 33 of the 33QFN package is located at the exposed pad of the QFN package.

## Table 4. Pin Description

| Pin number | | | | | | | | Pin Name | Type(1) | I/O Structure(2) | Output Driving | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 48 LQFP | 46 QFN | 44 LQFP | 33 QFN | 28 SOP | 28 SSOP | 24 SSOP | 24 QFN | | | | | Default function (AF0) |
| 1 | 46 | 1 | 1 | 4 | 4 | 4 | 1 | PA0 | AI/O | 5V | 4/8/12/16 mA | PA0 |
| 2 | 1 | 2 | 2 | 5 | 5 | 5 | 2 | PA1 | AI/O | 5V | 4/8/12/16 mA | PA1 |
| 3 | 2 | 3 | 3 | 6 | 6 | 6 | 3 | PA2 | AI/O | 5V | 4/8/12/16 mA | PA2 |
| 4 | 3 | 4 | 4 | 7 | 7 | 7 | 4 | PA3 | AI/O | 5V | 4/8/12/16 mA | PA3 |
| 5 | 4 | 5 | 5 | 8 | 8 | 8 | 5 | PA4 | AI/O | 5V | 4/8/12/16 mA | PA4 |
| 6 | 5 | 6 | 6 | 9 | 9 | 9 | 6 | PA5 | AI/O | 5V | 4/8/12/16 mA | PA5 |
| 7 | 6 | 7 | 7 | 10 | 10 | | | PA6 | AI/O | 5V | 4/8/12/16 mA | PA6 |
| 8 | 7 | 8 | 8 | 11 | 11 | | | PA7 | AI/O | 5V | 4/8/12/16 mA | PA7 |
| 9 | 8 | 9 | | | | | | PC4 | AI/O | 5V | 4/8/12/16 mA | PC4 |
| 10 | 9 | 10 | | | | | | PC5 | AI/O | 5V | 4/8/12/16 mA | PC5 |
| 11 | | 11 | | | | | | PC6 | I/O | 5V | 4/8/12/16 mA | PC6 |
| 12 | | | | | | | | PC7 | I/O | 5V | 4/8/12/16 mA | PC7 |
| 13 | 10 | 12 | 9 | 12 | 12 | 10 | 7 | CLDO | P | — | — | Core power LDO 1.5 V output It must be connected a 2.2 μF capacitor as close as possible between this pin and VSS_1. |
| 14 | 11 | 13 | 10 | 13 | 13 | 11 | 8 | VDD | P | — | — | Voltage for digital I/O |
| 15 | 12 | 14 | 11 | 14 | 14 | 12 | 9 | VSS_1 | P | — | — | Ground reference for digital I/O |
| 16 | 13 | 15 | 12 | 15 | 15 | 13 | 10 | nRST(3) | I | 5V_PU | — | External reset pin |
| 17 | 14 | 16 | | | | | | PB9(3) | I/O (VDD) | 5V | 4/8/12/16 mA | PB9 |
| 18 | 15 | 17 | 13 | | | | | PB10(3) | AI/O (VDD) | 5V | 4/8/12/16 mA | X32KIN |
| 19 | 16 | 18 | 14 | | | | | PB11(3) | AI/O (VDD) | 5V | 4/8/12/16 mA | X32KOUT |

| Pin number | | | | | | | | Pin Name | Type(1) | I/O Structure(2) | Output Driving | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 48 LQFP | 46 QFN | 44 LQFP | 33 QFN | 28 SOP | 28 SSOP | 24 SSOP | 24 QFN | | | | | Default function (AF0) |
| 20 | 17 | 19 | 15 | | 16 | 14 | 11 | PB12(3) | I/O (VDD) | 5V | 4/8/12/16 mA | RTCOUT |
| 21 | 18 | 20 | 16 | 16 | 17 | 15 | 12 | PB13 | AI/O | 5V | 4/8/12/16 mA | XTALIN |
| 22 | 19 | 21 | 17 | 17 | 18 | 16 | 13 | PB14 | AI/O | 5V | 4/8/12/16 mA | XTALOUT |
| 23 | 20 | 22 | | | | | | PB15 | I/O | 5V | 4/8/12/16 mA | PB15 |
| 24 | 21 | | | | | | | PC0 | I/O (VDDIO) | 5V | 4/8/12/16 mA | PC0 |
| 25 | 22 | | | | | | | PA8 | I/O (VDDIO) | 5V | 4/8/12/16 mA | PA8 |
| 26 | 23 | 23 | 18 | 18 | 19 | 17 | 14 | PA9 | I/O (VDDIO) | 5V_PU | 4/8/12/16 mA | PA9_BOOT |
| 27 | 24 | 24 | | 19 | | | | PA10 | I/O (VDDIO) | 5V | 4/8/12/16 mA | PA10 |
| 28 | 25 | 25 | | 20 | | | | PA11 | I/O (VDDIO) | 5V | 4/8/12/16 mA | PA11 |
| 29 | 26 | 26 | 19 | 21 | 20 | 18 | 15 | PA12 | I/O (VDDIO) | 5V_PU | 4/8/12/16 mA | SWCLK |
| 30 | 27 | 27 | 20 | 22 | 21 | 19 | 16 | PA13 | I/O (VDDIO) | 5V_PU | 4/8/12/16 mA | SWDIO |
| 31 | 28 | 28 | 21 | 23 | 22 | | | PA14 | I/O (VDDIO) | 5V | 4/8/12/16 mA | PA14 |
| 32 | 29 | 29 | 22 | 24 | 23 | | | PA15 | I/O (VDDIO) | 5V | 4/8/12/16 mA | PA15 |
| 33 | 30 | 30 | 23 | 25 | 24 | 20 | 17 | PB0 | I/O (VDDIO) | 5V | 4/8/12/16 mA | PB0 |
| 34 | 31 | 31 | 24 | 26 | 25 | 21 | 18 | PB1 | I/O (VDDIO) | 5V | 4/8/12/16 mA | PB1 |
| 35 | 32 | 32 | | 27 | | | | VDDIO | P | — | — | Voltage for digital I/O |
| 36 | 33 | 33 | 33 | | | | 21 | VSS_2 | P | — | — | Ground reference for digital I/O |
| 37 | 34 | 34 | 25 | 28 | 26 | 22 | 19 | PB2 | I/O | 5V | 4/8/12/16 mA | PB2 |
| 38 | 35 | 35 | 26 | | 27 | 23 | 20 | PB3 | I/O | 5V | 4/8/12/16 mA | PB3 |
| 39 | 36 | 36 | 27 | | 28 | 24 | | PB4 | I/O | 5V | 4/8/12/16 mA | PB4 |
| 40 | 37 | 37 | 28 | | | | | PB5 | I/O | 5V | 4/8/12/16 mA | PB5 |
| 41 | 38 | 38 | | | | | | PC1 | I/O | 5V | 4/8/12/16 mA | PC1 |
| 42 | 39 | 39 | | | | | | PC2 | I/O | 5V | 4/8/12/16 mA | PC2 |
| 43 | 40 | 40 | | | | | | PC3 | I/O | 5V | 4/8/12/16 mA | PC3 |
| 44 | 41 | | | | | | | PB6 | I/O | 5V | 4/8/12/16 mA | PB6 |
| 45 | 42 | 41 | 29 | 1 | 1 | 1 | 22 | PB7 | AI/O | 5V | 4/8/12/16 mA | PB7 |
| 46 | 43 | 42 | 30 | 2 | 2 | 2 | 23 | PB8 | AI/O | 5V | 4/8/12/16 mA | PB8 |
| 47 | 44 | 43 | 31 | 3 | 3 | 3 | 24 | VDDA | P | — | — | Analog voltage for ADC |
| 48 | 45 | 44 | 32 | | | | | VSSA | P | — | — | Ground reference for the ADC |

Note: 1. I = input, O = output, A = Analog port, P = power supply, $V_{DD}$ = $V_{DD}$ Power.
2. 5V = 5 V operation I/O type, PU = Pull-up.
3. These pins are located at the $V_{DD}$ power domain.

# 5 Electrical Characteristics



## Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**Table 5. Absolute Maximum Ratings**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | External Main Supply Voltage | $V_{SS}$ - 0.3 | $V_{SS}$ + 5.5 | V |
| $V_{DDIO}$ | External I/O Supply Voltage | $V_{SS}$ - 0.3 | $V_{SS}$ + 5.5 | V |
| $V_{DDA}$ | External Analog Supply Voltage | $V_{SSA}$ - 0.3 | $V_{SSA}$ + 5.5 | V |
| $V_{IN}$ | Input Voltage on I/O | $V_{SS}$ - 0.3 | $V_{DD}$ + 0.3 | V |
| $T_A$ | Ambient Operating Temperature Range | -40 | +85 | °C |
| $T_{STG}$ | Storage Temperature Range | -55 | +150 | °C |
| $T_J$ | Maximum Junction Temperature | — | 125 | °C |
| $P_D$ | Total Power Dissipation | — | 500 | mW |
| $V_{ESD}$ | Electrostatic Discharge Voltage – Human Body Mode | -4000 | +4000 | V |

## Recommended DC Operating Conditions

**Table 6. Recommended DC Operating Conditions**

$T_A$ = 25 °C, unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operating Voltage | — | 2.5 | 5.0 | 5.5 | V |
| $V_{DDIO}$ | I/O Operating Voltage | — | 1.8 | 5.0 | 5.5 | V |
| $V_{DDA}$ | Analog Operating Voltage | — | 2.5 | 5.0 | 5.5 | V |

## On-Chip LDO Voltage Regulator Characteristics

**Table 7. LDO Characteristics**

$T_A$ = 25 °C, unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{LDO}$ | Internal Regulator Output Voltage | $V_{DD}$ ≥ 2.5 V Regulator input @ $I_{LDO}$ = 35 mA and voltage variant = ±5 %, After trimming | 1.425 | 1.5 | 1.57 | V |
| $I_{LDO}$ | Output Current | $V_{DD}$ = 2.5 V Regulator input @ $V_{LDO}$ = 1.5 V | — | 30 | 35 | mA |
| $C_{LDO}$ | External Filter Capacitor Value for Internal Core Power Supply | The capacitor value is dependent on the core power current consumption | 1 | 2.2 | — | μF |

## Power Consumption

### Table 8. Power Consumption Characteristics

| Symbol | Parameter | Conditions | Typ | Max | | Unit |
|---|---|---|---|---|---|---|
| | | | $T_A$ = 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | |
| $I_{DD}$ | Supply Current (Run Mode) | $V_{DD}$ = 5.0 V, HSI = 20 MHz, $f_{CPU}$ = 20 MHz, $f_{BUS}$ = 20 MHz, all peripherals enabled | 6.5 | 7.2 | — | mA |
| | | $V_{DD}$ = 5.0 V, HSI = 20 MHz, $f_{CPU}$ = 20 MHz, $f_{BUS}$ = 20 MHz, all peripherals disabled | 4 | 4.5 | — | |
| | | $V_{DD}$ = 5.0 V, HSI = 20 MHz, $f_{CPU}$ = 10 MHz, $f_{BUS}$ = 10 MHz, all peripherals enabled | 3.5 | 3.9 | — | |
| | | $V_{DD}$ = 5.0 V, HSI = 20 MHz, $f_{CPU}$ = 10 MHz, $f_{BUS}$ = 10 MHz, all peripherals disabled | 2.25 | 2.5 | — | |
| | | $V_{DD}$ = 5.0 V, HSI off, LSI on, $f_{CPU}$ = 32 kHz, $f_{BUS}$ = 32 kHz, all peripherals enabled | 32 | 41 | — | µA |
| | | $V_{DD}$ = 5.0 V, HSI off, LSI on, $f_{CPU}$ = 32 kHz, $f_{BUS}$ = 32 kHz, all peripherals disabled | 28 | 37 | — | |
| | Supply Current (Sleep Mode) | $V_{DD}$ = 5.0 V, HSI = 20 MHz, $f_{CPU}$ = 0 MHz, $f_{BUS}$ = 20 MHz, all peripherals enabled | 3.5 | 3.9 | — | mA |
| | | $V_{DD}$ = 5.0 V, HSI = 20 MHz, $f_{CPU}$ = 0 MHz, $f_{BUS}$ = 20 MHz, all peripherals disabled | 0.8 | 0.92 | — | |
| | | $V_{DD}$ = 5.0 V, HSI = 20 MHz, $f_{CPU}$ = 0 MHz, $f_{BUS}$ = 10 MHz, all peripherals enabled | 2 | 2.25 | — | |
| | | $V_{DD}$ = 5.0 V, HSI = 20 MHz, $f_{CPU}$ = 0 MHz, $f_{BUS}$ = 10 MHz, all peripherals disabled | 0.65 | 0.75 | — | |
| | Supply Current (Deep-Sleep1 Mode) | $V_{DD}$ = 5.0 V, All clock off (HSE/HSI/LSE), LDO in low power mode, LSI on, RTC on | 23 | 29 | — | µA |
| | Supply Current (Deep-Sleep2 Mode) | $V_{DD}$ = 5.0 V, All clock off (HSE/HSI/LSE), LDO off, DMOS on, LSI on, RTC on | 6.5 | 10 | — | |

Note: 1. HSE means high speed external oscillator. HSI means 20 MHz high speed internal oscillator.
2. LSE means 32.768 kHz low speed external oscillator. LSI means 32 kHz low speed internal oscillator.
3. RTC means real time clock.
4. Code = while (1) {208 NOP} executed in Flash.
5. $f_{BUS}$ means $f_{HCLK}$ and $f_{PCLK}$.

# Reset and Supply Monitor Characteristics

### Table 9. $V_{DD}$ Power Reset Characteristics

$T_A$ = 25 °C, unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{POR}$ | Power On Reset Threshold (Rising Voltage on $V_{DD}$) | $T_A$ = -40 °C~ 85 °C | 2.22 | 2.35 | 2.48 | V |
| $V_{PDR}$ | Power Down Reset Threshold (Falling Voltage on $V_{DD}$) | | 2.12 | 2.2 | 2.33 | V |
| $V_{PORHYST}$ | POR Hysteresis | — | — | 150 | — | mV |
| $t_{POR}$ | Reset Delay Time | $V_{DD}$ = 5.0 V | — | 0.1 | 0.2 | ms |

Note: 1. Data based on characterization results only, not tested in production.
2. Guaranteed by design, not tested in production.
3. If the LDO is turned on, the $V_{DD}$ POR has to be in the de-assertion condition. When the $V_{DD}$ POR is in the assertion state then the LDO will be turned off.

### Table 10. LVD/BOD Characteristics

$T_A$ = 25 °C, unless otherwise specified.

| Symbol | Parameter | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{BOD}$ | Voltage of Brown Out Detection | $T_A$ = -40 °C~ 85 °C<br>After factory-trimmed,<br>$V_{DD}$ Falling edge | | 2.37 | 2.45 | 2.53 | V |
| $V_{LVD}$ | Voltage of Low Voltage Detection | $T_A$ = -40 °C~ 85 °C,<br>$V_{DD}$ Falling edge | LVDS = 000 | 2.57 | 2.65 | 2.73 | V |
| | | | LVDS = 001 | 2.77 | 2.85 | 2.93 | V |
| | | | LVDS = 010 | 2.97 | 3.05 | 3.13 | V |
| | | | LVDS = 011 | 3.17 | 3.25 | 3.33 | V |
| | | | LVDS = 100 | 3.37 | 3.45 | 3,53 | V |
| | | | LVDS = 101 | 4.15 | 4.25 | 4.35 | V |
| | | | LVDS = 110 | 4.35 | 4.45 | 4.55 | V |
| | | | LVDS = 111 | 4.55 | 4.65 | 4.75 | V |
| $V_{LVDHTST}$ | LVD Hysteresis | $V_{DD}$ = 5.0 V | — | — | 100 | — | mV |
| $t_{suLVD}$ | LVD Setup Time | $V_{DD}$ = 5.0 V | — | — | — | 5 | μs |
| $t_{atLVD}$ | LVD Active Delay Time | $V_{DD}$ = 5.0 V | — | — | — | — | ms |
| $I_{DDLVD}$ | Operation Current (3) | $V_{DD}$ = 5.0 V | — | — | 10 | 20 | μA |

Note: 1. Data based on characterization results only, not tested in production.
2. Guaranteed by design, not tested in production.
3. Bandgap current is not included.
4. LVDS field is in the PWRCU LVDCSR register.

## External Clock Characteristics

### Table 11. High Speed External Clock (HSE) Characteristics

$T_A$ = 25 °C, unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operation Range | $T_A$ = -40 °C ~ 85 °C | 2.5 | — | 5.5 | V |
| $f_{HSE}$ | High Speed External Oscillator Frequency (HSE) | $V_{DD}$ = 2.5 V ~ 5.0 V | 4 | — | 20 | MHz |
| $C_{LHSE}$ | Load Capacitance | $V_{DD}$ = 5.0 V, $R_{ESR}$ = 100 Ω @ 20 MHz | — | — | 12 | pF |
| $R_{FHSE}$ | Internal Feedback Resistor between XTALIN and XTALOUT pins | $V_{DD}$ = 5.0 V | — | 0.5 | — | MΩ |
| $R_{ESR}$ | Equivalent Series Resistance | $V_{DD}$ = 5.0 V, $C_L$ = 12 pF @ 20 MHz, HSEDR = 0 | — | — | 110 | Ω |
| | | $V_{DD}$ = 2.5 V, $C_L$ = 12 pF @ 20 MHz, HSEDR = 1 | | | | |
| $D_{HSE}$ | HSE Oscillator Duty Cycle | — | 40 | — | 60 | % |
| $I_{DDHSE}$ | HSE Oscillator Current Consumption | $V_{DD}$ = 5.0 V, $R_{ESR}$ = 100 Ω, $C_L$ = 12 pF @ 8 MHz, HSEDR = 0 | — | 0.85 | — | mA |
| | | $V_{DD}$ = 5.0 V, $R_{ESR}$ = 25 Ω, $C_L$ = 12 pF @ 20 MHz, HSEDR = 1 | — | 3.0 | — | |
| $I_{PWDHSE}$ | HSE Oscillator Power Down Current | $V_{DD}$ = 5.0 V | — | — | 0.01 | μA |
| $t_{SUHSE}$ | HSE Oscillator Startup Time | $V_{DD}$ = 5.0 V | — | — | 4 | ms |

Note: The following guidelines are recommended to increase the stability of the crystal circuit of the HSE clock in the PCB layout:

1. The crystal oscillator should be located as close as possible to the MCU to keep the trace lengths as short as possible to reduce any parasitic capacitance.
2. Shield lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
3. Keep any high frequency signal lines away from the crystal area to prevent any crosstalk adverse effects.

### Table 12. Low Speed External Clock (LSE) Characteristics

$T_A$ = 25 °C, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operation Range | $T_A$ = -40 °C ~ 85 °C | 2.5 | — | 5.5 | V |
| $f_{CK\_LSE}$ | LSE Frequency | $V_{DD}$ = 2.5 V ~ 5.5 V | — | 32.768 | — | kHz |
| $R_F$ | Internal Feedback Resistor | — | — | 10 | — | MΩ |
| $R_{ESR}$ | Equivalent Series Resistance | $V_{DD}$ = 5.0 V | 30 | — | TBD | kΩ |
| $C_L$ | Recommended Load Capacitances | $V_{DD}$ = 5.0 V | 6 | — | TBD | pF |
| $I_{DDLSE}$ | Oscillator Supply Current (High current mode) | $f_{CK\_LSE}$ = 32.768 kHz, $R_{ESR}$ = 50 kΩ, $C_L \geq$ 7 pF, $V_{DD}$ = 2.5 V ~ 5.5 V, $T_A$ = -40 °C ~ +85 °C | — | 4.0 | 5.6 | μA |
| | Oscillator Supply Current (Low Current Mode) | $f_{CK\_LSE}$ = 32.768 kHz, $R_{ESR}$ = 50 kΩ, $C_L <$ 7 pF, $V_{DD}$ = 2.5 V ~ 5.5 V, $T_A$ = -40 °C ~ +85 °C | — | 3.6 | 4.5 | μA |
| | Power Down Current | — | — | — | 0.01 | μA |
| $t_{SULSE}$ | Startup Time (Low Current Mode) | $f_{CK\_LSI}$ = 32.768 kHz, $V_{DD}$ = 2.5 V ~ 5.5 V | 500 | — | — | ms |

## Internal Clock Characteristics

### Table 13. High Speed Internal Clock (HSI) Characteristics

$T_A$ = 25 °C, unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operation Range | $T_A$ = -40 °C ~ 85 °C | 2.5 | — | 5.5 | V |
| $f_{HSI}$ | HSI Frequency | $V_{DD}$ = 5 V @ 25 °C | — | 20 | — | MHz |
| $ACC_{HSI}$ | Factory Calibrated HSI Oscillator Frequency Accuracy | $V_{DD}$ = 5.0 V, $T_A$ = 25 °C | -2 | — | 2 | % |
| | | $V_{DD}$ = 2.5 V ~ 5.5 V, $T_A$ = -40 °C ~ 85 °C | -3 | — | 3 | % |
| Duty | Duty Cycle | $f_{HSI}$ = 20 MHz | 35 | — | 65 | % |
| $I_{DDHSI}$ | Oscillator Supply Current | $f_{HSI}$ = 20 MHz @ $V_{DD}$ = 2.5 V ~ 5.5 V | — | — | 140 | μA |
| | Power Down Current | | — | — | 0.01 | μA |
| $T_{SUHSI}$ | HSI Oscillator Startup time | $f_{HSI}$ = 20 MHz | — | — | 20 | μs |

### Table 14. Low Speed Internal Clock (LSI) Characteristics

$T_A$ = 25 °C, unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operation Range | $T_A$ = -40 °C ~ 85 °C | 2.5 | — | 5.5 | V |
| $f_{LSI}$ | Low Speed Internal Oscillator Frequency (LSI) | $V_{DD}$ = 5.0 V, $T_A$ = -40 °C ~ 85 °C | 21 | 32 | 43 | kHz |
| $ACC_{LSI}$ | LSI Frequency Accuracy | $V_{DD}$ = 5.0 V, with factory-trimmed | -10 | — | +10 | % |
| $I_{DDLSI}$ | LSI Oscillator Operating Current | $V_{DD}$ = 5.0 V | — | 0.5 | 0.8 | μA |
| $t_{SULSI}$ | LSI Oscillator Startup Time | $V_{DD}$ = 5.0 V | — | — | 100 | μs |

## Memory Characteristics

### Table 15. Flash Memory Characteristics

$T_A$ = 25 °C, unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $N_{ENDU}$ | Number of Guaranteed Program/ Erase Cycles before failure (Endurance) | $T_A$ = -40 °C ~ 85 °C | 10 | — | — | K cycles |
| $t_{RET}$ | Data Retention Time | $T_A$ = -40 °C ~ 85 °C | 10 | — | — | Years |
| $t_{PROG}$ | Word Programming Time | $T_A$ = -40 °C ~ 85 °C | 20 | — | — | μs |
| $t_{ERASE}$ | Page Erase Time | $T_A$ = -40 °C ~ 85 °C | 2 | — | — | ms |
| $t_{MERASE}$ | Mass Erase Time | $T_A$ = -40 °C ~ 85 °C | 10 | — | — | ms |

## I/O Port Characteristics

### Table 16. I/O Port Characteristics

$T_A$ = 25 °C, unless otherwise specified.

| Symbol | Parameter | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{IL}$ | Low Level Input Current | 5.0 V I/O | $V_I$ = $V_{SS}$, On-chip pull-up resister disabled | — | — | 3 | μA |
| | | Reset pin | | — | — | 3 | μA |
| $I_{IH}$ | High Level Input Current | 5.0 V I/O | $V_I$ = $V_{DD}$, On-chip pull-down resister disabled | — | — | 3 | μA |
| | | Reset pin | | — | — | 3 | μA |
| $V_{IL}$ | Low Level Input Voltage | 5.0 V I/O | | -0.5 | — | $V_{DD}$ × 0.35 | V |
| | | Reset pin | | -0.5 | — | $V_{DD}$ × 0.35 | V |
| $V_{IH}$ | High Level Input Voltage | 5.0 V I/O | | $V_{DD}$ × 0.65 | — | $V_{DD}$ + 0.5 | V |
| | | Reset pin | | $V_{DD}$ × 0.65 | — | $V_{DD}$ + 0.5 | V |
| $V_{HYS}$ | Schmitt Trigger Input Voltage Hysteresis | 5.0 V I/O | | — | 0.12 × $V_{DD}$ | — | mV |
| | | Reset pin | | — | 0.12 × $V_{DD}$ | — | mV |
| $I_{OL}$ | Low Level Output Current (GPIO Sink Current) | 5.0 V I/O 4 mA drive, $V_{OL}$ = 0.6 V | | 4 | — | — | mA |
| | | 5.0 V I/O 8 mA drive, $V_{OL}$ = 0.6 V | | 8 | — | — | mA |
| | | 5.0 V I/O 12 mA drive, $V_{OL}$ = 0.6 V | | 12 | — | — | mA |
| | | 5.0 V I/O 16 mA drive, $V_{OL}$ = 0.6 V | | 16 | — | — | mA |
| $I_{OH}$ | High Level Output Current (GPIO Source Current) | 5.0 V I/O 4 mA drive, $V_{OH}$ = $V_{DD}$ - 0.6 V | | — | 4 | — | mA |
| | | 5.0 V I/O 8 mA drive, $V_{OH}$ = $V_{DD}$ - 0.6 V | | — | 8 | — | mA |
| | | 5.0 V I/O 12 mA drive, $V_{OH}$ = $V_{DD}$ - 0.6 V | | — | 12 | — | mA |
| | | 5.0 V I/O 16 mA drive, $V_{OH}$ = $V_{DD}$ - 0.6 V | | — | 16 | — | mA |

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OL}$ | Low Level Output Voltage | 5.0 V 4 mA drive I/O, $I_{OL}$ = 4 mA | — | — | 0.6 | V |
| | | 5.0 V 8 mA drive I/O, $I_{OL}$ = 8 mA | — | — | 0.6 | V |
| | | 5.0 V 12 mA drive I/O, $I_{OL}$ = 12 mA | — | — | 0.6 | V |
| | | 5.0 V 16 mA drive I/O, $I_{OL}$ = 16 mA | — | — | 0.6 | V |
| $V_{OH}$ | High Level Output Voltage | 5.0 V 4 mA drive I/O, $I_{OH}$ = 4 mA | $V_{DD}$ - 0.6 | — | — | V |
| | | 5.0 V 8 mA drive I/O, $I_{OH}$ = 8 mA | $V_{DD}$ - 0.6 | — | — | V |
| | | 5.0 V 12 mA drive I/O, $I_{OH}$ = 12 mA | $V_{DD}$ - 0.6 | — | — | V |
| | | 5.0 V 16 mA drive I/O, $I_{OH}$ = 16 mA | $V_{DD}$ - 0.6 | — | — | V |
| $R_{PU}$ | Internal Pull-up Resistor | $V_{DD}$ = 5.0 V | — | 50 | — | kΩ |
| | | $V_{DD}$ = 3.3 V | — | 76 | — | kΩ |
| $R_{PD}$ | Internal Pull-down Resistor | $V_{DD}$ = 5.0 V | — | 50 | — | kΩ |
| | | $V_{DD}$ = 3.3 V | — | 76 | — | kΩ |



## ADC Characteristics

### Table 17. ADC Characteristics

$T_A$ = 25 °C, unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Operating Voltage | — | 2.5 | 5.0 | 5.5 | V |
| $V_{ADCIN}$ | A/D Converter Input Voltage Range | — | 0 | — | $V_{REF+}$ | V |
| $V_{REF+}$ | A/D Converter Reference Voltage | — | — | $V_{DDA}$ | $V_{DDA}$ | V |
| $I_{ADC}$ | Current Consumption | $V_{DDA}$ = 5.0 V | — | 1.4 | 1.5 | mA |
| $I_{ADC\_DN}$ | Power Down Current Consumption | $V_{DDA}$ = 5.0 V | — | — | 0.1 | μA |
| $f_{ADC}$ | A/D Converter Clock Frequency | — | 0.7 | — | 16 | MHz |
| $f_S$ | Sampling Rate | — | 0.05 | — | 1 | MHz |
| $t_{DL}$ | Data Latency | — | — | 12.5 | — | $1/f_{ADC}$ Cycles |
| $t_{S\&H}$ | Sampling & Hold Time | — | — | 3.5 | — | $1/f_{ADC}$ Cycles |
| $t_{ADCCONV}$ | A/D Converter Conversion Time | — | — | 16 | — | $1/f_{ADC}$ Cycles |
| $R_I$ | Input Sampling Switch Resistance | — | — | — | 1 | kΩ |
| $C_I$ | Input Sampling Capacitance | No pin/pad capacitance included | — | 4 | — | pF |
| $t_{SU}$ | Startup Time | — | — | — | 1 | μs |
| N | Resolution | — | — | 12 | — | bits |

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| INL | Integral Non-linearity Error | $f_S$ = 750 kHz, $V_{DDA}$ = 5.0 V | — | ±2 | ±5 | LSB |
| DNL | Differential Non-linearity Error | $f_S$ = 750 kHz, $V_{DDA}$ = 5.0 V | — | ±1 | — | LSB |
| $E_O$ | Offset Error | — | — | — | ±10 | LSB |
| $E_G$ | Gain Error | — | — | — | ±10 | LSB |

Note: 1. Guaranteed by design, not tested in production.

2. Due to the A/D Converter input channel and GPIO pin-shared function design limitation, the $V_{DDA}$ supply power of the A/D Converter has to be equal to the $V_{DD}$ supply power of the MCU in the application circuit.
3. The figure below shows the equivalent circuit of the A/D Converter Sample-and-Hold input stage where $C_I$ is the storage capacitor, $R_I$ is the resistance of the sampling switch and $R_S$ is the output impedance of the signal source $V_S$. Normally the sampling phase duration is approximately, $3.5/f_{ADC}$. The capacitance, $C_I$, must be charged within this time frame and it must be ensured that the voltage at its terminals becomes sufficiently close to $V_S$ for accuracy. To guarantee this, $R_S$ is not allowed to have an arbitrarily large value.

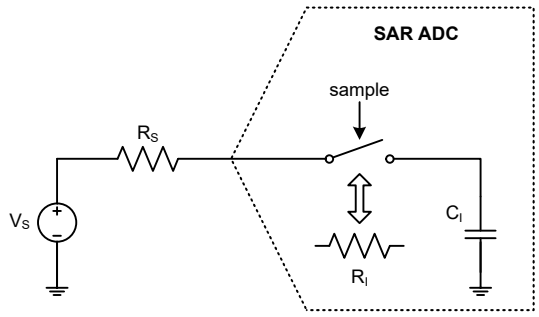



**Figure 12. ADC Sampling Network Model**

The worst case occurs when the extremities of the input range (0V and $V_{REF}$) are sampled consecutively. In this situation a sampling error below 1/4 LSB is ensured by using the following equation:

$$R_S < \frac{3.5}{f_{ADC} C_I \ln(2^{N+2})} - R_I$$

Where $f_{ADC}$ is the ADC clock frequency and N is the ADC resolution (N = 12 in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model.

If, in a system where the A/D Converter is used, there are no rail-to-rail input voltage variations between consecutive sampling phases, $R_S$ may be larger than the value indicated by the equation above.

## MCTM/GPTM/PWM Characteristics

**Table 18. MCTM/GPTM/PWM Characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{TM}$ | Timer Clock Source for MCTM, GPTM and PWM | — | — | — | $f_{PCLK}$ | MHz |
| $t_{RES}$ | Timer Resolution Time | — | 1 | — | — | $f_{TM}$ |
| $f_{EXT}$ | External Single Frequency on Channel 1 ~ 4 | — | — | — | 1/2 | $f_{TM}$ |
| RES | Timer Resolution | — | — | — | 16 | bits |

## I²C Characteristics

**Table 19. I²C Characteristics**

| Symbol | Parameter | Standard Mode | | Fast Mode | | Fast Plus Mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $f_{SCL}$ | SCL Clock Frequency | — | 100 | — | 400 | — | 1000 | kHz |
| $t_{SCL(H)}$ | SCL Clock High Time | 4.5 | — | 1.125 | — | 0.45 | — | μs |
| $t_{SCL(L)}$ | SCL Clock Low Time | 4.5 | — | 1.125 | — | 0.45 | — | μs |
| $t_{FALL}$ | SCL And SDA Fall Time | — | 1.3 | — | 0.34 | — | 0.135 | μs |
| $t_{RISE}$ | SCL And SDA Rise Time | — | 1.3 | — | 0.34 | — | 0.135 | μs |
| $t_{SU(SDA)}$ | SDA Data Setup Time | 500 | — | 125 | — | 50 | — | ns |
| $t_{H(SDA)}$ | SDA Data Hold Time (Note 5) | 0 | — | 0 | — | 0 | — | ns |
| | SDA Data Hold Time (Note 6) | 100 | — | 100 | — | 100 | — | ns |
| $t_{VD(SDA)}$ | SDA Data Valid Time | — | 1.6 | — | 0.475 | — | 0.25 | μs |
| $t_{SU(STA)}$ | START Condition Setup Time | 500 | — | 125 | — | 50 | — | ns |
| $t_{H(STA)}$ | START Condition Hold Time | 0 | — | 0 | — | 0 | — | ns |
| $t_{SU(STO)}$ | STOP Condition Setup Time | 500 | — | 125 | — | 50 | — | ns |

Note: 1. Guaranteed by design, not tested in production.
2. To achieve 100 kHz standard mode, the peripheral clock frequency must be higher than 2 MHz.
3. To achieve 400 kHz fast mode, the peripheral clock frequency must be higher than 8 MHz.
4. To achieve 1 MHz fast mode plus, the peripheral clock frequency must be higher than 20 MHz.
5. The above characteristic parameters of the I²C bus timing are based on: COMB_FILTER_En = 0 and SEQ_FILTER = 00.
6. The above characteristic parameters of the I²C bus timing are based on: COMB_FILTER_En = 1 and SEQ_FILTER = 00.

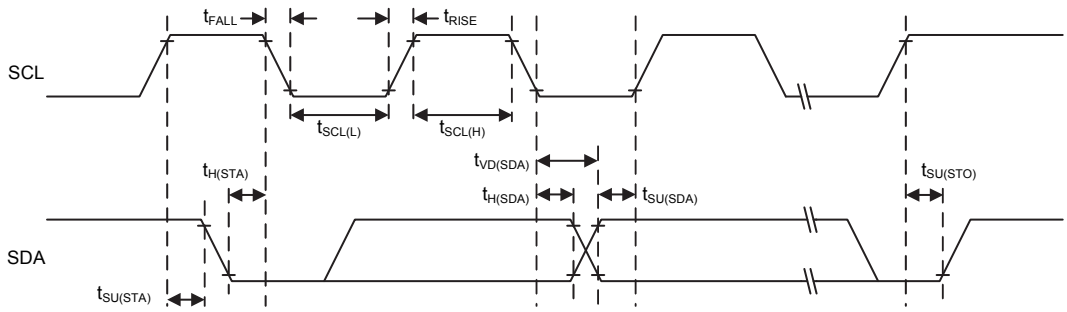



**Figure 13. I²C Timing Diagrams**

## SPI Characteristics

### Table 20. SPI Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **SPI Master Mode** | | | | | | |
| $f_{SCK}$ | SPI Master Output SCK Clock Frequency | Master mode SPI peripheral clock frequency $f_{PCLK}$ | — | — | $f_{PCLK}/2$ | MHz |
| $t_{SCK(H)}$ $t_{SCK(L)}$ | SCK Clock High and Low Time | — | $t_{SCK}/2$ - 2 | — | $t_{SCK}/2$ + 1 | ns |
| $t_{V(MO)}$ | Data Output Valid Time | — | — | — | 5 | ns |
| $t_{H(MO)}$ | Data Output Hold Time | — | 2 | — | — | ns |
| $t_{SU(MI)}$ | Data Input Setup Time | — | 5 | — | — | ns |
| $t_{H(MI)}$ | Data Input Hold Time | — | 5 | — | — | ns |
| **SPI Slave Mode** | | | | | | |
| $f_{SCK}$ | SPI Slave Input SCK Clock Frequency | Slave mode SPI peripheral clock frequency $f_{PCLK}$ | — | — | $f_{PCLK}/3$ | MHz |
| $Duty_{SCK}$ | SPI Slave Input SCK Clock Duty Cycle | — | 30 | — | 70 | % |
| $t_{SU(SEL)}$ | SEL Enable Setup Time | — | 3 $t_{PCLK}$ | — | — | ns |
| $t_{H(SEL)}$ | SEL Enable Hold Time | — | 2 $t_{PCLK}$ | — | — | ns |
| $t_{A(SO)}$ | Data Output Access Time | — | — | — | 3 $t_{PCLK}$ | ns |
| $t_{DIS(SO)}$ | Data Output Disable Time | — | — | — | 10 | ns |
| $t_{V(SO)}$ | Data Output Valid Time | — | — | — | 25 | ns |
| $t_{H(SO)}$ | Data Output Hold Time | — | 15 | — | — | ns |
| $t_{SU(SI)}$ | Data Input Setup Time | — | 5 | — | — | ns |
| $t_{H(SI)}$ | Data Input Hold Time | — | 4 | — | — | ns |

Note: 1. $f_{SCK}$ is SPI output/input clock frequency and $t_{SCK}$= 1/$f_{SCK}$.
2. $f_{PCLK}$ is SPI peripheral clock frequency and $t_{PCLK}$= 1/$f_{PCLK}$.

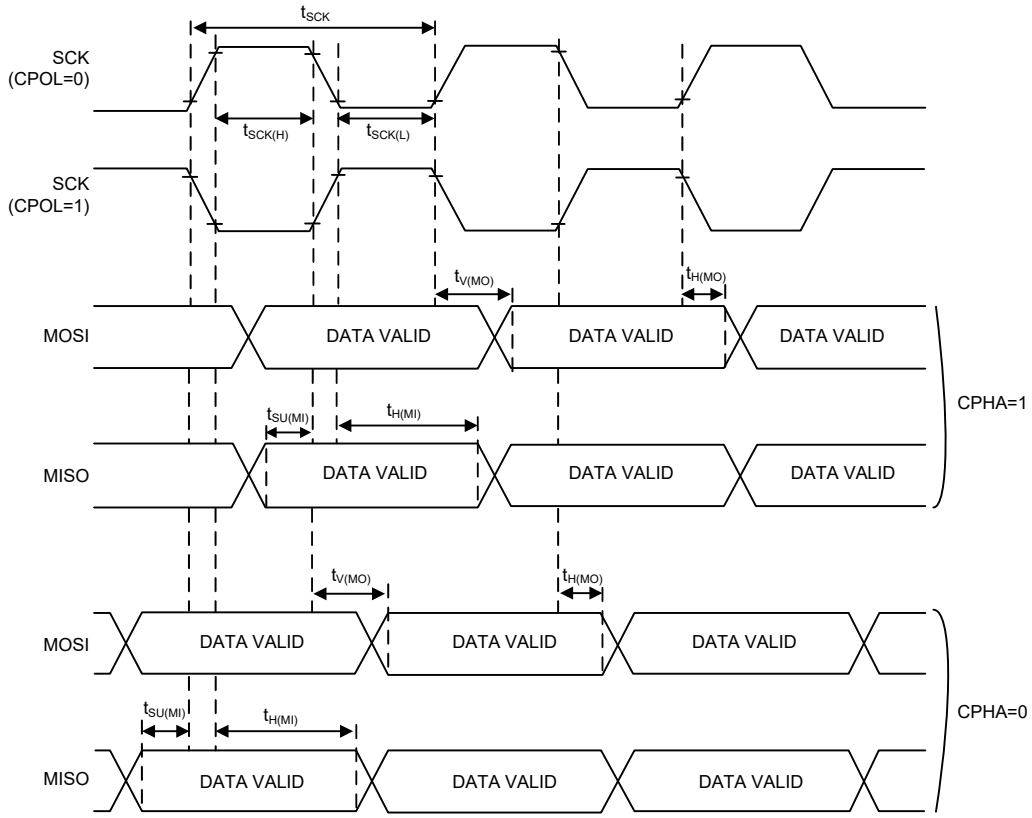



**Figure 14. SPI Timing Diagrams – SPI Master Mode**

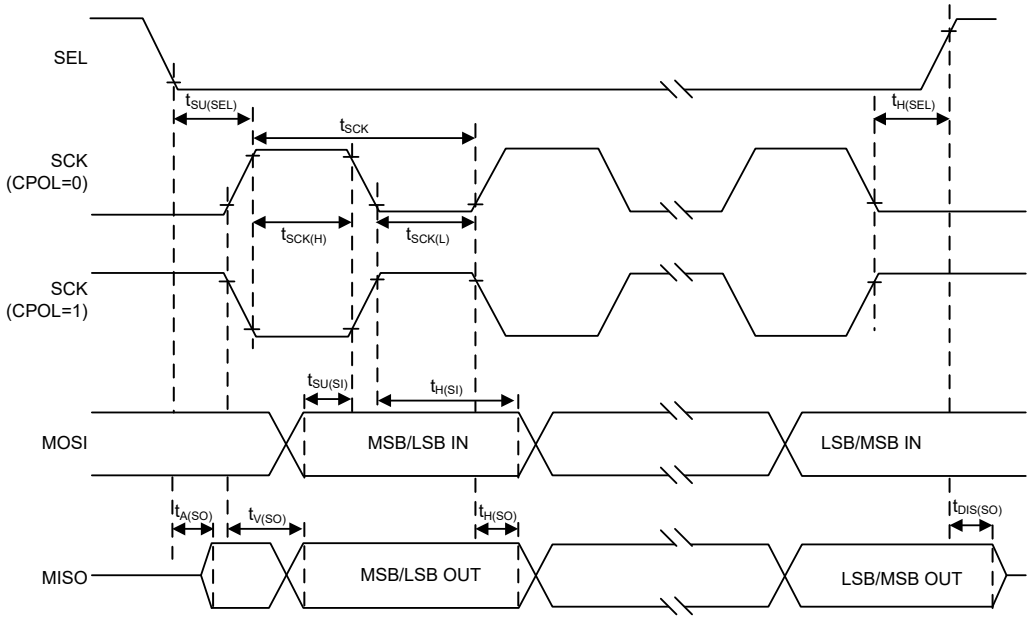



**Figure 15. SPI Timing Diagrams – SPI Slave Mode with CPHA=1**

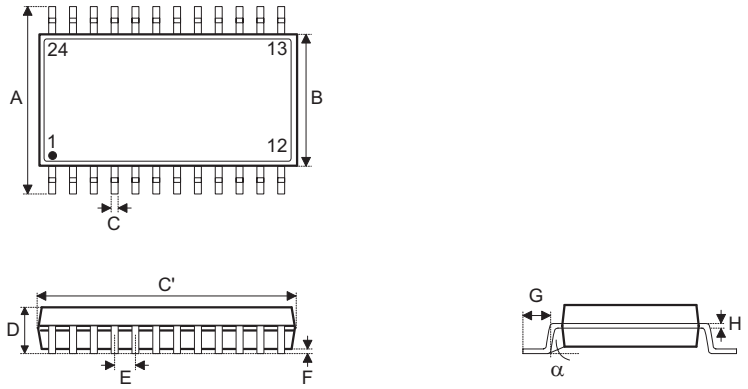
# 6 Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

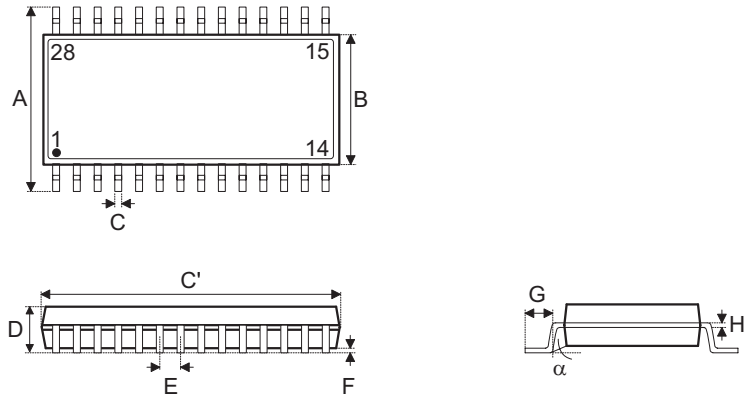
## 24-pin SSOP (150mil) Outline Dimensions




| Symbol | Dimensions in inch | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | — | 0.236 BSC | — |
| B | — | 0.154 BSC | — |
| C | 0.008 | — | 0.012 |
| C’ | — | 0.341 BSC | — |
| D | — | — | 0.069 |
| E | — | 0.025 BSC | — |
| F | 0.004 | — | 0.010 |
| G | 0.016 | — | 0.050 |
| H | 0.004 | — | 0.010 |
| α | 0° | — | 8° |

| Symbol | Dimensions in mm | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | — | 6.00 BSC | — |
| B | — | 3.90 BSC | — |
| C | 0.20 | — | 0.30 |
| C’ | — | 8.66 BSC | — |
| D | — | — | 1.75 |
| E | — | 0.635 BSC | — |
| F | 0.10 | — | 0.25 |
| G | 0.41 | — | 1.27 |
| H | 0.10 | — | 0.25 |
| α | 0° | — | 8° |

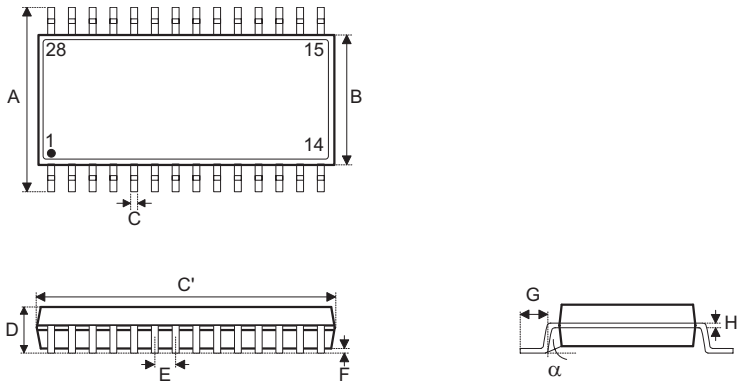
## 28-pin SSOP (150mil) Outline Dimensions




| Symbol | Dimensions in inch | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | — | 0.236 BSC | — |
| B | — | 0.154 BSC | — |
| C | 0.008 | — | 0.012 |
| C’ | — | 0.390 BSC | — |
| D | — | — | 0.069 |
| E | — | 0.025 BSC | — |
| F | 0.004 | — | 0.010 |
| G | 0.016 | — | 0.050 |
| H | 0.004 | — | 0.010 |
| α | 0° | — | 8° |

| Symbol | Dimensions in mm | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | — | 6.00 BSC | — |
| B | — | 3.90 BSC | — |
| C | 0.20 | — | 0.30 |
| C’ | — | 9.90 BSC | — |
| D | — | — | 1.75 |
| E | — | 0.635 BSC | — |
| F | 0.10 | — | 0.25 |
| G | 0.41 | — | 1.27 |
| H | 0.10 | — | 0.25 |
| α | 0° | — | 8° |

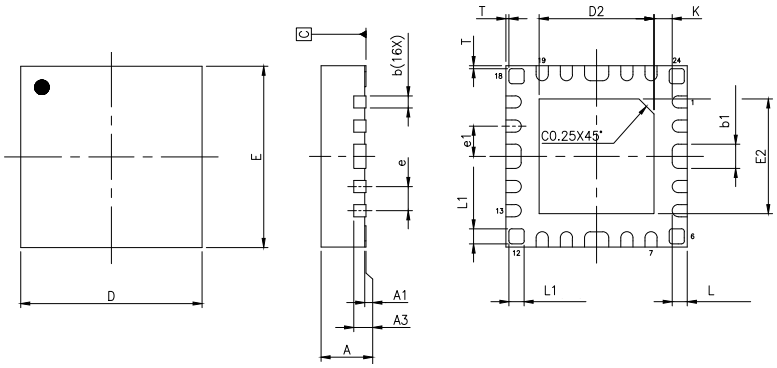
## 28-pin SOP (300mil) Outline Dimensions




| Symbol | Dimensions in inch | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | — | 0.406 BSC | — |
| B | — | 0.295 BSC | — |
| C | 0.012 | — | 0.020 |
| C' | — | 0.705 BSC | — |
| D | — | — | 0.104 |
| E | — | 0.050 BSC | — |
| F | 0.004 | — | 0.012 |
| G | 0.016 | — | 0.050 |
| H | 0.008 | — | 0.013 |
| α | 0° | — | 8° |

| Symbol | Dimensions in mm | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | — | 10.30 BSC | — |
| B | — | 7.50 BSC | — |
| C | 0.31 | — | 0.51 |
| C' | — | 17.90 BSC | — |
| D | — | — | 2.65 |
| E | — | 1.27 BSC | — |
| F | 0.10 | — | 0.30 |
| G | 0.40 | — | 1.27 |
| H | 0.20 | — | 0.33 |
| α | 0° | — | 8° |

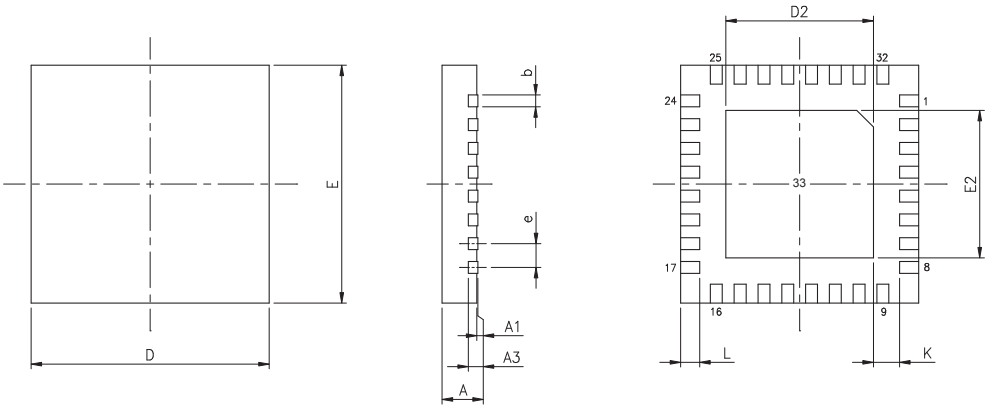
# SAW Type 24-pin QFN (3mm×3mm×0.55mm) Outline Dimensions




| Symbol | Dimensions in inch | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | 0.020 | 0.022 | 0.024 |
| A1 | 0.000 | 0.001 | 0.002 |
| A3 | — | 0.006 BSC | — |
| b | 0.006 | 0.008 | 0.010 |
| b1 | 0.014 | 0.016 | 0.018 |
| D | — | 0.118 BSC | — |
| E | — | 0.118 BSC | — |
| e | — | 0.016 BSC | — |
| e1 | — | 0.020 BSC | — |
| D2 | 0.073 | 0.075 | 0.077 |
| E2 | 0.073 | 0.075 | 0.077 |
| L | 0.006 | 0.010 | 0.014 |
| L1 | 0.008 | 0.010 | 0.012 |
| K | 0.008 | — | — |

| Symbol | Dimensions in mm | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | 0.50 | 0.55 | 0.60 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | — | 0.150 BSC | — |
| b | 0.15 | 0.20 | 0.25 |
| b1 | 0.35 | 0.40 | 0.45 |
| D | — | 3.00 BSC | — |
| E | — | 3.00 BSC | — |
| e | — | 0.40 BSC | — |
| e1 | — | 0.50 BSC | — |
| D2 | 1.85 | 1.90 | 1.95 |
| E2 | 1.85 | 1.90 | 1.95 |
| L | 0.15 | 0.25 | 0.35 |
| L1 | 0.20 | 0.25 | 0.30 |
| K | 0.20 | — | — |

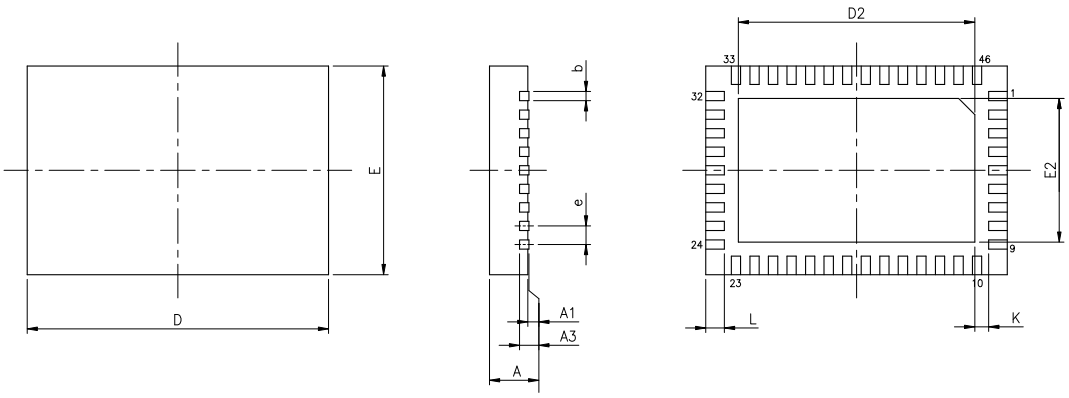
## SAW Type 33-pin QFN (4mm×4mm) Outline Dimensions




| Symbol | Dimensions in inch | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | 0.028 | 0.030 | 0.031 |
| A1 | 0.000 | 0.001 | 0.002 |
| A3 | — | 0.008 BSC | — |
| b | 0.006 | 0.008 | 0.010 |
| D | — | 0.157 BSC | — |
| E | — | 0.157 BSC | — |
| e | — | 0.016 BSC | — |
| D2 | 0.104 | 0.106 | 0.108 |
| E2 | 0.104 | 0.106 | 0.108 |
| L | 0.014 | 0.016 | 0.018 |
| K | 0.008 | — | — |

| Symbol | Dimensions in mm | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | — | 0.203 BSC | — |
| b | 0.15 | 0.20 | 0.25 |
| D | — | 4.00 BSC | — |
| E | — | 4.00 BSC | — |
| e | — | 0.40 BSC | — |
| D2 | 2.65 | 2.70 | 2.75 |
| E2 | 2.65 | 2.70 | 2.75 |
| L | 0.35 | 0.40 | 0.45 |
| K | 0.20 | — | — |

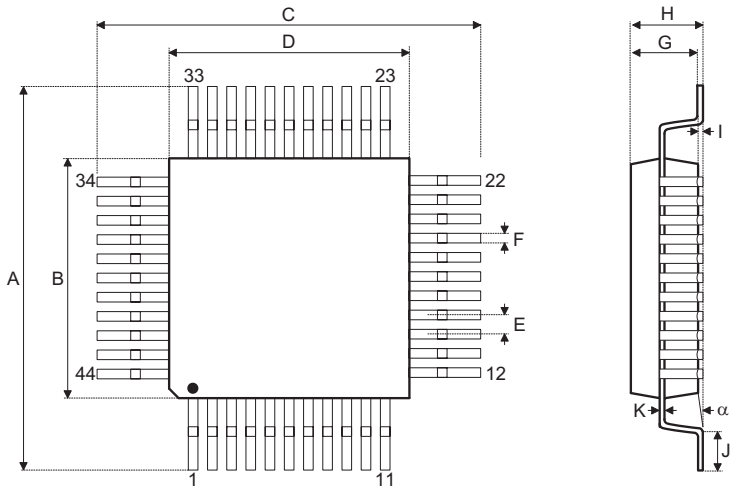
## SAW Type 46-pin QFN (6.5mm×4.5mm×0.75mm) Outline Dimensions




| Symbol | Dimensions in inch | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | 0.028 | 0.030 | 0.031 |
| A1 | 0.000 | 0.001 | 0.002 |
| A3 | — | 0.008 BSC | — |
| b | 0.006 | 0.008 | 0.010 |
| D | — | 0.256 BSC | — |
| E | — | 0.177 BSC | — |
| e | — | 0.016 BSC | — |
| D2 | 0.199 | 0.201 | 0.203 |
| E2 | 0.120 | 0.122 | 0.124 |
| L | 0.014 | 0.016 | 0.018 |
| K | 0.008 | — | — |

| Symbol | Dimensions in mm | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | — | 0.203 BSC | — |
| b | 0.15 | 0.20 | 0.25 |
| D | — | 6.50 BSC | — |
| E | — | 4.50 BSC | — |
| e | — | 0.40 BSC | — |
| D2 | 5.05 | 5.10 | 5.15 |
| E2 | 3.05 | 3.10 | 3.15 |
| L | 0.35 | 0.40 | 0.45 |
| K | 0.20 | — | — |

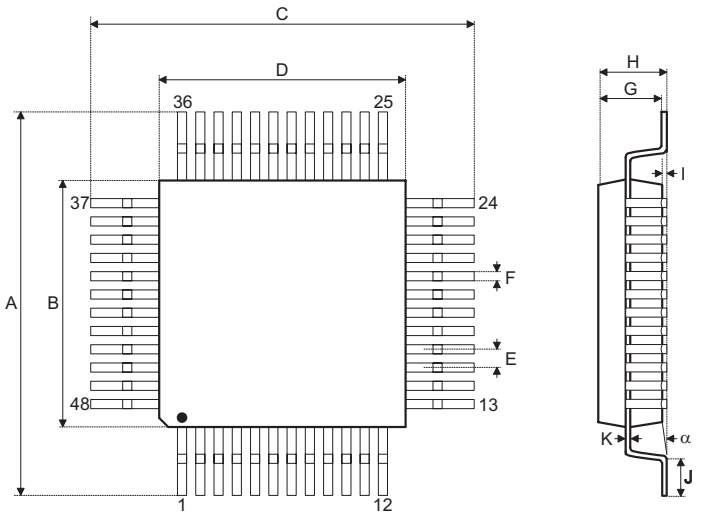
## 44-pin LQFP (10mm×10mm) (FP2.0mm) Outline Dimensions




| Symbol | Dimensions in inch | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | — | 0.472 BSC | — |
| B | — | 0.394 BSC | — |
| C | — | 0.472 BSC | — |
| D | — | 0.394 BSC | — |
| E | — | 0.032 BSC | — |
| F | 0.012 | 0.015 | 0.018 |
| G | 0.053 | 0.055 | 0.057 |
| H | — | — | 0.063 |
| I | 0.002 | — | 0.006 |
| J | 0.018 | 0.024 | 0.030 |
| K | 0.004 | — | 0.008 |
| α | 0° | — | 7° |

| Symbol | Dimensions in mm | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | — | 12.00 BSC | — |
| B | — | 10.00 BSC | — |
| C | — | 12.00 BSC | — |
| D | — | 10.00 BSC | — |
| E | — | 0.80 BSC | — |
| F | 0.30 | 0.37 | 0.45 |
| G | 1.35 | 1.40 | 1.45 |
| H | — | — | 1.60 |
| I | 0.05 | — | 0.15 |
| J | 0.45 | 0.60 | 0.75 |
| K | 0.09 | — | 0.20 |
| α | 0° | — | 7° |

## 48-pin LQFP (7mm×7mm) Outline Dimensions




| Symbol | Dimensions in inch | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | — | 0.354 BSC | — |
| B | — | 0.276 BSC | — |
| C | — | 0.354 BSC | — |
| D | — | 0.276 BSC | — |
| E | — | 0.020 BSC | — |
| F | 0.007 | 0.009 | 0.011 |
| G | 0.053 | 0.055 | 0.057 |
| H | — | — | 0.063 |
| I | 0.002 | — | 0.006 |
| J | 0.018 | 0.024 | 0.030 |
| K | 0.004 | — | 0.008 |
| α | 0° | — | 7° |

| Symbol | Dimensions in mm | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | — | 9.0 BSC | — |
| B | — | 7.0 BSC | — |
| C | — | 9.0 BSC | — |
| D | — | 7.0 BSC | — |
| E | — | 0.5 BSC | — |
| F | 0.17 | 0.22 | 0.27 |
| G | 1.35 | 1.4 | 1.45 |
| H | — | — | 1.60 |
| I | 0.05 | — | 0.15 |
| J | 0.45 | 0.60 | 0.75 |
| K | 0.09 | — | 0.20 |
| α | 0° | — | 7° |