RAM Mapping 24×4 / 22×6 / 20×8 LCD Controller Driver with Key Scan

HT16K24

Revision: V1.00 Date: June 11, 2025

www.holtek.com

Table of Contents

Features

- Operating voltage: 2.4V~5.5V
- Internal 32kHz RC oscillator
- Bias: 1/3 or 1/4; Duty: 1/4, 1/6 or 1/8
- Internal LCD bias generation from resistor divider
- I^2C-bus interface
- LCD frame frequency: 72Hz
- Up to 24×8 bits RAM for display data storage
- Various display modes
  - 24×4 patterns: 24 segments and 4 commons
  - 22×6 patterns: 22 segments and 6 commons
  - 20×8 patterns: 20 segments and 8 commons
- Key scan function
  - 24×1 matrix key scanning in 24×4 display mode
  - 22×1 matrix key scanning in 22×6 display mode
  - 20×1 matrix key scanning in 20×8 display mode
- Eight general purpose output (GPO) ports, can be set to buzzer or LED driver output
- Four driver output modes: Common, Segment, Key, GPO
- Four selectable buzzer frequencies: 1kHz, 2kHz, 4kHz, 8kHz
- Selectable hardware interrupt
- R/W address auto increment
- Low power consumption
- Manufactured in silicon gate CMOS process
- Package Types: 32-pin QFN

Applications

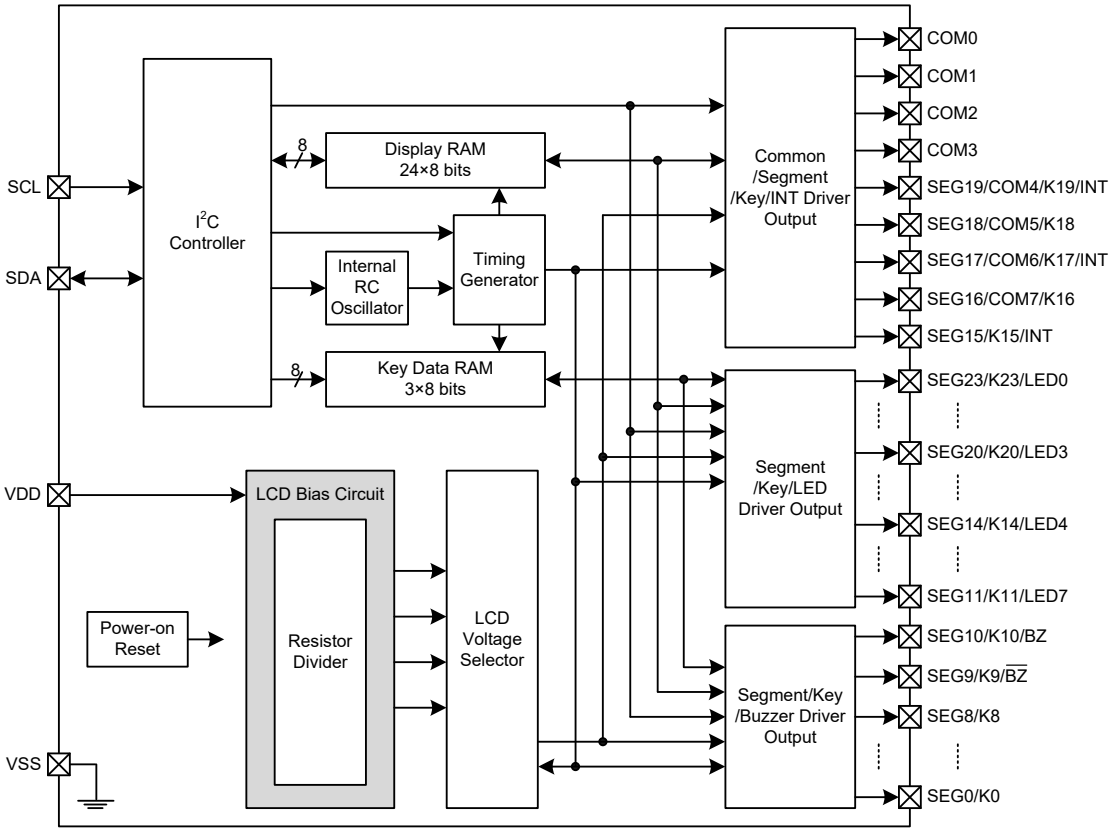
- Measurement equipment displays
- Kitchen Appliance displays
- Audio Combo displays
- Leisure products
- Household appliance
- Games
- Telephones
- Consumer electronics

General Description

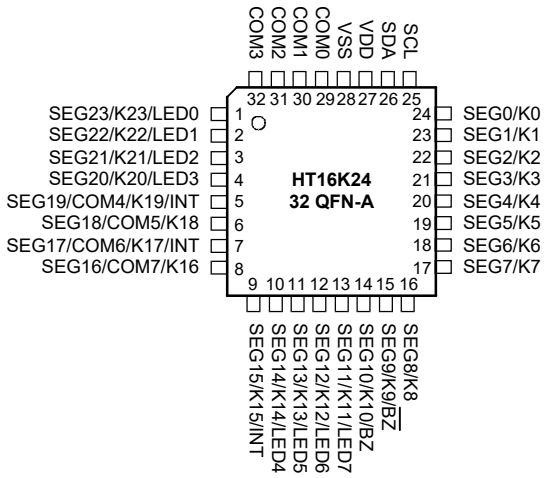
The HT16K24 device is a memory mapping and multi-function LCD controller driver which can be switched to either 1/4, 1/6 or 1/8 duty. The display modes of the device are 96 patterns (24 segments and 4 commons), 132 patterns (22 segments and 6 commons) or 160 patterns (20 segments and 8 commons). It also supports 24×1 (Maximum) key matrix circuit and supports up to 8 segment/GPO shared pin outputs to control other devices. The GPO outputs can be programmed to drive up to 8 LEDs and a set of direct push buzzer output functions.

The software configuration feature of the HT16K24 device makes it suitable for multiple LCD applications including LCD modules and display subsystems. The HT16K24 device communicates with most microprocessors or microcontrollers via a two-line bidirectional I^2C-bus.

Block Diagram



Pin Assignment

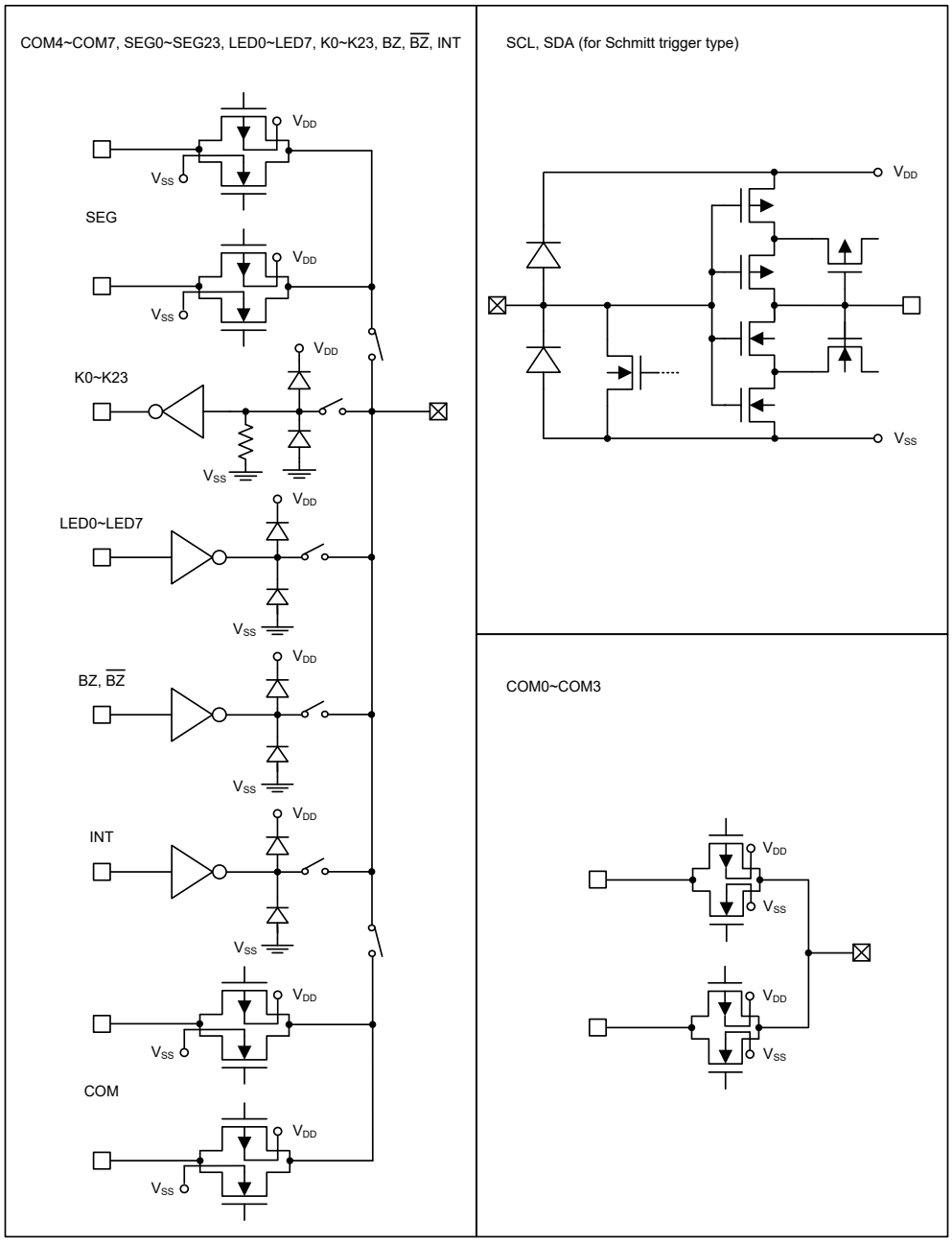


Pin Description

Pin Name	Type	Description
SDA	I/O	Serial Data Input/Output for I^2C interface
SCL	I	Serial Clock Input for I^2C interface
VDD	—	Positive power supply
VSS	—	Negative power supply, ground
COM0~COM3	O	LCD Common output
SEG19/COM4/K19/INT	I/O	• LCD Segment output • LCD Common output • Key input • Interrupt signal output
SEG18/COM5/K18	I/O	• LCD Segment output • LCD Common output • Key input
SEG17/COM6/K17/INT	I/O	• LCD Segment output • LCD Common output • Key input • Interrupt signal output
SEG16/COM7/K16	I/O	• LCD Segment output • LCD Common output • Key input
SEG15/K15/INT	I/O	• LCD Segment output • Key input • Interrupt signal output
SEG20/K20/LED3~ SEG23/K23/LED0	I/O	• LCD Segment output • Key input • LED output
SEG11/K11/LED7~ SEG14/K14/LED4	I/O	• LCD Segment output • Key input • LED output
SEG10/K10/BZ	I/O	• LCD Segment output • Key input • Buzzer frequency output

Pin Name	Type	Description
SEG9/K9/$\overline{BZ}$	I/O	• LCD Segment output • Key input • Buzzer frequency sub-output
SEG8/K8~SEG0/K0	I/O	• LCD Segment output • Key input

Approximate Internal Connections



Absolute Maximum Ratings

Supply Voltage ..... V_{SS}-0.3V to V_{SS}+6.5V

Input Voltage ..... V_{SS}-0.3V to V_{DD}+0.3V

Storage Temperature..... -55°C to 150°C

Operating Temperature..... -40°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

V_{SS}=0V, V_{DD}=2.4V~5.5V, Ta=-40°C~85°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.4	—	5.5	V
I_{DD}	Operating Current	3V	No load, LCD display on, other functions are set to default value, BR[1:0]=10b	—	155	310	μA
		5V		—	260	420	μA
I_{DD1}	Operating Current	3V	No load, LCD display off, other functions are set to default value, BR[1:0]=10b	—	8	30	μA
		5V		—	20	60	μA
I_{STB}	Standby Current	3V	No load, standby mode, BR[1:0]=10b	—	1	3	μA
		5V		—	2	5	μA
I_{IL}	Input Leakage Current	—	V_{IN}=V_{SS} or V_{DD}	-1	—	1	μA
I_{OL1}	Low Level Output Current	3V	V_{OL}=0.4V, SDA	3	—	—	mA
		5V		6	—	—	mA
I_{OL2}	Low Level Output Current	3V	V_{OL}=0.1V_{DD}, LED pin, LCn[1:0]=00b, n=0~7	3	6	—	mA
		5V		6	12	—	mA
		3V	V_{OL}=0.1V_{DD}, LED pin, LCn[1:0]=01b, n=0~7	5	10	—	mA
		5V		10	20	—	mA
		3V	V_{OL}=0.1V_{DD}, LED pin, LCn[1:0]=10b, n=0~7	7	15	—	mA
		5V		14	30	—	mA
		3V	V_{OL}=0.1V_{DD}, LED pin, LCn[1:0]=11b, n=0~7	16	32	—	mA
		5V		32	65	—	mA
I_{OH}	High Level Output Current	3V	V_{OL}=0.9V_{DD}, LED pin, LCn[1:0]=00b, n=0~7	-0.7	-1.5	—	mA
		5V		-1.5	-2.9	—	mA
		3V	V_{OL}=0.9V_{DD}, LED pin, LCn[1:0]=01b, n=0~7	-1.3	-2.5	—	mA
		5V		-2.5	-5.1	—	mA
		3V	V_{OL}=0.9V_{DD}, LED pin, LCn[1:0]=10b, n=0~7	-1.8	-3.6	—	mA
		5V		-3.6	-7.3	—	mA
		3V	V_{OL}=0.9V_{DD}, LED pin, LCn[1:0]=11b, n=0~7	-4	-8	—	mA
		5V		-8	-16	—	mA
V_{IH}	Input High Voltage	—	SDA, SCL	0.7V_{DD}	—	V_{DD}	V
V_{IL}	Input Low Voltage	—	SDA, SCL	0	—	0.3V_{DD}	V
I_{OL4}	LCD COM Sink Current	3V	V_{OL}=0.3V	80	160	—	μA
		5V	V_{OL}=0.5V	180	360	—	μA
I_{OH1}	LCD COM Source Current	3V	V_{OH}=2.7V	-80	-120	—	μA
		5V	V_{OH}=4.5V	-120	-200	—	μA

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
I_{OL5}	LCD SEG Sink Current	3V	V_{OL}=0.3V	60	120	—	μA
		5V	V_{OL}=0.5V	120	200	—	μA
I_{OH2}	LCD SEG Source Current	3V	V_{OH}=2.7V	-40	-70	—	μA
		5V	V_{OH}=4.5V	-70	-140	—	μA
I_{OL6}	INT Sink Current	3V	V_{OL}=0.3V	1	—	—	mA
		5V	V_{OL}=0.5V	2	—	—	mA
I_{OH3}	INT Source Current	3V	V_{OL}=2.7V	-1	—	—	mA
		5V	V_{OL}=4.5V	-2	—	—	mA
I_{OL7}	BZ/$\overline{BZ}$ Sink Current	3V	V_{OL}=0.3V	16	32	—	mA
		5V	V_{OL}=0.5V	32	65	—	mA
I_{OH4}	BZ/$\overline{BZ}$ Source Current	3V	V_{OL}=2.7V	-4	-8	—	mA
		5V	V_{OL}=4.5V	-8	-16	—	mA
R_{PL}	Input Pull-low Resistance	3V	During key scan period	220	400	600	kΩ
		5V		220	400	600	kΩ

A.C. Characteristics

V_{SS}=0V, V_{DD}=2.4V~5.5V, Ta=-40°C~85°C, unless otherwise specified

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{LCD}	LCD Frame Frequency	4V	Ta=25°C, KP[2:0]=000b 1/4 duty, 1/6 duty, 1/8 duty	68.5	72.0	75.5	Hz
		4V	Ta=-40~85°C, KP[2:0]=000b 1/4 duty, 1/6 duty, 1/8 duty	50	72	105	Hz
V_{POR}	V_{DD} Start Voltage to Ensure Power-on Reset	—	—	—	—	100	mV
RR_{POR}	V_{DD} Rising Rate to Ensure Power-on Reset	—	—	0.05	—	—	V/ms
t_{POR}	Minimum Time for V_{DD} to Remain at V_{POR} to Ensure Power-on Reset	—	—	10	—	—	ms

A.C. Characteristics − I²C-Bus Interface

Ta=-40°C~85°C

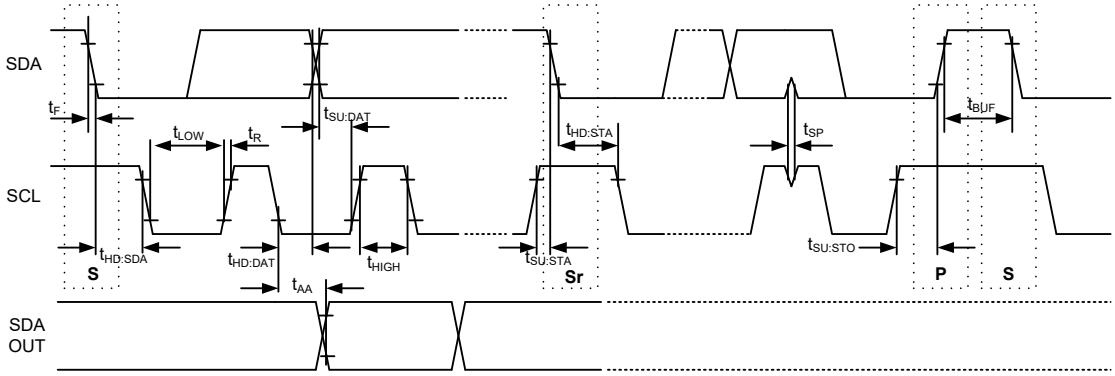
Symbol	Parameter	Test Conditions	V_{DD}=2.4V~5.5V		V_{DD}=3.0V~5.5V		Unit
			Min.	Max.	Min.	Max.	
f_{SCL}	Clock Frequency	—	—	100	—	400	kHz
t_{BUF}	Bus Free Time	Time in which the bus must be free before a new transmission can start	4.7	—	1.3	—	μs
$t_{HD:STA}$	START Condition Hold Time	After this period, the first clock pulse is generated	4.0	—	0.6	—	μs
t_{LOW}	SCL Low Time	—	4.7	—	1.3	—	μs
t_{HIGH}	SCL High Time	—	4.0	—	0.6	—	μs
$t_{SU:STA}$	START Condition Setup Time	Only relevant for repeated START condition	4.7	—	0.6	—	μs
$t_{HD:DAT}$	Data Hold Time	—	0	—	0	—	ns
$t_{SU:DAT}$	Data Setup Time	—	250	—	100	—	ns
t_R	SDA and SCL Rise Time (Note)	—	—	1.0	—	0.3	μs
t_F	SDA and SCL Fall Time (Note)	—	—	0.3	—	0.3	μs

Symbol	Parameter	Test Conditions	V_{DD}=2.4V~5.5V		V_{DD}=3.0V~5.5V		Unit
			Min.	Max.	Min.	Max.	
$t_{SU:STO}$	STOP Condition Setup Time	—	4.0	—	0.6	—	μs
t_{AA}	Output Valid from Clock	—	—	3.5	—	0.9	μs
t_{SP}	Input Filter Time Constant (SDA and SCL Pins)	Noise suppression time	—	100	—	50	ns

Note: These parameters are periodically sampled but not 100% tested.

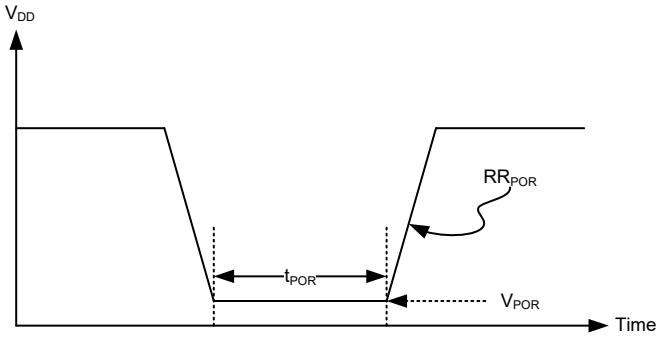
Timing Diagrams

I²C Timing



Power-on Reset Timing

The device must be powered up under certain conditions to ensure correct operation as shown in the accompanying diagram.



Note: 1. If the Power on Reset timing conditions are not satisfied in the power On/Off sequence, the internal Power on Reset circuit will not operate normally.

2. If V_{DD} drops below the minimum voltage of the operating voltage spec. during operating, the Power on Reset timing conditions must also be satisfied. That is, V_{DD} must drop to 0V and remain at 0V for 20ms (min.) before rising to the normal operating voltage.

Functional Description

Power-on Reset

When power is turned on, the device is initialised by the internal power-on reset circuit. The status of the internal circuit after initialization is as follows:

- Display mode is 24×4, 24 segments and 4 commons.
- System oscillator and the LCD bias generator are off.
- LCD Display is off.
- Key scan stops.
- All common pins are set to V_{SS}.
- All segment pins are in an input state.
- The Segment/LED/INT/BZ/$\overline{BZ}$ shared pin is set as the Segment pin.
- The control registers, key data RAM and display data RAM are set to their default value.

Data transfers on the I^2C-bus should be avoided for 1ms following power-on to allow completion of the reset procedure.

Standby Mode

Before the standby command is executed, all key data must be read.

In the standby mode, the HT16K24 cannot accept any input command or write data to the display RAM except for the system mode setting command.

If the standby mode is selected by clearing the “S” bit of the system mode setting command to “0”, the status of the standby mode is as follows:

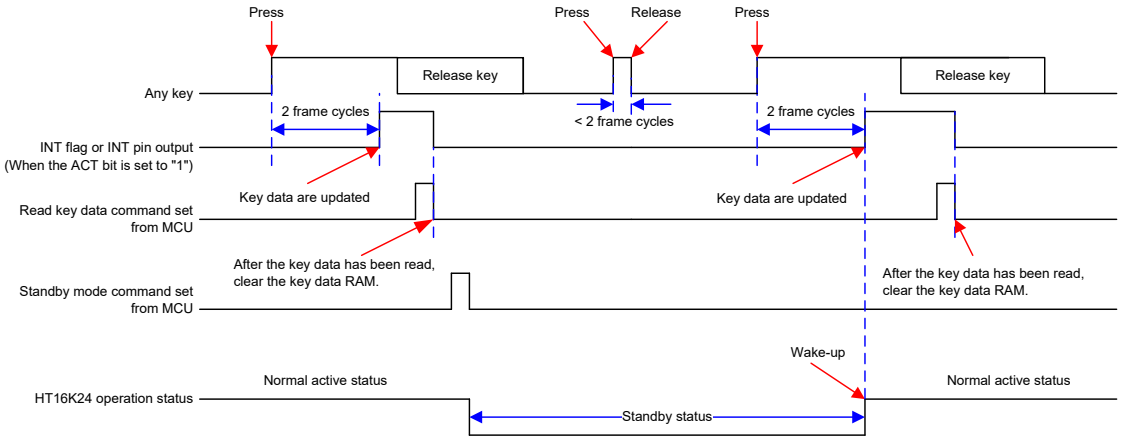
- System Oscillator is off.
- LCD display is off.
- Key scan stops.
- All key data and INT flags are cleared, until the standby mode is cancelled.
- The key matrix is pushed by any key or if the “S” bit of the system mode setting command is set to “1”, this standby mode will be cancelled and the device will wake up.
- All common pins are set to V_{SS}.
- If the “INT/ROW” bit of the driver mode setting command is set to “0”, all segment/INT shared pins are changed to input pins.
- If the “INT/ROW” bit of the driver mode setting command is set to “1”, all segment/INT shared pins are changed to input pins except for the INT pin (output).
- The INT pin output keeps at a high level when the “ACT” bit of the driver mode setting command is set to “0”. The INT pin output keeps at a low level when the “ACT” bit of the driver mode setting command is set to “1”, if the “INT/ROW” bit of the driver mode setting command is set to “1”.
- If the SEG/LED shared pin command is set to segment output function, all segment output pin status are changed to input pins.
- If the SEG/LED shared pin command is set to LED output function, all LED output pin status are not changed. The LED pin output level is kept at the setting before the standby mode, until the standby mode is canceled.

- If the SEG/Buzzer shared pin command is set to segment output function, all segment output pin status are changed to input pins.
- If the SEG/Buzzer shared pin command is set to Buzzer output function, all Buzzer output pin status are not changed, the BZ/$\overline{BZ}$ pin output level is kept at a low level, until the standby mode is canceled.

Wake-up

The device can be woken up by a valid key press or setting the "S" bit of the system mode setting command to "1". The status after wake-up is shown below.

- System Oscillator restarts for normal operation.
- The key scan will be performed.
- The previous output will be displayed until updated by each mode command set.
- The relationship between Wake-up, any key press delay time, INT flag or INT pin output is as follows.



System Oscillator

The internal logic and the LCD driver signals of the HT16K24 are timed by the integrated RC oscillator.

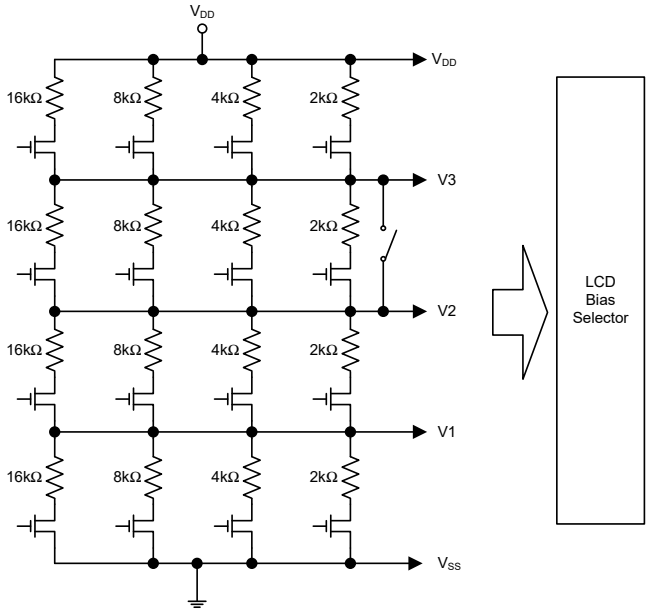
The System Clock frequency (f_{SYS}) determines the LCD frame frequency. A clock signal must always be supplied to the device as removing the clock may freeze the standby mode command is executed. At initial system power on, the System Oscillator is in the stop state.

LCD Bias Generator

The full-scale LCD voltage (V_{OP}) is obtained from (V_{DD}-V_{SS}).

Fractional LCD biasing voltages are obtained from an internal voltage divider of four series resistors connected between V_{DD} and V_{SS}. If all resistors are used, a 1/4 bias voltage level configuration is generated. The center resistor can be switched out of the circuit to provide a 1/3 bias voltage level configuration.

There are 4 kinds of bias resistor values, 2kΩ, 4kΩ, 8kΩ, and 16kΩ, as shown below.



Segment Driver Outputs

The LCD driver section includes segment outputs which should be connected directly to the LCD panel. The segment output signals are generated in accordance with the multiplexed common signals and with the data resident in the display latch. The unused segment outputs should be left open-circuit.

Common Driver Outputs

The LCD driver section includes outputs which should be connected directly to the LCD panel. The common output signals are generated in accordance with the selected LCD drive mode. The unused common outputs should be left open-circuit.

Address Pointer

The addressing mechanism for the display RAM is implemented using the address pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the address pointer by the Address pointer command.

Frame Frequency

The device provides one frame frequency, which is 72Hz.

Display Memory – RAM Structure

The display RAM is a static 24×8-bit RAM where the LCD data is stored. A logic "1" in the RAM bit-map indicates the "on" state of the corresponding LCD segment; similarly a logic 0 indicates the "off" state.

There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the common outputs. The following tables show the mapping from the RAM to the LCD pattern:

Output	COM3	COM2	COM1	COM0	Output	COM3	COM2	COM1	COM0	Address
SEG1					SEG0					00H
SEG3					SEG2					01H
SEG5					SEG4					02H
SEG7					SEG6					03H
SEG9					SEG8					04H
SEG11					SEG10					05H
SEG13					SEG12					06H
SEG15					SEG14					07H
SEG17					SEG16					08H
SEG19					SEG18					09H
SEG21					SEG20					0AH
SEG23					SEG22					0BH
	D7	D6	D5	D4		D3	D2	D1	D0	Data Bit

RAM Mapping of 24×4 Display Mode

Output			SEG18/ COM5	SEG19/ COM4	COM3	COM2	COM1	COM0	Address
SEG0	—	—							00H
SEG1	—	—							01H
SEG2	—	—							02H
SEG3	—	—							03H
SEG4	—	—							04H
SEG5	—	—							05H
SEG6	—	—							06H
SEG7	—	—							07H
SEG8	—	—							08H
SEG9	—	—							09H
SEG10	—	—							0AH
SEG11	—	—							0BH
SEG12	—	—							0CH
SEG13	—	—							0DH
SEG14	—	—							0EH
SEG15	—	—							0FH
SEG16	—	—							10H
SEG17	—	—							11H
SEG20	—	—							12H
SEG21	—	—							13H
SEG22	—	—							14H
SEG23	—	—							15H
	D7	D6	D5	D4	D3	D2	D1	D0	Data Bit

RAM Mapping of 22×6 Display Mode

Output	SEG16/ COM7	SEG17/ COM6	SEG18/ COM5	SEG19/ COM4	COM3	COM2	COM1	COM0	Address
SEG0									00H
SEG1									01H
SEG2									02H
SEG3									03H
SEG4									04H
SEG5									05H
SEG6									06H
SEG7									07H
SEG8									08H
SEG9									09H
SEG10									0AH
SEG11									0BH
SEG12									0CH
SEG13									0DH
SEG14									0EH
SEG15									0FH
SEG20									10H
SEG21									11H
SEG22									12H
SEG23									13H
	D7	D6	D5	D4	D3	D2	D1	D0	Data Bit

RAM Mapping of 20×8 Display Mode

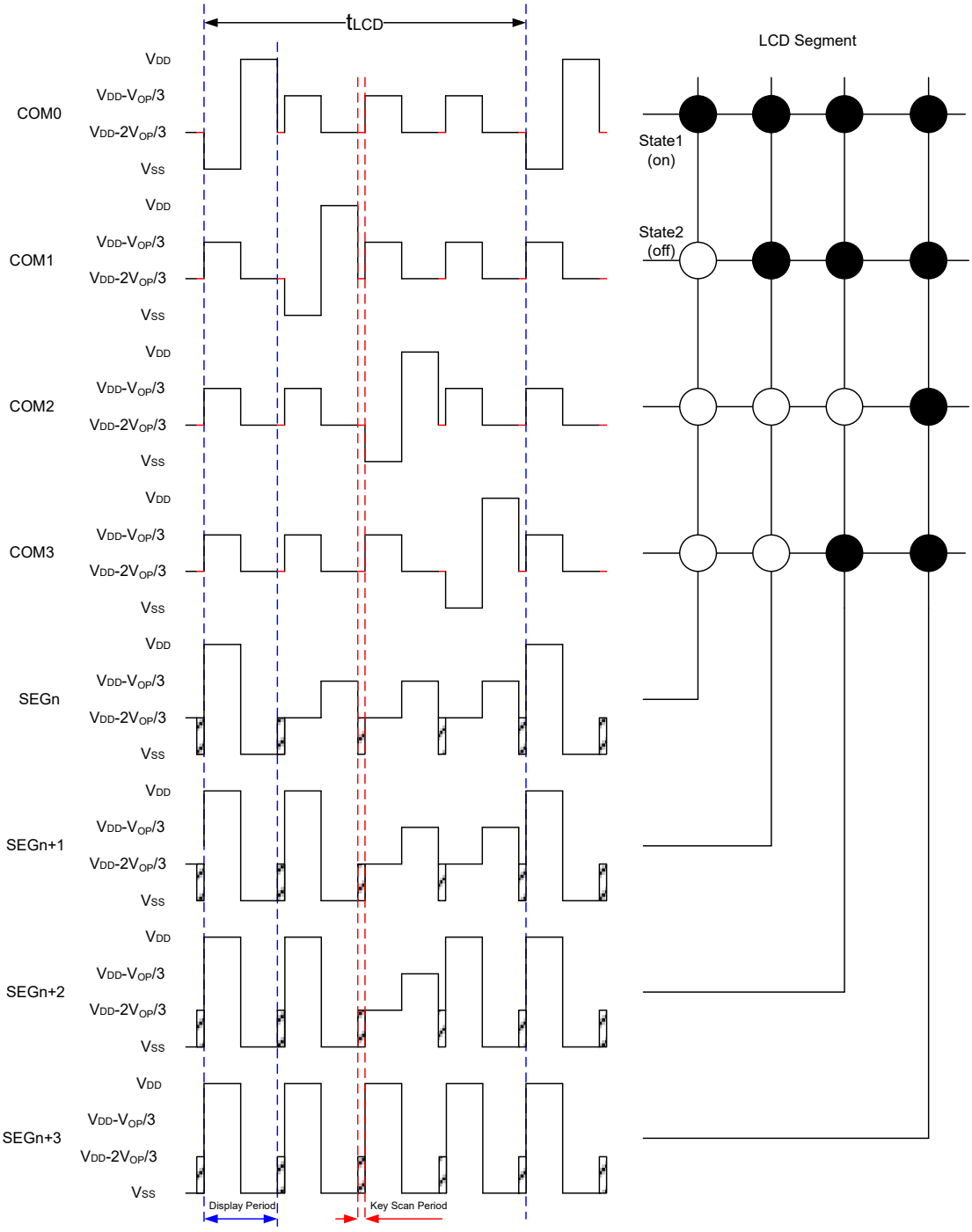
MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0

Display Data Transfer Format for I²C Bus Interface

LCD Drive Mode Waveforms

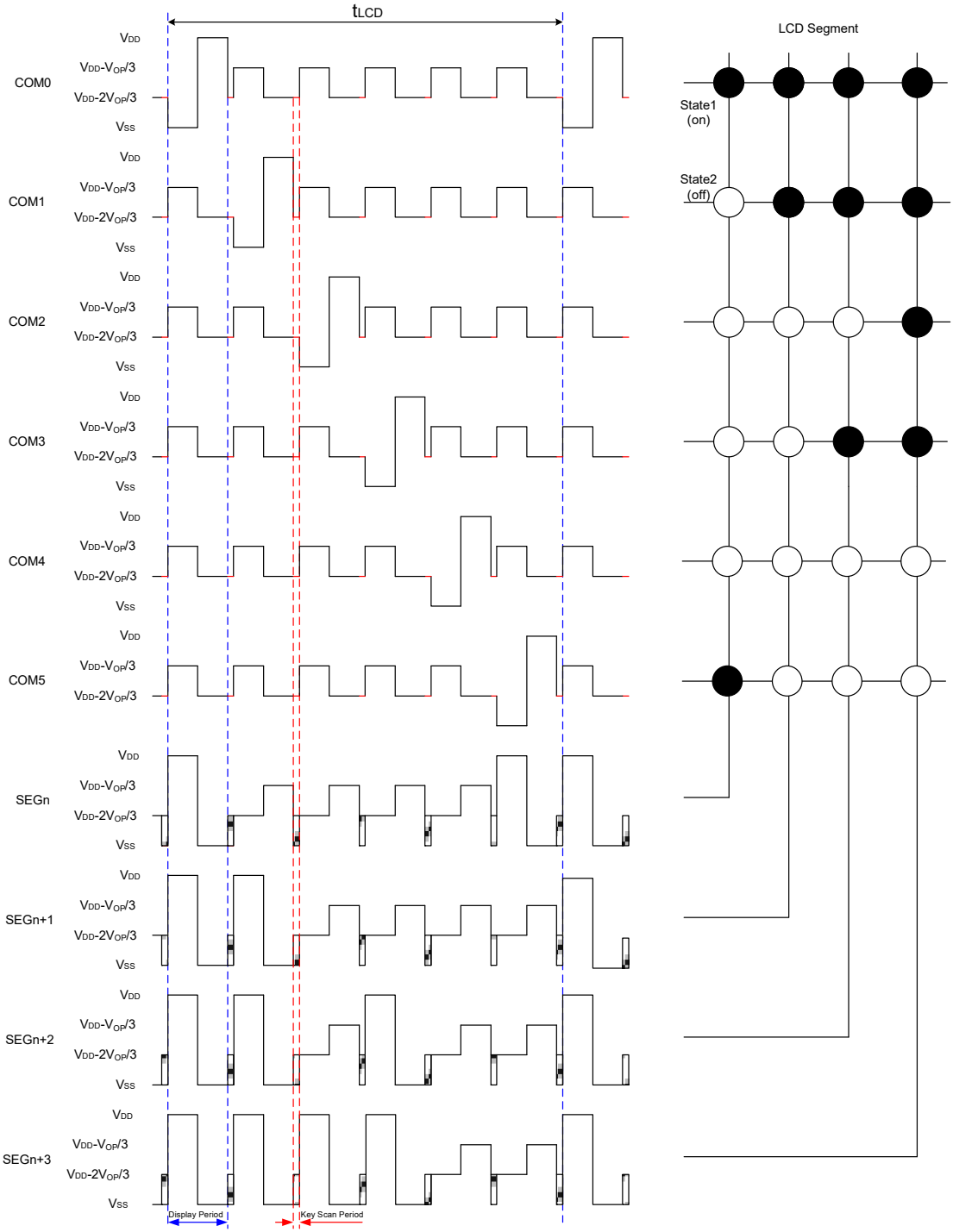
- When the LCD drive mode is selected as 1/4 duty and 1/3 bias, the waveform and LCD display are shown as follows.



Waveforms for 1/4 Duty Drive Mode with 1/3 Bias (V_{OP}=V_{DD}-V_{SS})

Note: 1. t_{LCD}=1/f_{LCD}.
2. The display period is about 3.375ms (108 clock cycles) without key scan period.
3. The key scan period is about 62.5μs (2 clock cycles) @ KP[2:0]=000b.

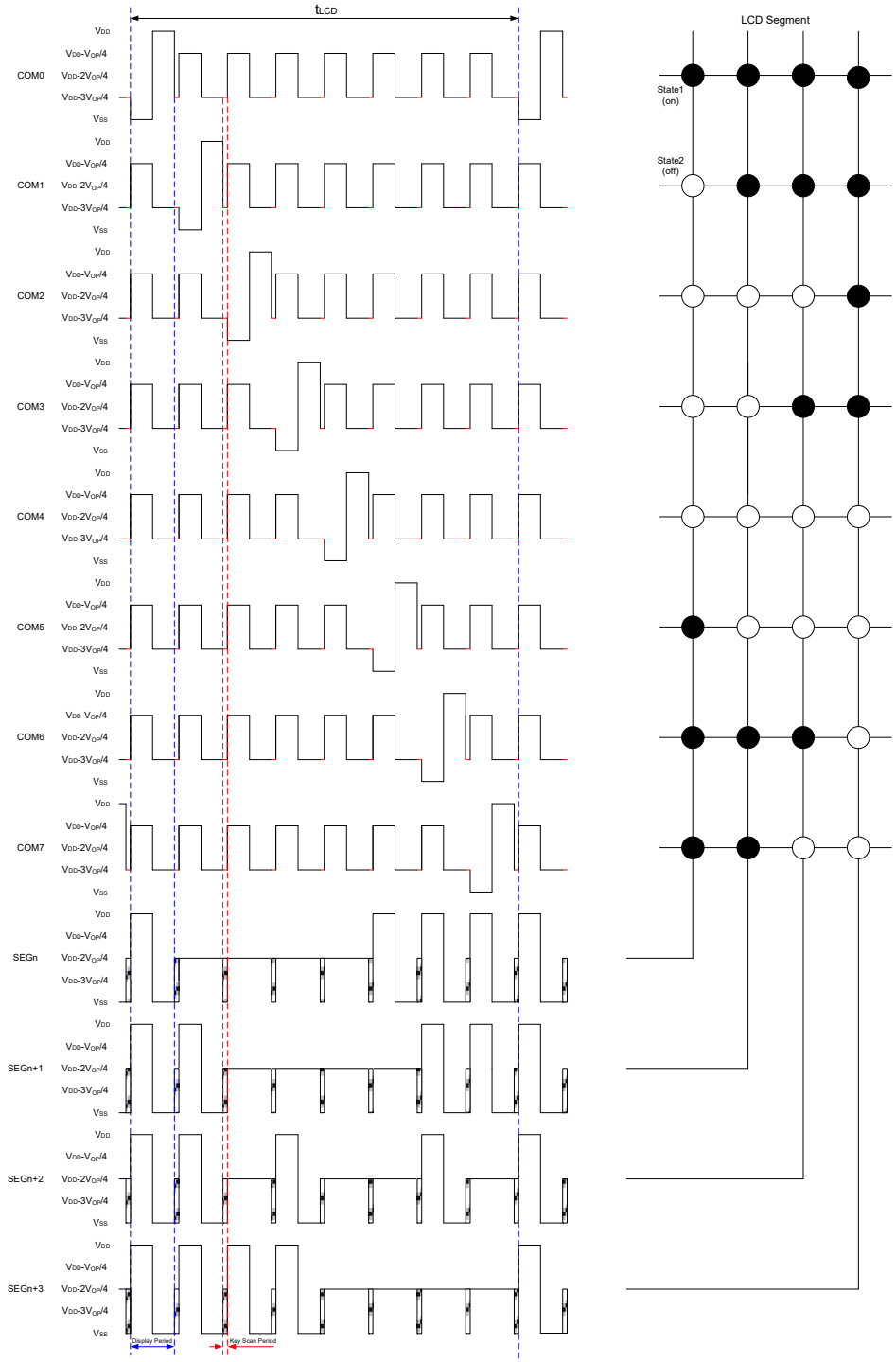
- When the LCD drive mode is selected as 1/6 duty and 1/3 bias, the waveform and LCD display are shown as follows.



Waveforms for 1/6 Duty Drive Mode with 1/3 Bias (V_{OP}=V_{DD}-V_{SS})

Note: 1. t_{LCD}=1/ f_{LCD}.
2. The display period is about 2.281ms (73 clock cycles) without key scan period.
3. The key scan period is about 31.25μs (1 clock cycle) @ KP[2:0]=000b.

- When the LCD drive mode is selected as 1/8 duty and 1/4 bias, the waveform and LCD display are shown as follows.



Waveforms for 1/8 Duty Drive Mode with 1/4 Bias (V_{OP}=V_{DD}-V_{SS})

Note: 1. t_{LCD}=1/ f_{LCD}.
2. The display period is about 1.719ms (55 clock cycles) without key scan period.
3. The key scan period is about 31.25μs (1 clock cycle) @ KP[2:0]=000b.

Tone Output

A simple tone generator is implemented in the HT16K24. The tone generator can output a pair of differential driving signals on the BZ and $\overline{BZ}$, which are used to generate a single tone. By executing the Buzzer frequency command there are four selectable tone frequency outputs. The Buzzer frequency command can set the tone frequency to 1kHz, 2kHz, 4kHz and 8kHz, respectively. The tone output can be turned on or off by invoking the BZEN bit. The tone outputs, namely BZ and $\overline{BZ}$, are a pair of differential driving outputs used to drive a piezoelectric buzzer. Once the tone output is inhibited, the BZ and the $\overline{BZ}$ outputs will remain at a low level.

LED Function

The HT16K24 supports 8 LED output ports. These ports are CMOS output structure. Use the write LED data command to write data to the LED port. Users use internal CMOS devices to directly drive LED components. When a bit of the port is set to 1, the corresponding LED is on. When the bit is cleared to 0, the LED is off.

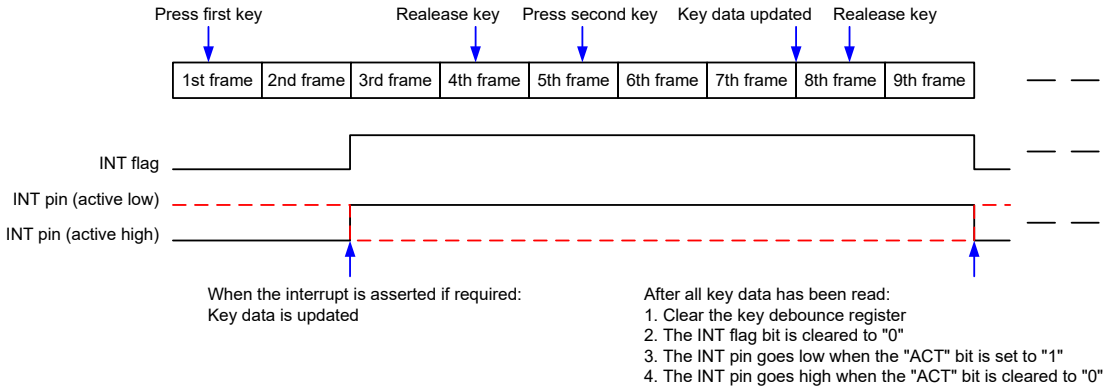
Key Scan

- The HT16K24 supports a 24×1 matrix key scan in the 24×4 display mode, a 22×1 matrix key scan in the 22×6 display mode and a 20×1 matrix key scan in the 20×8 display mode.
- The hardware interrupt function is optional, allowing SEG19/COM4/K19/INT in the 24×4 display mode or SEG17/COM6/K17/INT in the 22×6 display mode or SEG15/K15/INT in the 20×8 display mode to be used as an INT output or as a segment driver. The interrupt flag can be read (polled) through the serial interface instead.
- The key scan input pins are shared with segment output pins.
- The key scan cycle loops continuously with time, with all keys experiencing a full key scan debounce of over 20ms. A key press is debounced and an interrupt issued if at least one key that was not pressed in a previous cycle is found pressed during both sampling periods.
- The INT output is active-low when the “ACT” bit of the driver mode setting command is set to “0”.
- The INT output is active-high when the “ACT” bit of the driver mode setting command is set to “1”.

INT Timing

- The key data is updated and the INT function is changed if the key has been pressed for 2 frame cycles.
- The INT function is changed when the first key has been pressed.
- After the key data has been read, the key data registers are cleared to “0” and the INT flag bit is cleared to “0”. The INT pin goes low when the “ACT” bit of the driver mode setting command is set to “1”.
- After the key data has been read, the key data registers are cleared to “0” and the INT flag bit is cleared to “0”. The INT pin goes high when the “ACT” bit of the driver mode setting command is cleared to “0”.
- The INT flag register is shown below. To clear the INT flag status, the key data register must be read from 0x20H~0x22H in one operation.

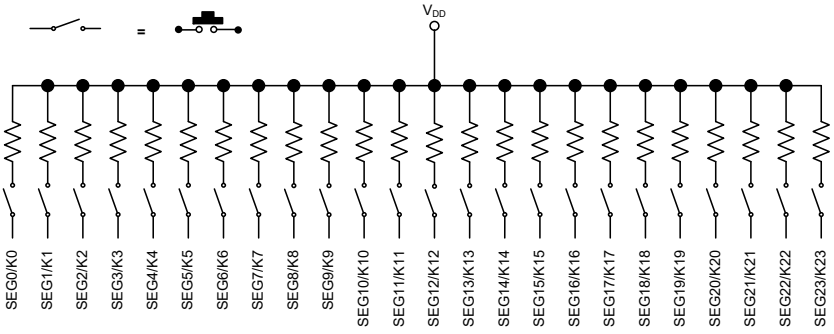
INT Flag Register	Address Code	R/W	Register Data								
			D7	D6	D5	D4	D3	D2	D1	D0	Def.
INT flag register	0x30H	R	0	0	0	0	0	0	0	INT flag	00H



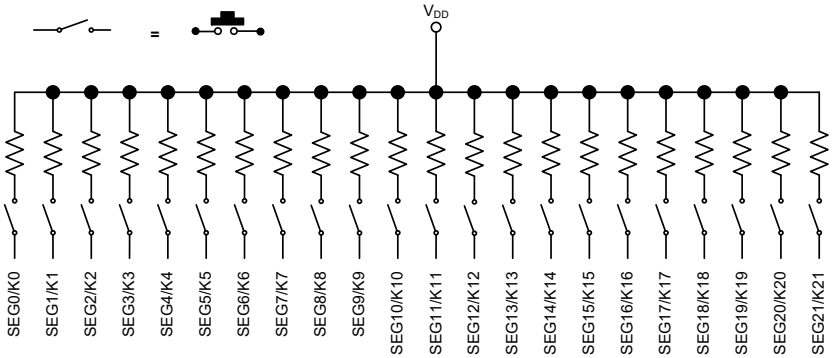
Key Matrix Configuration

There is a key scan circuit integral to the HT16K24 which can detect a key press. It includes twenty-four inputs (K0 to K23, shared with SEG0 to SEG23) in the 24×4 display mode, twenty-two inputs (K0 to K21, shared with SEG0 to SEG21) in 22×6 display mode or twenty inputs (K0 to K19, shared with SEG0 to SEG19) in 20×8 display mode.

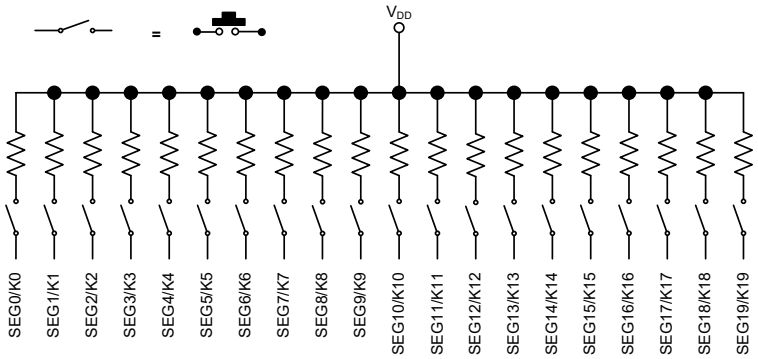
The key matrix has a 24×1 matrix in the 24×4 display mode, a 22×1 matrix in the 22×6 display or a 20×1 matrix in the 20×8 display configuration as shown below.



24×1 Matrix in 24×4 Display Mode



22×1 Matrix in 22×6 Display Mode



20×1 Matrix in 20×8 Display Mode

Key Data Register

After the key data registers have been read, the key data registers are cleared to "0", to enable future key presses to be identified. If the key data register is not read, the key data accumulates. There is no FIFO register in the HT16K24. The key-press order, or whether a key has been pressed more than once, cannot be determined unless all of the key data RAM is read after each interrupt and before completion of the next key scan cycle.

After the key data registers have been read, the INT output and INT flag status are cleared. If a key is pressed and held down, the key is reported as being debounced (and an INT is issued) only once. The key must be detected as released by the key scan circuit before it is debounced again.

It is strongly recommended to read the key data registers from the address 0x20H only. The key data registers of addresses from 0x20H to 0x22H should be read continuously and completed in one operation.

There is a one-to-one correspondence between the key data register addresses and the key data outputs and between the individual bits of a key data register word and the key data outputs. The following table shows the mapping from the RAM to the key data output:

The key data registers are read only. The key data register format is shown below:

Key Data Register	Address Code	R/W	Register Data								
			D7	D6	D5	D4	D3	D2	D1	D0	Def.
Key data registers	0x20H	R	K7	K6	K5	K4	K3	K2	K1	K0	00H
	0x21H	R	K15	K14	K13	K12	K11	K10	K9	K8	00H
	0x22H	R	K23	K22	K21	K20	K19	K18	K17	K16	00H

Key Scan Period Setting Command

Due to various LCD characteristic, it will have different RC time constant in key scan period. If the equivalent capacitance is larger in the LCD, it cannot be charged or discharged fully in key scan period. The key cannot be read correctly. To avoid read key error, users can adjust the key scan period through this command. If key scan period is too longer, it may affect the LCD visual quality.

The key scan period can be adjusted through this command. In generally, users do not need to use this command, when key data can be read correctly.

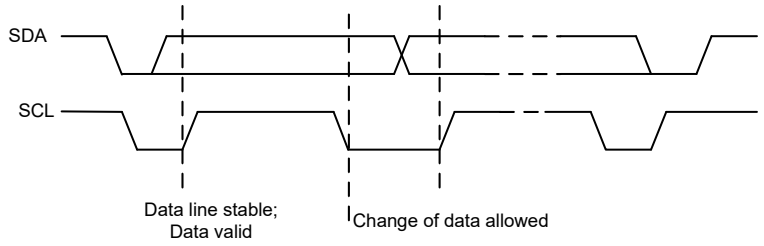
The default value of key scan period is 2 clock cycle time in 24×4 display mode, 1 clock cycle time in 22×6 display mode and 20×8 display mode.

I²C Serial Interface

The device includes an I²C serial interface. The I²C bus is used for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines are connected to a positive supply via a pull-up resistor. When the bus is free, both lines are high. The output stages of devices connected to the bus must have an open-drain or open-collector output type to implement the required wired-and function. Data transfer is initiated only when the bus is not busy.

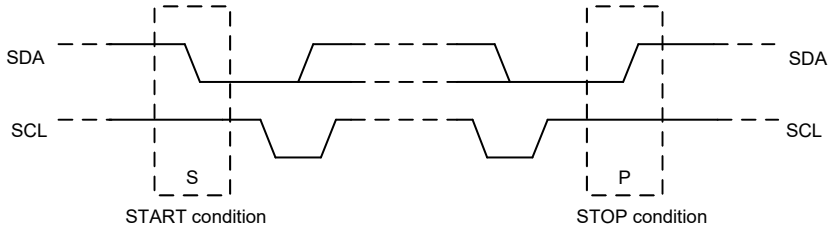
Data Validity

The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low as shown below.



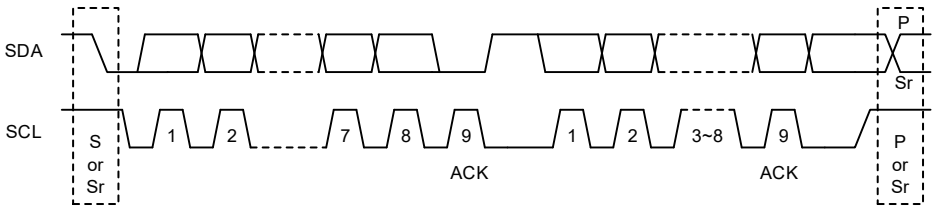
START and STOP Conditions

- A high to low transition on the SDA line while SCL is high defines a START condition.
- A low to high transition on the SDA line while SCL is high defines a STOP condition.
- START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.
- The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. In this respect, the START (S) and repeated START (Sr) conditions are functionally identical.



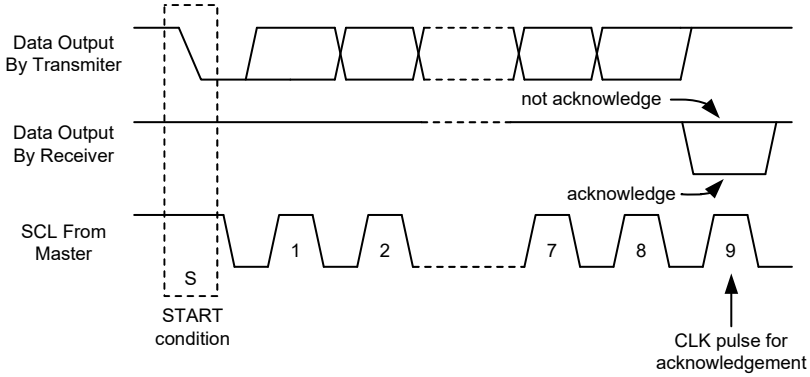
Byte Format

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first.



Acknowledge

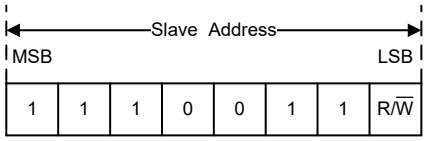
- Each byte of eight bits is followed by a single acknowledge bit. This acknowledge bit is a low level which is placed on the bus by the receiver. The master generates an extra acknowledge related clock pulse.
- A slave receiver which is addressed must generate an acknowledge (ACK) after the reception of each byte.
- The device that provides an acknowledge must pull down the SDA line during the acknowledge clock pulse so that it remains at a stable low level during the high period of this clock pulse.
- A master receiver must signal an end of data status to the slave by generating a not-acknowledge (NACK) bit on the last byte that has been clocked out of the slave. In this case, the master receiver must leave the data line high during the 9th pulse to not acknowledge. The master will generate a STOP or repeated START condition.



Device Addressing

The slave address byte is the first byte received following a START condition from the master device. The first seven bits of the first byte make up the slave address. The eighth bit defines whether a read or write operation is to be performed. When this R/$\overline{W}$ bit is "1", then a read operation is selected. A "0" selects a write operation.

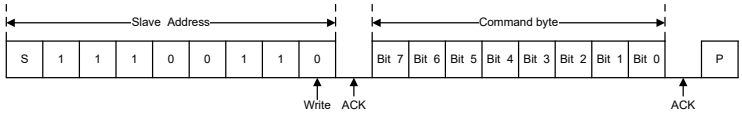
The HT16K24 address bits are "1110011" as shown below. When an address byte is sent, the device compares the first seven bits after the START condition. If they match, the device outputs an acknowledge on the SDA line.



Write Operation

Command Byte Write Operation

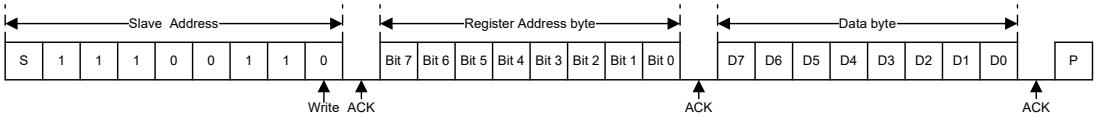
A command byte write operation requires a START condition, a slave address with an R/$\overline{W}$ bit, a command byte and a STOP condition.



Command Byte Write Operation

Display RAM Single Data Byte Write Operation

A display RAM data byte write operation requires a START condition, a slave address with an R/$\overline{W}$ bit, a valid Register Address byte, a Data byte and a STOP condition.

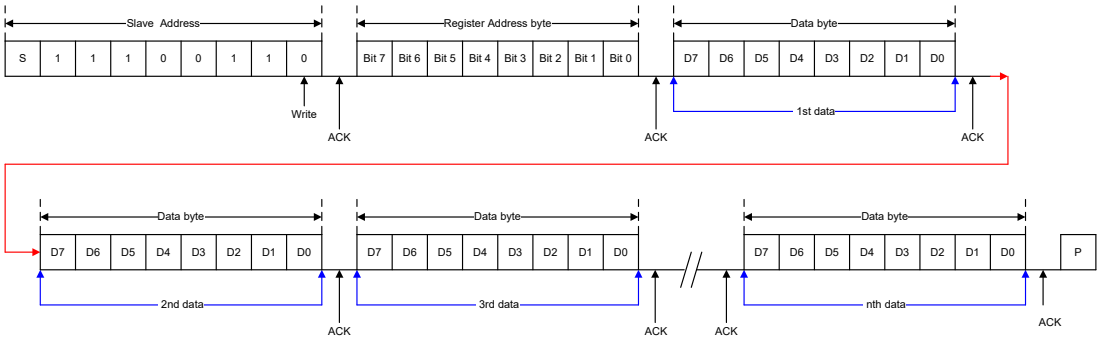


Display RAM Single Data Byte Write Operation

Note: If the byte followed by the slave address is a command code, the bytes followed by the command code will be ignored.

Display RAM Page Write Operation

A START condition and a slave address with an R/$\overline{W}$ bit placed on the bus indicates to the addressed device that a Register Address will follow and is to be written to the internal address pointer. The data to be written to the memory will be transmitted next and then the internal address pointer will be incremented by 1 to indicate the next memory address location after the reception of an acknowledge clock pulse.



N Bytes Display RAM Data Write Operation

If memory location exceeds the limit value, the memory pointer will return to 00H. The limit value of Memory location is shown below:

Display Mode	Memory Location Limit Value
24×4	0Bh
22×6	15h
20×8	13h

Read Operation

Display RAM Page Read Operation

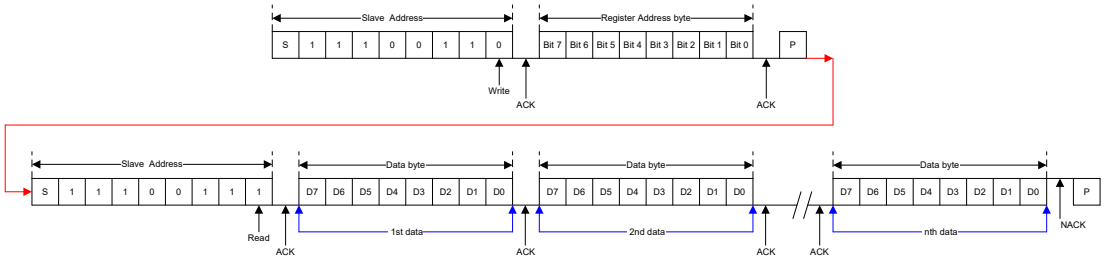
In this mode, the master reads the device data after setting the slave address. Following the R/$\overline{W}$ bit (="0") is an acknowledge bit and the register address byte which is written to the internal address pointer. After the start address of the Read Operation has been configured, another START condition and the slave address transferred on the bus followed by the R/$\overline{W}$ bit (="1"). Then the MSB of the data which was addressed is transmitted first on the I^2C bus. The address pointer is only incremented by 1 after the reception of an acknowledge clock. That means that if the device is configured to transmit the data at the address of An+1, the master will read and acknowledge the transferred new data byte and the address pointer is incremented to An+2.

If memory location exceeds the limit value, the memory pointer will return to 00H. The limit value of Memory location is shown below:

Display Mode	Memory Location Limit Value
24×4	0Bh
22×6	15h
20×8	13h

The read key data register address point range is 20h ~ 22h, after reaching the memory location 22H, the pointer will reset to 20h.

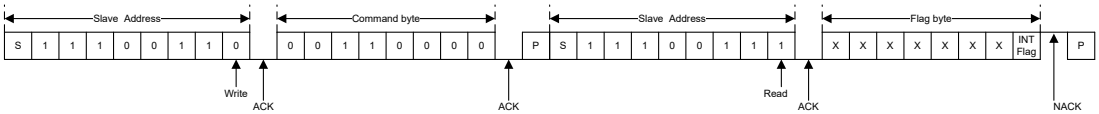
This cycle of reading consecutive addresses will continue until the master sends a STOP condition.



Note: This cycle for reading consecutive addresses will continue until the master sends a NACK and STOP condition.

INT Flag Read Operation

In this mode, the master reads the device data after setting the slave address. Following the R/$\overline{W}$ bit, which is zero, and the acknowledge bit, and then follows the read INT flag command byte and a STOP condition. Next is the START condition and slave address, followed by an R/$\overline{W}$ bit which is high. The data which was addressed is then transmitted. The Read INT Flag status format is as follows:



Note: This cycle for reading consecutive addresses will continue until the master sends a NACK and STOP condition.

Command Summary

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.	Description
Display RAM Read/Write Command											
Display Data Read/Write	W	0	0	0	A4	A3	A2	A1	A0	00h	Read/Write display RAM address command
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	—	Read/Write display data
Key Data Read Command											
Key Data Read	W	0	0	1	0	0	0	K1	K0	20h	Read key data address command
	R	D7	D6	D5	D4	D3	D2	D1	D0	—	Read key data
Key Flag and Register Read Command											
INT Flag and Register	W	0	0	1	1	0	0	0	0	30h	INT flag and register address point setting
	R	—	—	—	—	—	—	—	INT Flag	—	Read INT flag and register status
LED Current Set Command											
LED Current 1	W	0	1	0	0	LC11	LC10	LC01	LC00	40h	4-level LED output current adjustment LC0[1:0]: For LED0 pin LC1[1:0]: For LED1 pin

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.	Description
LED Current 2	W	0	1	0	1	LC31	LC30	LC21	LC20	50h	4-level LED output current adjustment LC2[1:0]: For LED2 pin LC3[1:0]: For LED3 pin
LED Current 3	W	0	1	1	0	LC51	LC50	LC41	LC40	60h	4-level LED output current adjustment LC4[1:0]: For LED4 pin LC5[1:0]: For LED5 pin
LED Current 4	W	0	1	1	1	LC71	LC70	LC61	LC60	70h	4-level LED output current adjustment LC6[1:0]: For LED6 pin LC7[1:0]: For LED7 pin
Function Command											
System Mode	W	1	0	0	0	0	0	D	S	80h	S bit: Standby mode selection {0}: Standby mode (system oscillator off) {1}: Normal mode (system oscillator on) D bit: Display on/off control {0}: LCD display off {1}: LCD display on
Configure SEG/LED Shared Pin Mode 1	W	1	0	0	1	SL3	SL2	SL1	SL0	90h	SL[3:0]: Segment or LED3~LED0 shared pin selection {0}: Segment output {1}: LED output
Driver Mode Setting	W	1	0	1	0	M1	ACT	INT/ ROW	M0	A0h	M[1:0]: LCD display mode selection {0,0}: 24×4 display mode {0,1}: 20×8 display mode {1,x}: 22×6 display mode INT/ROW: Segment or INT pin selection {0}: Segment output {1}: INT output ACT: INT output level selection {0}: INT output is active-low {1}: INT output is active-high
Configure SEG/LED Shared Pin Mode 2	W	1	0	1	1	SL7	SL6	SL5	SL4	B0H	[SL7:SL4]: Segment or LED7~LED4 shared pin selection {0}: Segment output {1}: LED output
Write LED0~LED3 Data	W	1	1	0	0	LD3	LD2	LD1	LD0	C0h	Write data to LED0~LED3 {0}: LED off {1}: LED on
Write LED4~LED7 Data	W	1	1	0	1	LD7	LD6	LD5	LD4	D0h	Write data to LED4~LED7 {0}: LED off {1}: LED on
Buzzer Frequency	W	1	1	1	0	0	BZEN	BF1	BF0	E0h	BZEN: Buzzer function on/off control {0}: Off {1}: On BF[1:0]: Buzzer frequency setting {0,0}: 1kHz {0,1}: 2kHz {1,0}: 4kHz {1,1}: 8kHz
Configure SEG/Buzzer Shared Pin	W	1	1	1	0	1	0	SB1	SB0	E8h	SB1: Segment or BZ pin selection {0}: Segment output {1}: BZ output SB0: Segment or $\overline{BZ}$ pin selection {0}: Segment output {1}: $\overline{BZ}$ output
Bias Resistor	W	1	1	1	0	1	1	BR1	BR0	EEh	BR[1:0]: Resistor divider setting for LCD bias circuit {0,0}: 2kΩ {0,1}: 4kΩ {1,0}: 8kΩ {1,1}: 16kΩ

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.	Description
Key Scan Period	W	1	1	1	1	1	KP2	KP1	KP0	F8h	KP[2:0]: Key period setting 24×4 display mode: {0,0,0}: 2 clock cycle time {0,0,1}: 4 clock cycle time {0,1:0}: 6 clock cycle time {0,1,1}: 8 clock cycle time {1,0,0}: 10 clock cycle time {1,0,1}: 12 clock cycle time {1,1:0}: 14 clock cycle time {1,1,1}: 16 clock cycle time 22×6 / 20×8 display mode: {0,0,0}:1 clock cycle time {0,0,1}:3 clock cycle time {0,1:0}:5 clock cycle time {0,1,1}:7 clock cycle time {1,0,0}:9 clock cycle time {1,0,1}:11 clock cycle time {1,1:0}:13 clock cycle time {1,1,1}:15 clock cycle time

Note: 1. x: Don't care.
2. Def.: Power on reset default.
3. If the programmed command is not defined, the function will not be affected.

Command Description

Display Data Read/Write Command

This command can write display data from an MCU to the device memory map or can read from the device.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Display data Read/Write	W	0	0	0	A4	A3	A2	A1	A0	00h
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	—

Note: 1. Power on status: The address is set to 00H.
2. If the programmed command is not defined, the function will not be affected.
3. For 24×4 display mode after reaching the memory location 0BH, the pointer will reset to 00H.
4. For 22×6 display mode after reaching the memory location 15H, the pointer will reset to 00H.
5. For 20×8 display mode after reaching the memory location 13H, the pointer will reset to 00H.

Key Data Read Command

This command can read key data from the device.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Key data Read	W	0	0	1	0	0	0	K1	K0	20h
	R	D7	D6	D5	D4	D3	D2	D1	D0	—

The following table is a mapping from the RAM to the key data output:

Bit		Key Data									Note
K1	K0	D7	D6	D5	D4	D3	D2	D1	D0	Def.	
0	0	K7	K6	K5	K4	K3	K2	K1	K0	00h	Default value
0	1	K15	K14	K13	K12	K11	K10	K9	K8	00h	—
1	x	K23	K22	K21	K20	K19	K18	K17	K16	00h	—

Note: 1. Power on status: The address is set to 20H.

2. If the programmed command is not defined, the function will not be affected.
3. It is strongly recommended that read the key data registers from address 0x20H only. The key data registers of address from 0x20H to 0x22H should be read continuously and complete in one time.
4. After the key data registers have been read, the key data registers are cleared to "0".

INT Flag and Register Read Command

This command can read the INT flag and the device register status.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
INT Flag and Register Read	W	0	0	1	1	0	0	0	0	30h
	R	—	—	—	—	—	—	—	INT Flag	—

Note: 1. Power on status: The address is set to 30H.

2. If the programmed command is not defined, the function will not be affected.

LED Current Set Command

This command can set four levels of the source/sink current driving capability for each LED port.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
LED Current 1	W	0	1	0	0	LC11	LC10	LC01	LC00	40h
LED Current 2	W	0	1	0	1	LC31	LC30	LC21	LC20	50h
LED Current 3	W	0	1	1	0	LC51	LC50	LC41	LC40	60h
LED Current 4	W	0	1	1	1	LC71	LC70	LC61	LC60	70h

Bit		LED0~LED7 Source/Sink Current Selection	Note
LCn1	LCn0		
0	0	Source/Sink current = Level 0 (min.)	Default value
0	1	Source/Sink current = Level 1	—
1	0	Source/Sink current = Level 2	—
1	1	Source/Sink current = Level 3 (max.)	—

Note: 1. n: 0~7, corresponding to LED0~LED7

2. Refer to D.C. Characteristics for the detailed LED current value.
3. Power on status: The Source/Sink current Level0 is selected.
4. If the programmed command is not defined, the function will not be affected.

System Mode Command

This command controls the internal system oscillator on/off and display on/off.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
System Mode	W	1	0	0	0	0	0	D	S	80h

Bit		LCD Display	Internal System Oscillator	Note
D	S			
0	0	Off	Off	Standby mode Default value
0	1	Off	On	Display off Enable Internal System oscillator
1	0	Off	Off	Standby mode
1	1	On	On	Normal mode

Note: 1. Power on status: Display off and disable Internal System oscillator

2. If the programmed command is not defined, the function will not be affected.

Configure SEG/LED Shared Pin Mode Command

This command controls the SEG/LED shared pin selection.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Configure SEG/LED shared pin mode 1	W	1	0	0	1	SL3	SL2	SL1	SL0	90h
Configure SEG/LED shared pin mode 2	W	1	0	1	1	SL7	SL6	SL5	SL4	B0h

Bit				Shared Pin Mode 1				Note
SL3	SL2	SL1	SL0	SEG23/LED0	SEG22/LED1	SEG21/LED2	SEG20/LED3	
0	0	0	0	SEG23	SEG22	SEG21	SEG20	Default value
0	0	0	1	SEG23	SEG22	SEG21	LED3	—
0	0	1	0	SEG23	SEG22	LED2	SEG20	—
0	0	1	1	SEG23	SEG22	LED2	LED3	—
0	1	0	0	SEG23	LED1	SEG21	SEG20	—
0	1	0	1	SEG23	LED1	SEG21	LED3	—
0	1	1	0	SEG23	LED1	LED2	SEG20	—
0	1	1	1	SEG23	LED1	LED2	LED3	—
1	0	0	0	LED0	SEG22	SEG21	SEG20	—
1	0	0	1	LED0	SEG22	SEG21	LED3	—
1	0	1	0	LED0	SEG22	LED2	SEG20	—
1	0	1	1	LED0	SEG22	LED2	LED3	—
1	1	0	0	LED0	LED1	SEG21	SEG20	—
1	1	0	1	LED0	LED1	SEG21	LED3	—
1	1	1	0	LED0	LED1	LED2	SEG20	—
1	1	1	1	LED0	LED1	LED2	LED3	—

Bit				Shared Pin Mode 2				Note
SL7	SL6	SL5	SL4	SEG14/LED4	SEG13/LED5	SEG12/LED6	SEG11/LED7	
0	0	0	0	SEG14	SEG13	SEG12	SEG11	Default value
0	0	0	1	SEG14	SEG13	SEG12	LED7	—
0	0	1	0	SEG14	SEG13	LED6	SEG11	—
0	0	1	1	SEG14	SEG13	LED6	LED7	—
0	1	0	0	SEG14	LED5	SEG12	SEG11	—
0	1	0	1	SEG14	LED5	SEG12	LED7	—
0	1	1	0	SEG14	LED5	LED6	SEG11	—
0	1	1	1	SEG14	LED5	LED6	LED7	—
1	0	0	0	LED4	SEG13	SEG12	SEG11	—
1	0	0	1	LED4	SEG13	SEG12	LED7	—
1	0	1	0	LED4	SEG13	LED6	SEG11	—
1	0	1	1	LED4	SEG13	LED6	LED7	—
1	1	0	0	LED4	LED5	SEG12	SEG11	—
1	1	0	1	LED4	LED5	SEG12	LED7	—
1	1	1	0	LED4	LED5	LED6	SEG11	—
1	1	1	1	LED4	LED5	LED6	LED7	—

Note: 1. Power on status: The Segment/LED shared pin is set to segment pin.
2. If the programmed command is not defined, the function will not be affected.

Driver Mode Command

This command controls the display mode, INT/SEG shared pin selection and INT output active-level setting.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Driver Mode	W	1	0	1	0	M1	ACT	INT/ ROW	M0	A0h

Bit		Display Mode	Duty	Bias	Note
M1	M0				
0	0	24×4	1/4	1/3	Default value
0	1	20×8	1/8	1/4	—
1	x	22×6	1/6	1/3	—

Bit		Display Mode	Shared Pin		INT Output Active-Level	Note
ACT	INT/ROW		SEG19/COM4/K19/INT	SEG15/K15/INT		
0	0	24×4	SEG19/K19	SEG15/K15	—	Default value
0	1		INT	SEG15/K15	Low	—
1	0		SEG19/K19	SEG15/K15	—	—
1	1		INT	SEG15/K15	High	—
0	0	22×6	COM4	SEG15/K15	—	—
0	1		COM4	INT	Low	—
1	0		COM4	SEG15/K15	—	—
1	1		COM4	INT	High	—
0	0	20×8	COM4	SEG15/K15	—	—
0	1		COM4	INT	Low	—
1	0		COM4	SEG15/K15	—	—
1	1		COM4	INT	High	—

Note: 1. Power on status: The Segment/INT shared pin is set to segment pin and 24×4 display mode is selected.
2. If the programmed command is not defined, the function will not be affected.

Write LED Data Command

This command is used to write data to LED device. A logic "1" in the register indicates the "on" state of the corresponding LED; similarly, a logic 0 indicates the "off" state.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Write LED0~LED3 Data	W	1	1	0	0	LD3	LD2	LD1	LD0	C0h
Write LED4~LED7 Data	W	1	1	0	1	LD7	LD6	LD5	LD4	D0h

Bit				LED Data 0~3				Note
LD3	LD2	LD1	LD0	LED3	LED2	LED1	LED0	
0	0	0	0	Off	Off	Off	Off	Default value
0	0	0	1	Off	Off	Off	On	—
0	0	1	0	Off	Off	On	Off	—
0	0	1	1	Off	Off	On	On	—
0	1	0	0	Off	On	Off	Off	—
0	1	0	1	Off	On	Off	On	—
0	1	1	0	Off	On	On	Off	—
0	1	1	1	Off	On	On	On	—
1	0	0	0	On	Off	Off	Off	—
1	0	0	1	On	Off	Off	On	—
1	0	1	0	On	Off	On	Off	—
1	0	1	1	On	Off	On	On	—
1	1	0	0	On	On	Off	Off	—
1	1	0	1	On	On	Off	On	—
1	1	1	0	On	On	On	Off	—
1	1	1	1	On	On	On	On	—

Bit				LED Data 4~7				Note
LD7	LD6	LD5	LD4	LED7	LED6	LED5	LED4	
0	0	0	0	Off	Off	Off	Off	Default value
0	0	0	1	Off	Off	Off	On	—
0	0	1	0	Off	Off	On	Off	—
0	0	1	1	Off	Off	On	On	—
0	1	0	0	Off	On	Off	Off	—
0	1	0	1	Off	On	Off	On	—
0	1	1	0	Off	On	On	Off	—
0	1	1	1	Off	On	On	On	—
1	0	0	0	On	Off	Off	Off	—
1	0	0	1	On	Off	Off	On	—
1	0	1	0	On	Off	On	Off	—
1	0	1	1	On	Off	On	On	—
1	1	0	0	On	On	Off	Off	—
1	1	0	1	On	On	Off	On	—
1	1	1	0	On	On	On	Off	—
1	1	1	1	On	On	On	On	—

Note: 1. Power on status: The LED output off.

2. If the programmed command is not defined, the function will not be affected.
3. When the LED is off, the LED pin outputs low. When the LED is on, the LED pin outputs high.

Buzzer Frequency Setting Command

This command controls the buzzer frequency and the buzzer on/off.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Buzzer (tone) frequency	W	1	1	1	0	0	BZEN	BF1	BF0	E0h

Bit	Buzzer	Note
BZEN		
0	Off	Default value
1	On	—

Bit		Buzzer Frequency	Note
BF1	BF0		
0	0	1kHz	Default value
0	1	2kHz	—
1	0	4kHz	—
1	1	8kHz	—

Note: 1. Power on status: The buzzer device is off.

2. If the programmed command is not defined, the function will not be affected.

Configure SEG/Buzzer Shared Pin Mode Command

This command controls the SEG/Buzzer shared pin selection.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Configure SEG / Buzzer shared pin	W	1	1	1	0	1	0	SB1	SB0	E8h

Bit		Shared Pin		Note
SB1	SB0	SEG10/K10/BZ	SEG9/K9/$\overline{BZ}$	
0	0	SEG10/K10	SEG9/K9	Default value
0	1	SEG10/K10	$\overline{BZ}$	—
1	0	BZ	SEG9/K9	—
1	1	BZ	$\overline{BZ}$	—

Note: 1. Power on status: The Segment/BZ and Segment/$\overline{BZ}$ shared pin are set to segment pin.

2. If the programmed command is not defined, the function will not be affected.

Bias Resistor Setting Command

This command sets the four-level resistance selection for the bias circuit.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Bias Resistor	W	1	1	1	0	1	1	BR1	BR0	EEh

Bit		Resistor Value of Each Section	Total Bias Resistor Selection		Note
BR1	BR0		1/3 Bias	1/4 Bias	
0	0	2kΩ	6kΩ	8kΩ	—
0	1	4kΩ	12kΩ	16kΩ	—
1	0	8kΩ	24kΩ	32kΩ	Default value
1	1	16kΩ	48kΩ	64kΩ	—

Note: 1. Power on status: The 8kΩ resistance of each section is selected.

2. If the programmed command is not defined, the function will not be affected.

Key Scan Period Command

This command selects the frame frequency.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Key Scan Period	W	1	1	1	1	1	KP2	KP1	KP0	F8h

Bit			Display Mode			Note
KP2	KP1	KP0	24×4	22×6	20×8	
0	0	0	2 clock cycle time	1 clock cycle time	1 clock cycle time	Default value
0	0	1	4 clock cycle time	3 clock cycle time	3 clock cycle time	—
0	1	0	6 clock cycle time	5 clock cycle time	5 clock cycle time	—
0	1	1	8 clock cycle time	7 clock cycle time	7 clock cycle time	—
1	0	0	10 clock cycle time	9 clock cycle time	9 clock cycle time	—
1	0	1	12 clock cycle time	11 clock cycle time	11 clock cycle time	—
1	1	0	14 clock cycle time	13 clock cycle time	13 clock cycle time	—
1	1	1	16 clock cycle time	15 clock cycle time	15 clock cycle time	—

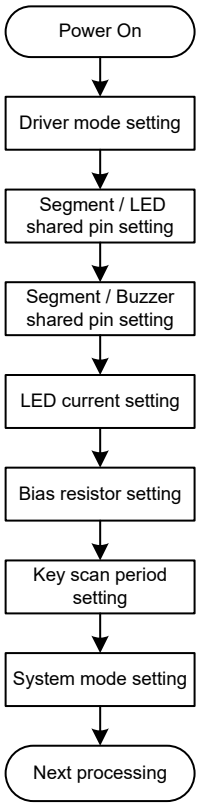
Note: 1. Power on status: 2 clock cycle time for 24×4 Display mode

2. If the programmed command is not defined, the function will not be affected.

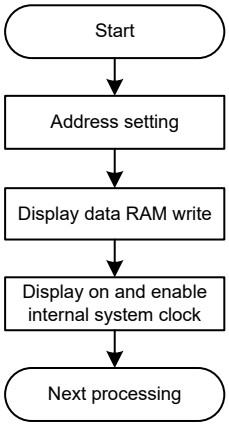
Operation FlowChart

The access procedure is illustrated using the following flowcharts.

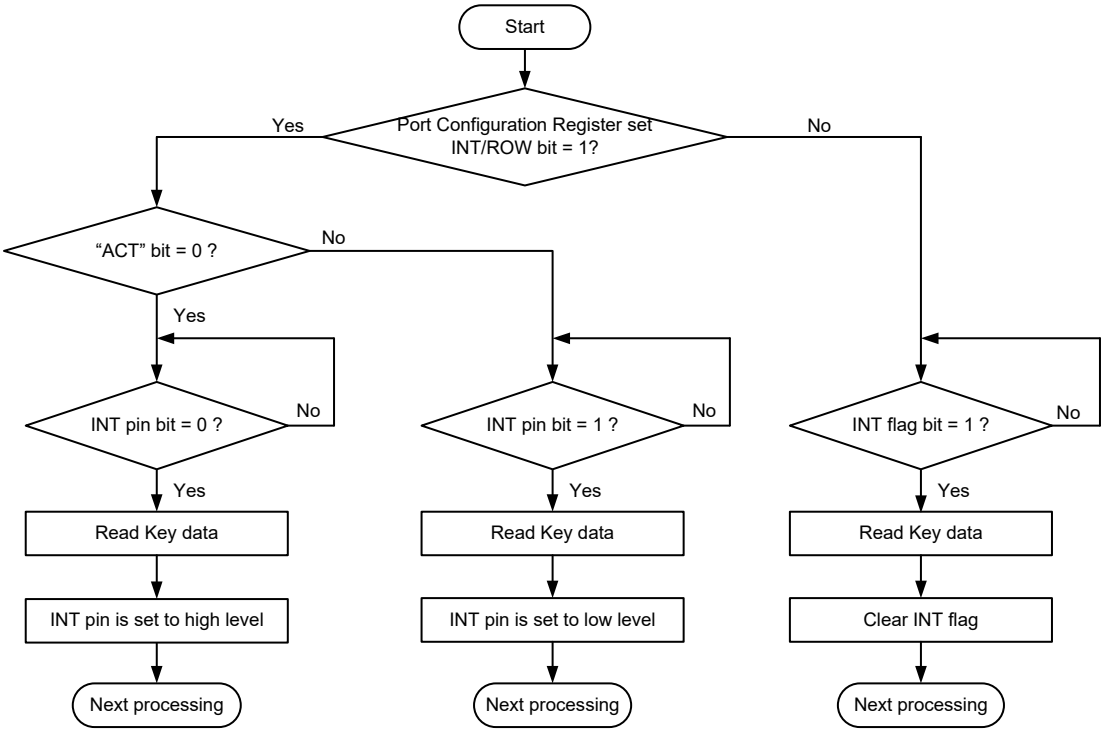
- Initialisation



- Display Data Write – Address Setting



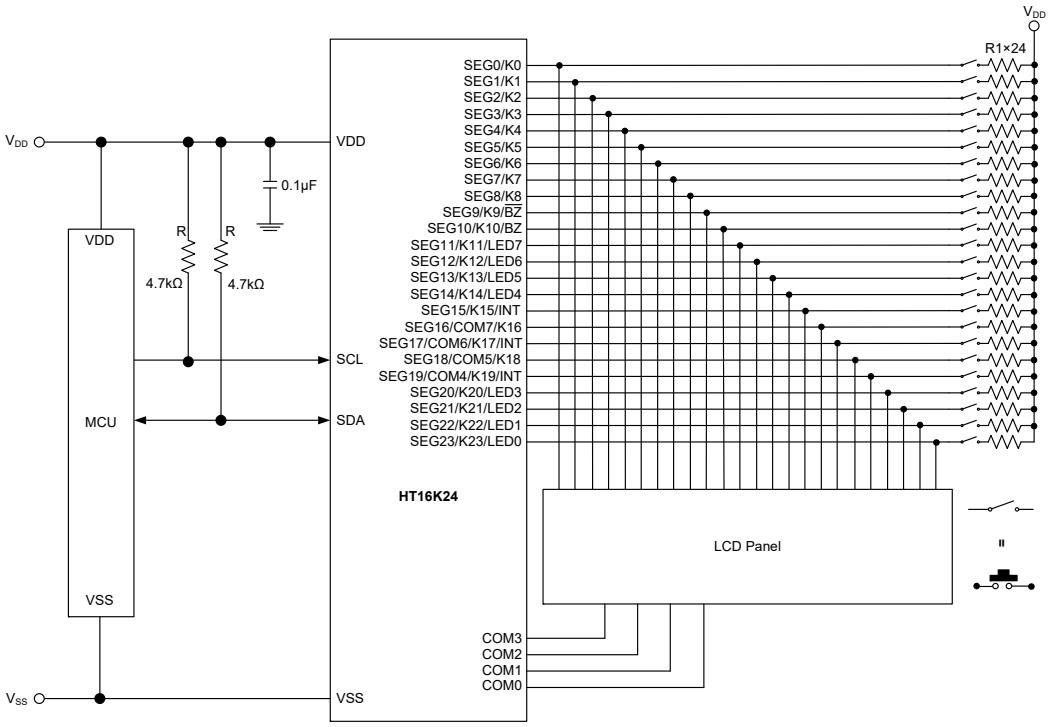
- Key Data Read



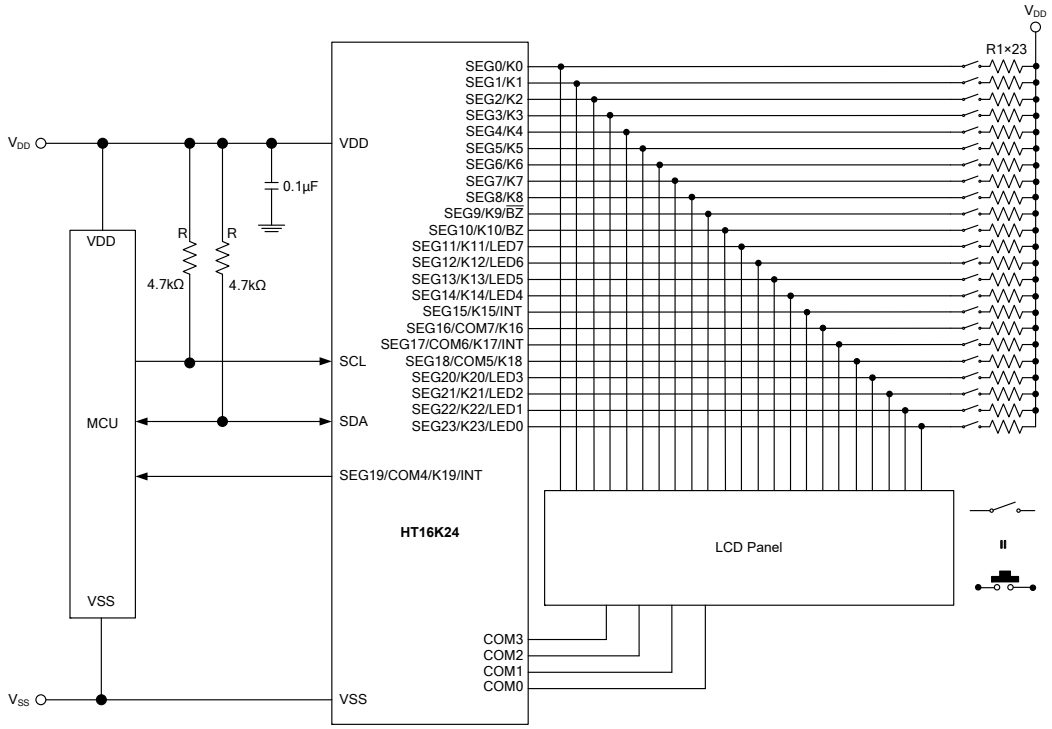
Application Circuit

24×4 Display Mode

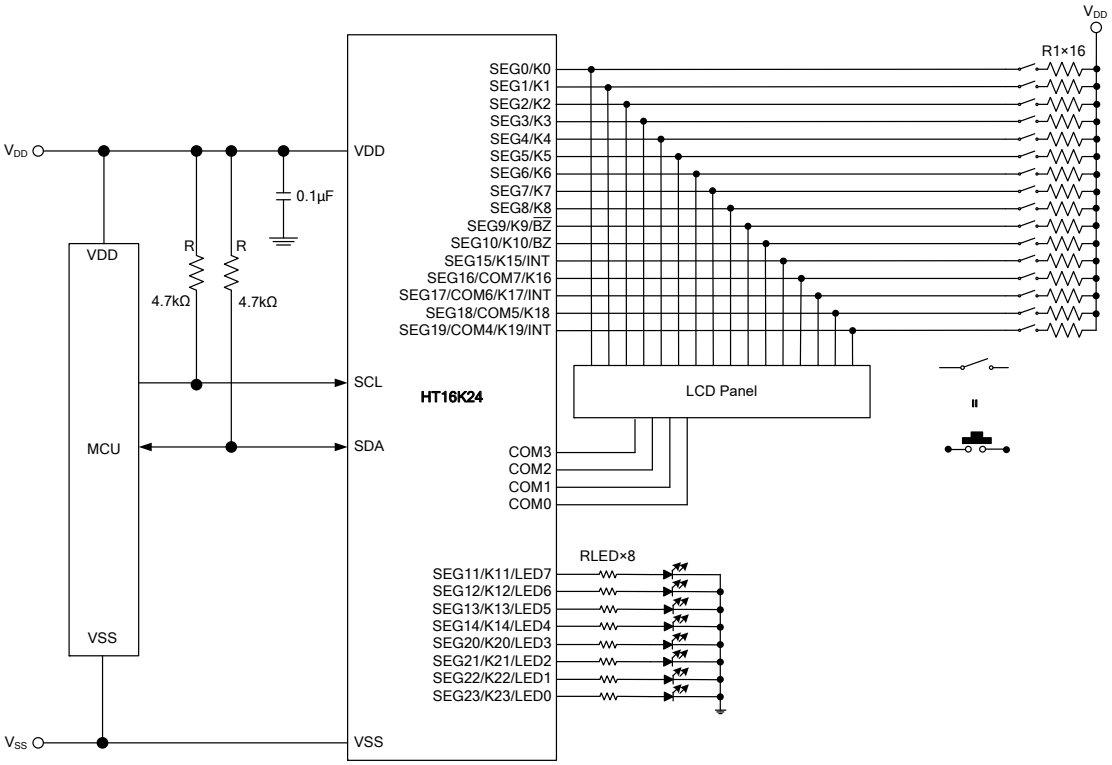
- Display Mode without INT



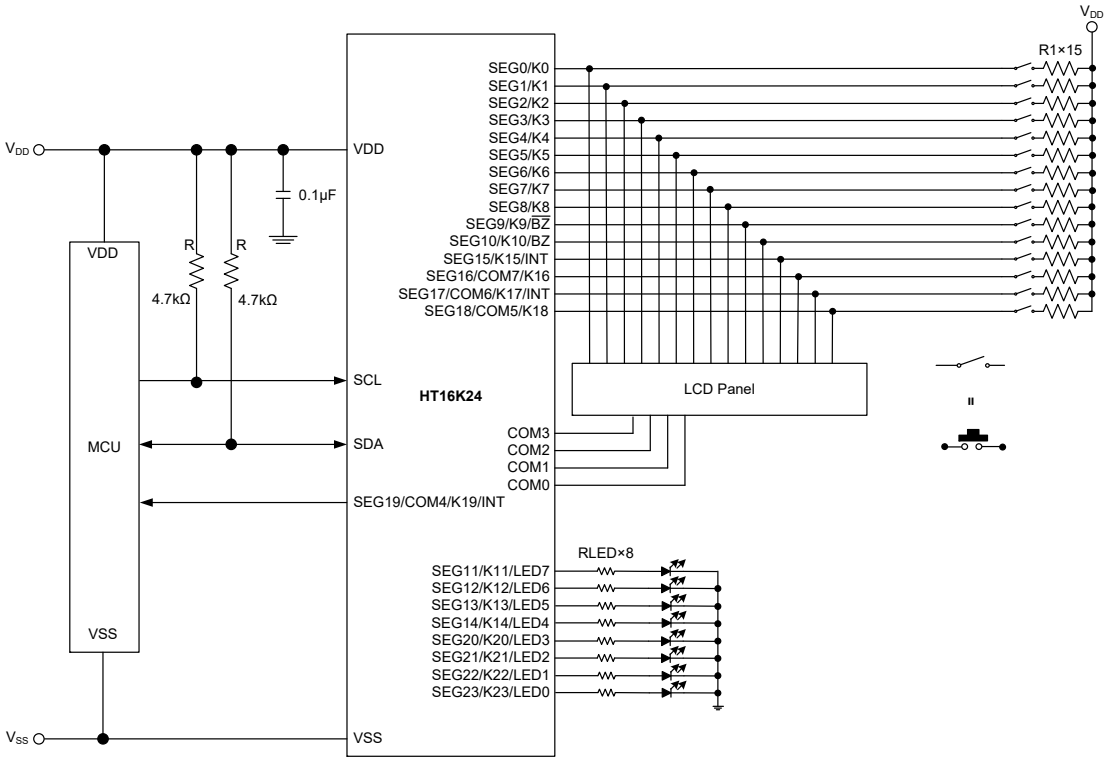
- Display Mode with INT



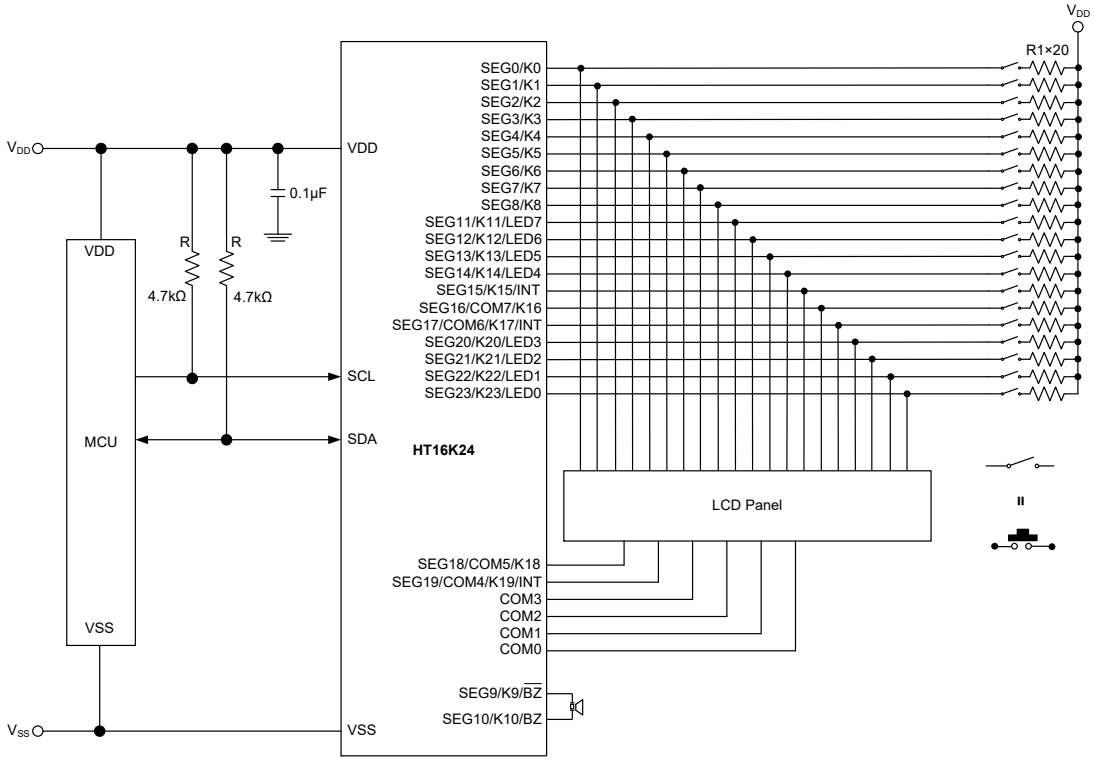
- Display Mode with LED and no INT



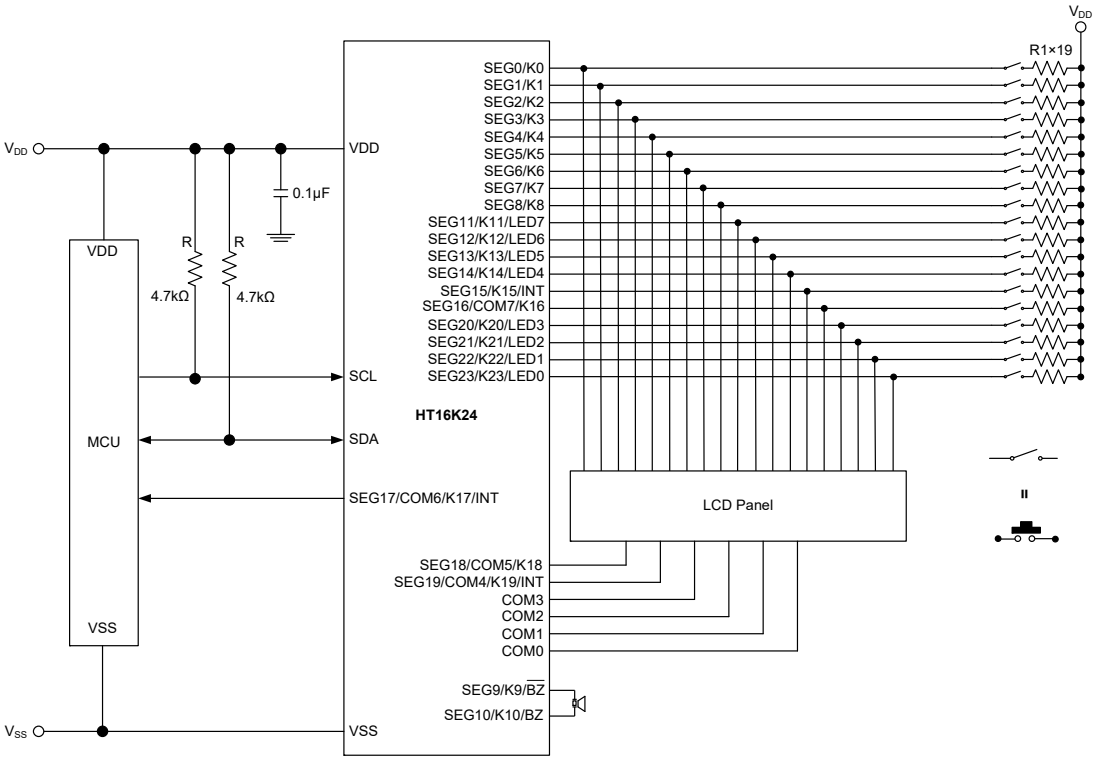
- Display Mode with LED and INT



- Display Mode with Buzzer and no INT



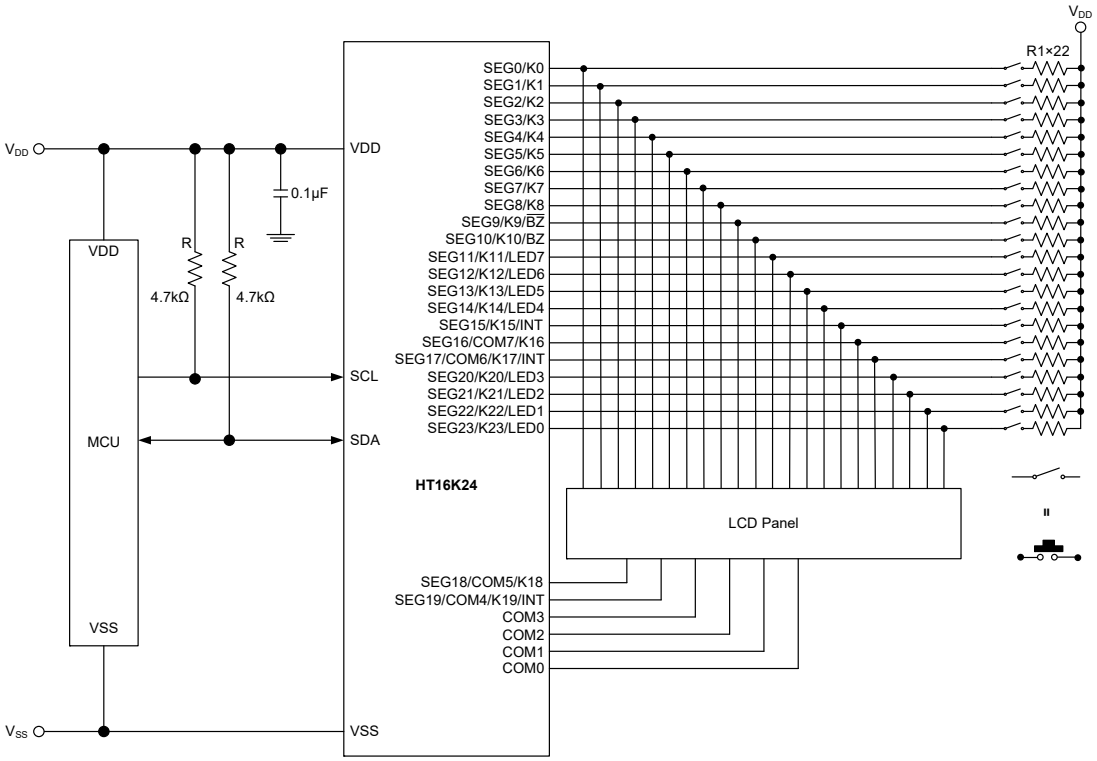
- Display Mode with Buzzer and INT



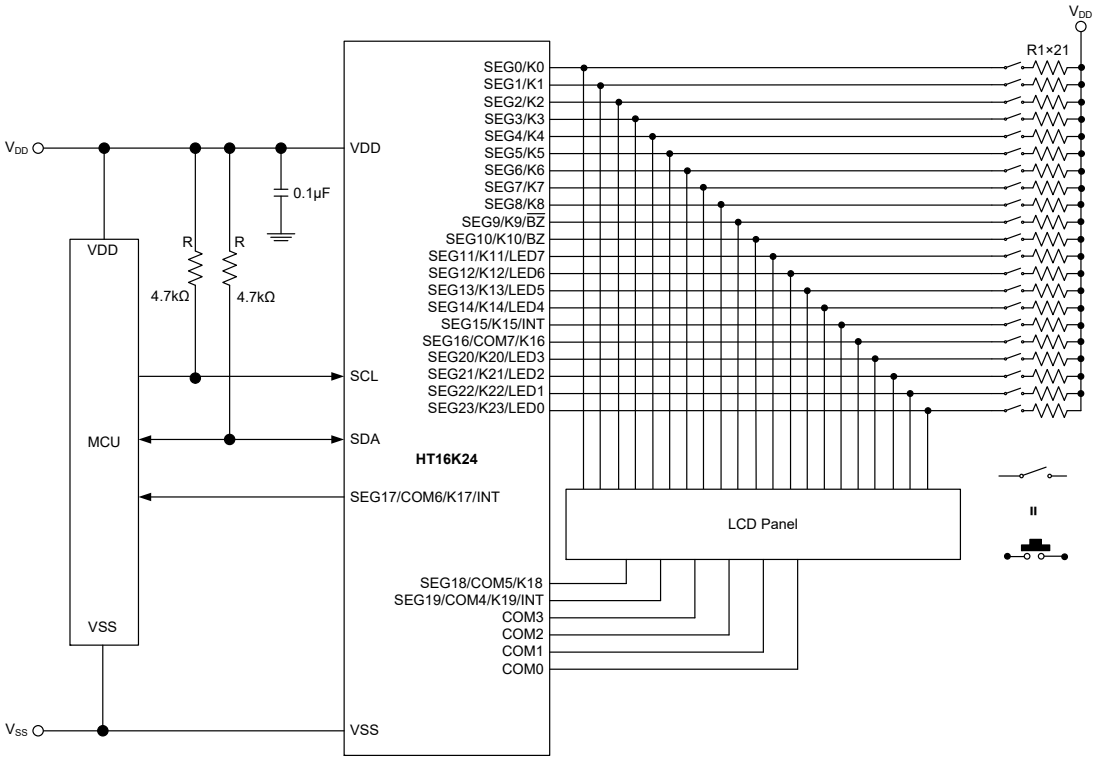
Note: R1=180kΩ~220kΩ, adjust R1 to fit the LCD visual quality.

22×6 Display Mode

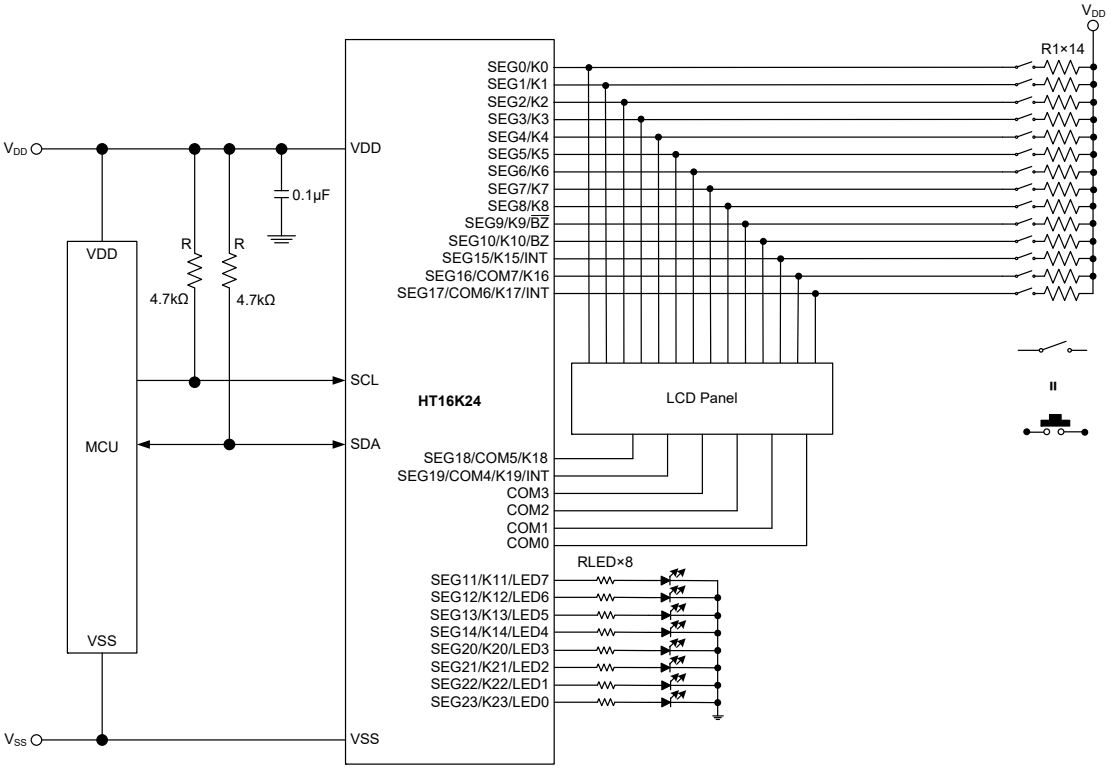
- Display Mode without INT



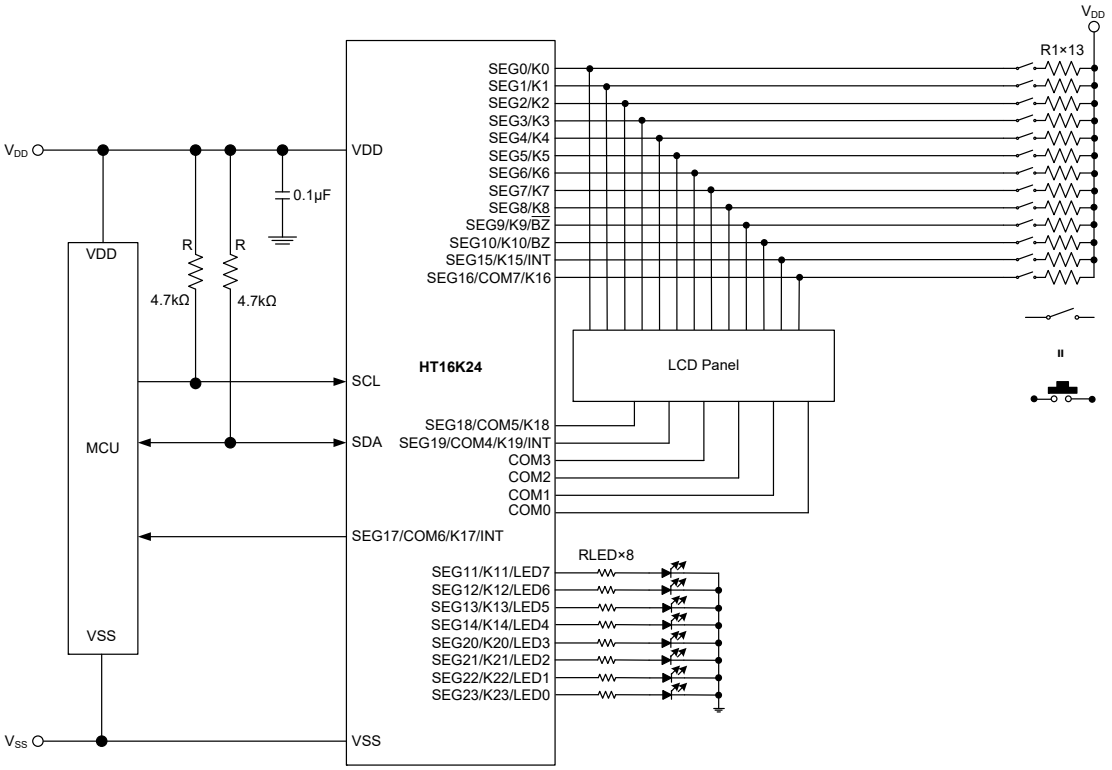
- Display Mode with INT



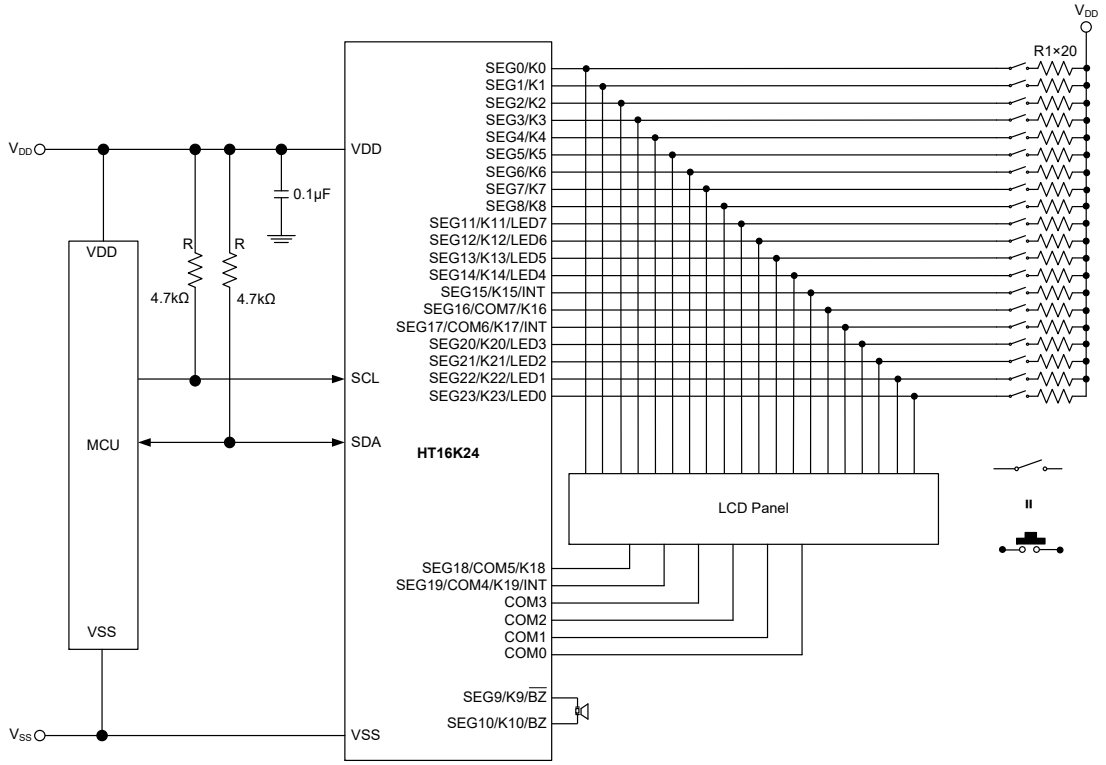
- Display Mode with LED and no INT



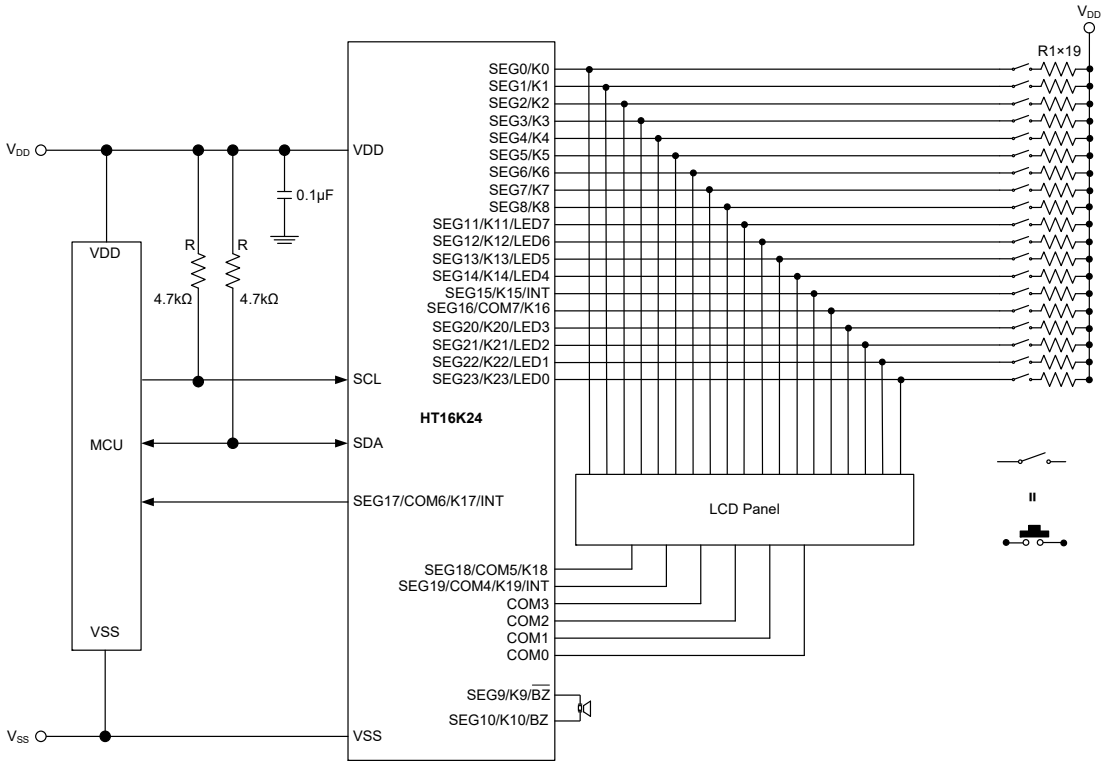
- Display Mode with LED and INT



- Display Mode with Buzzer and no INT



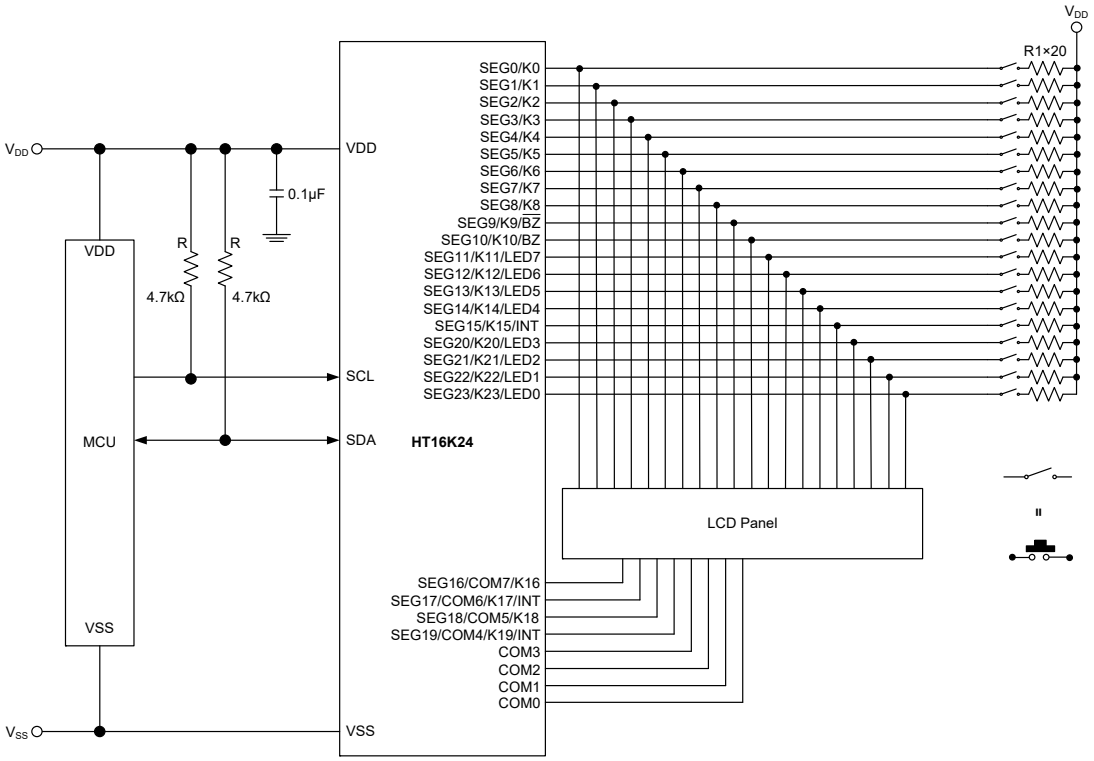
- Display Mode with Buzzer and INT



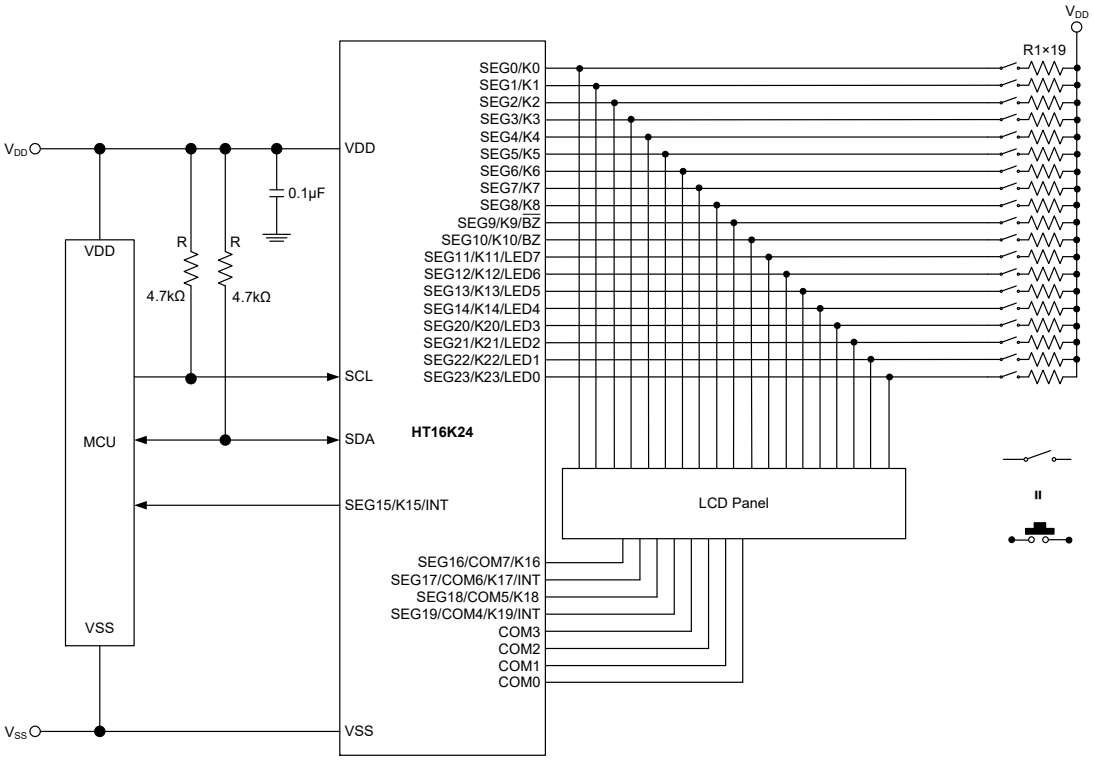
Note: R1=180kΩ~220kΩ, adjust R1 to fit the LCD visual quality.

20×8 Display Mode

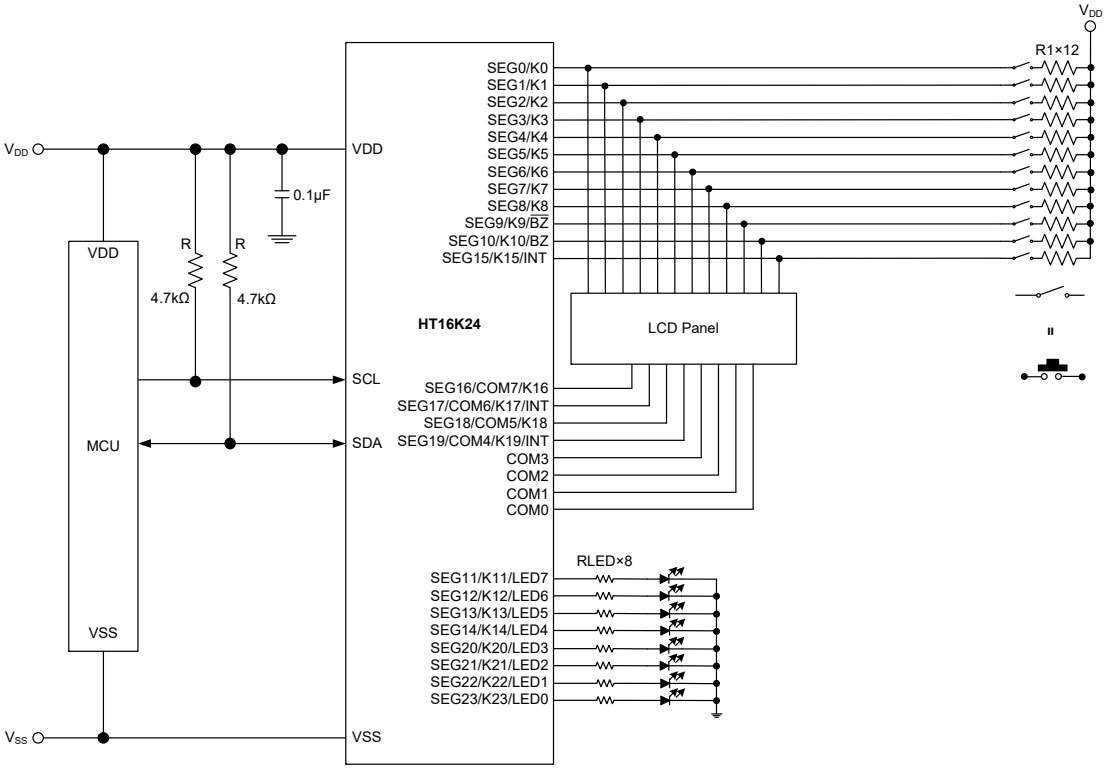
- Display Mode without INT



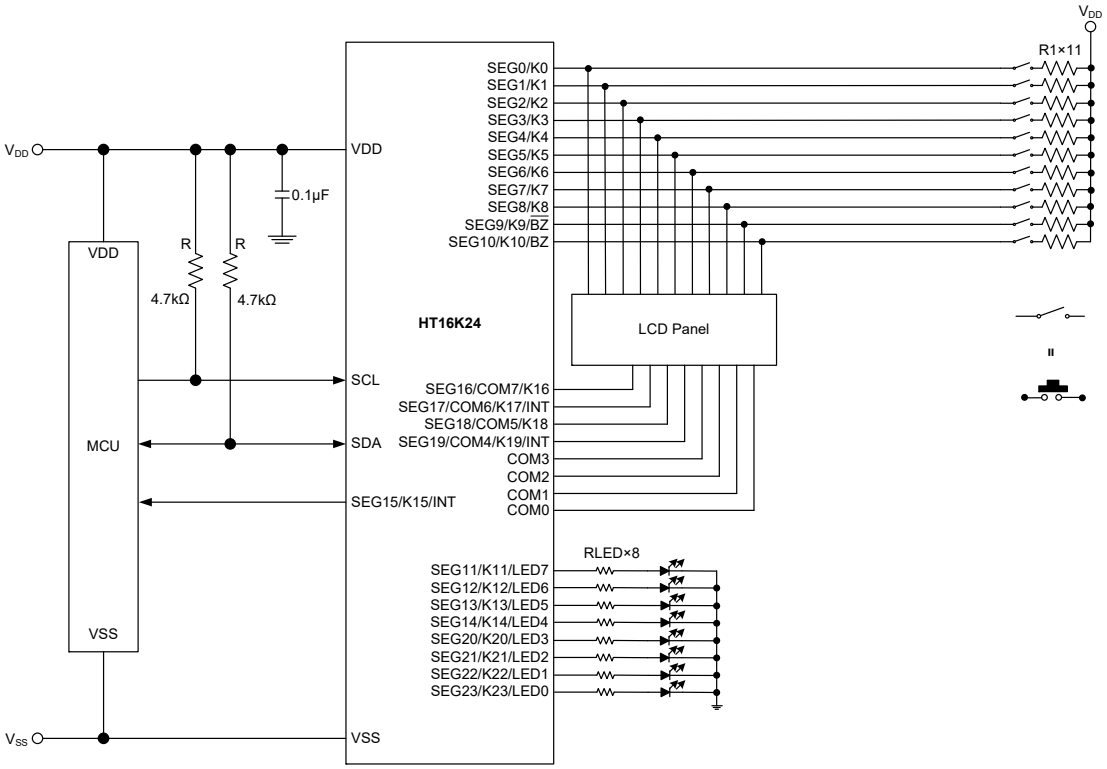
- Display Mode with INT



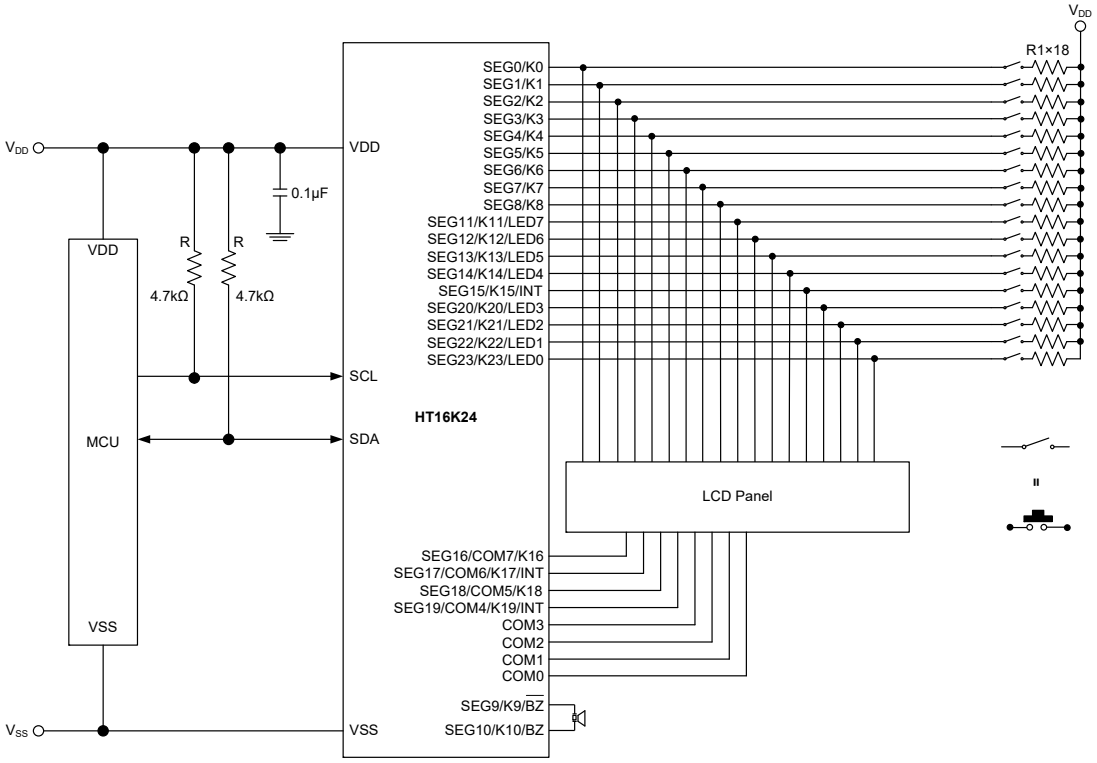
- Display Mode with LED and no INT



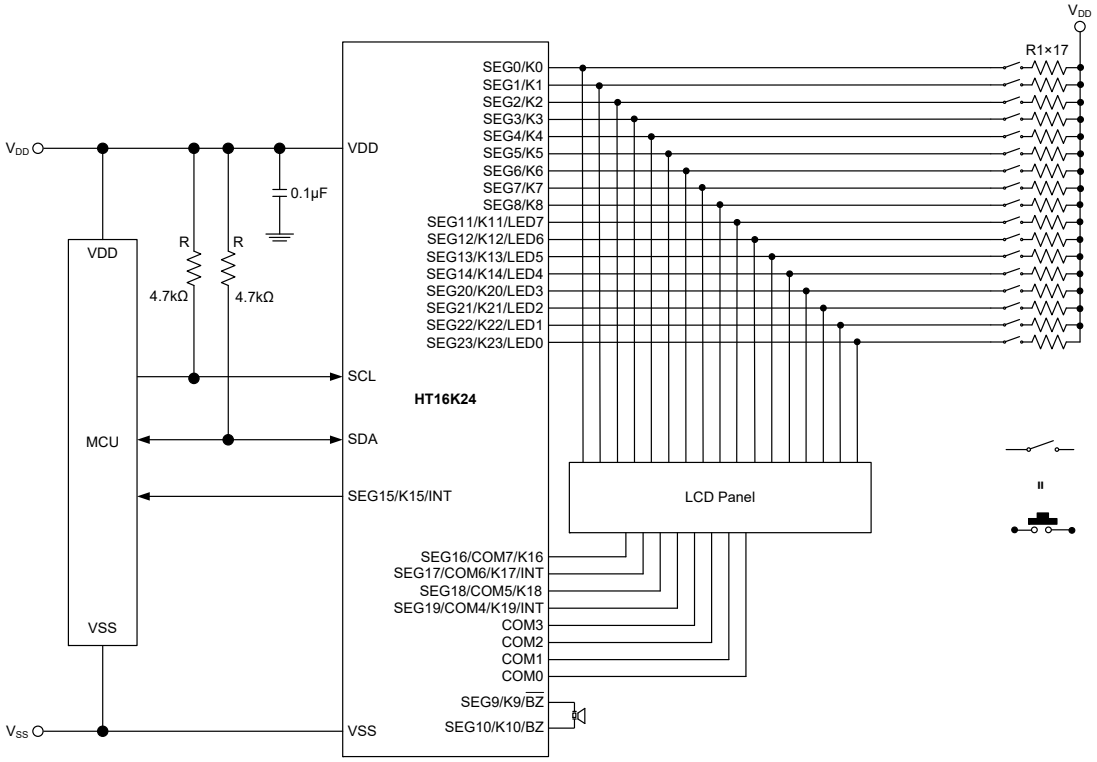
- Display Mode with LED and INT



- Display Mode with Buzzer and no INT



- Display Mode with Buzzer and INT



Note: R1=180kΩ~220kΩ, adjust R1 to fit the LCD visual quality.

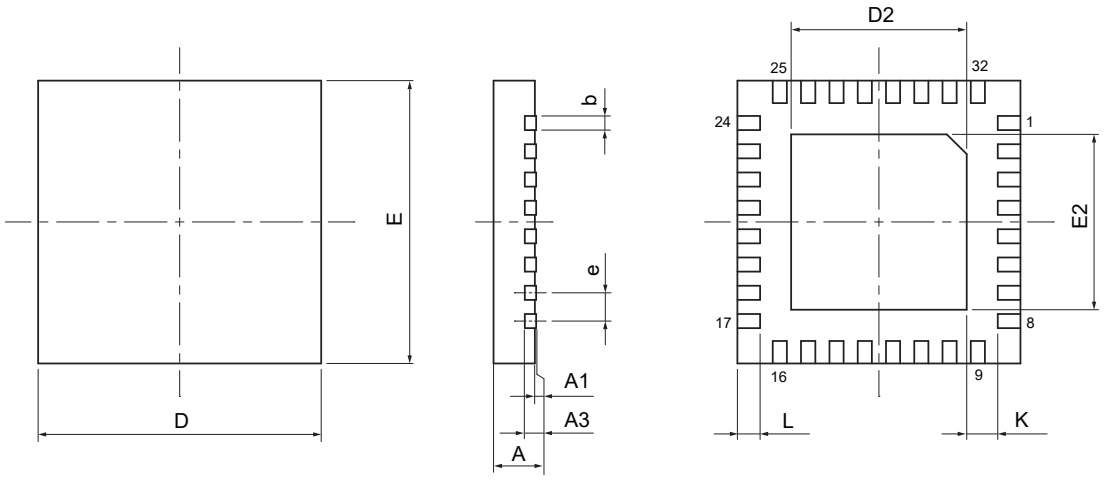
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

SAW Type 32-pin QFN (4mm×4mm×0.75mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3		0.008 REF	
b	0.006	0.008	0.010
D		0.157 BSC	
E		0.157 BSC	
e		0.016 BSC	
D2	0.100	—	0.108
E2	0.100	—	0.108
L	0.010	—	0.018
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF	
b	0.15	0.20	0.25
D		4.00 BSC	
E		4.00 BSC	
e		0.40 BSC	
D2	2.55	—	2.75
E2	2.55	—	2.75
L	0.25	—	0.45
K	0.20	—	—