HT16C24A/HT16C24AG
RAM Mapping 72×4/68×8/60×16 LCD Driver Controller

Features

- Operating voltage: 2.4V~5.5V
- Internal 32kHz RC oscillator
- Bias: 1/3, 1/4 or 1/5; Duty:1/4, 1/8 or 1/16
- Internal LCD bias generation with voltage-follower buffers
- I²C bus interface
- Two selectable LCD frame frequencies: 80Hz or 160Hz
- Up to 60 × 16 bits RAM for display data storage
- Display patterns:
  - 72×4 patterns: 72 segments and 4 commons
  - 68×8 patterns: 68 segments and 8 commons
  - 60×16 patterns: 60 segments and 16 commons
- Versatile blinking modes
- R/$\overline{W}$ address auto increment
- Internal 16-step voltage adjustment to adjust LCD operating voltage
- Low power consumption
- Provides the VLCD pin to adjust LCD operating voltage
- Manufactured in silicon gate CMOS process
- Package types: 64/80-pin LQFP and COG

Applications

- Electronic meter
- Water meter
- Gas meter
- Heat energy meter
- Household appliance
- Games
- Telephone
- Consumer electronics

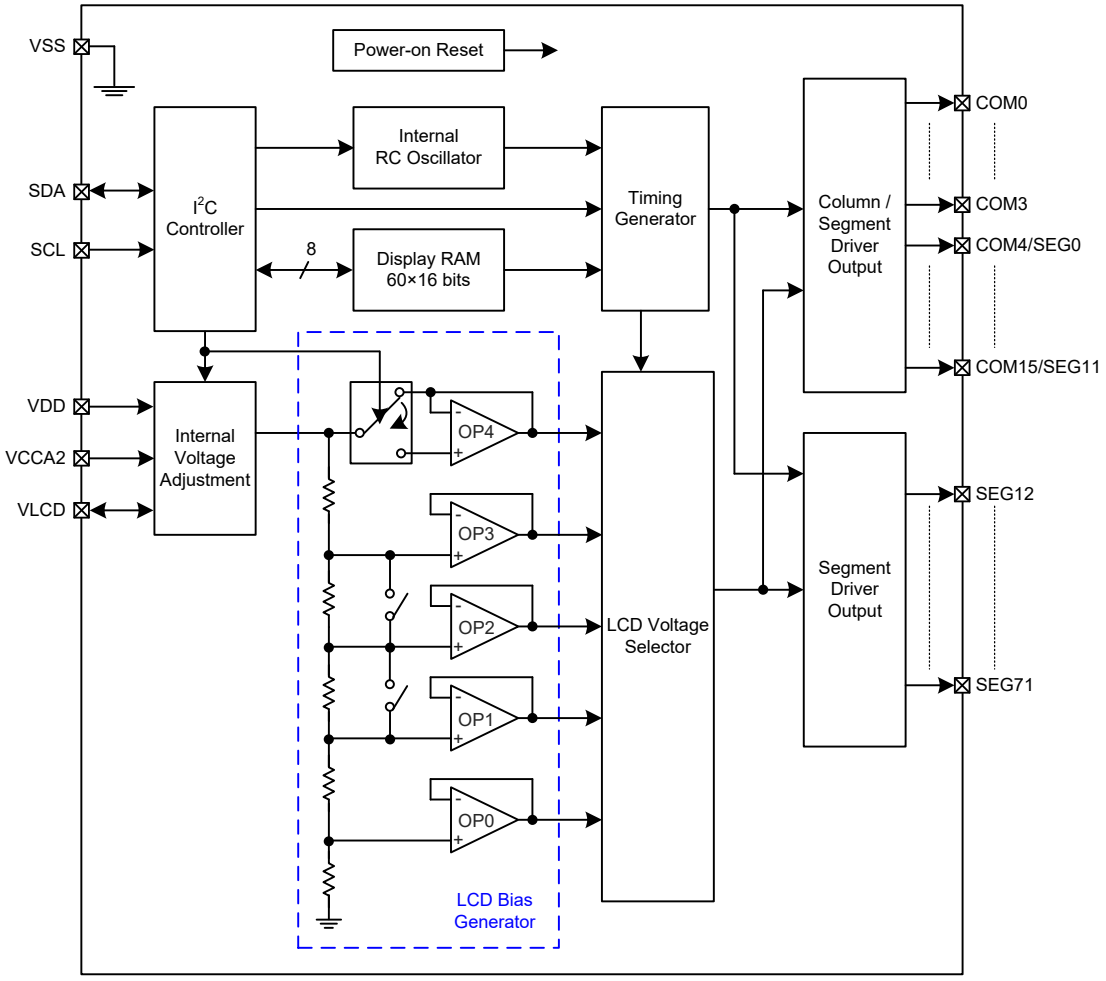
General Description

The HT16C24A/HT16C24AG devices are a memory mapping and multi-function LCD controller driver. The display segments of the devices are 288 patterns (72 segments and 4 commons), 544 patterns (68 segments and 8 commons) or 960 patterns (60 segments and 16 commons). The software configuration feature of the devices make it suitable for multiple LCD applications including LCD modules and display subsystems. The devices communicate with most microprocessors/microcontrollers via a two-line bidirectional I²C bus.

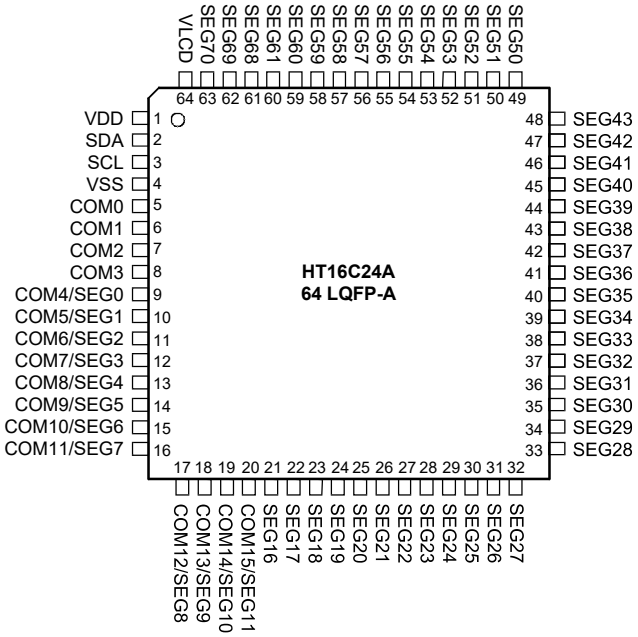
Selection Table

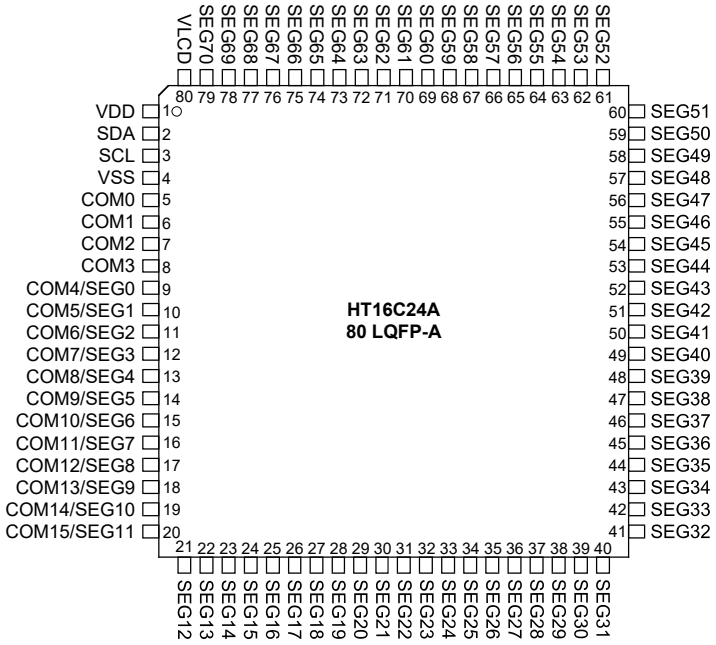
Part No.	VDD	Max. Resolution Segment × Common	LCD Voltage	Bias	Interface	Package
HT16C24A	2.4V~5.5V	72×4, 68×8, 60×16	2.4V~5.5V	1/3, 1/4, 1/5	I²C	64/80LQFP
HT16C24AG						Gold Bump

Block Diagram



Pin Assignment

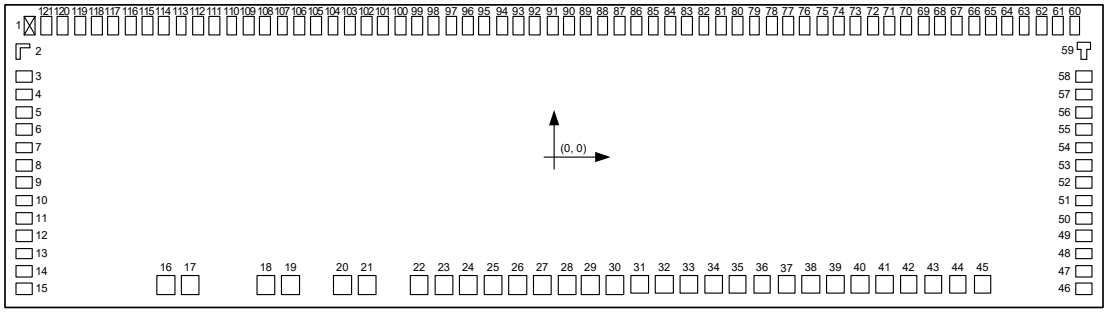




Note: 1. Application at $V_{DD} \leq V_{LCD}$ or $V_{LCD} \leq V_{DD}$.

2. The VCCA2 pad is internally connected with the VLCD pad.

Pad Assignment for COG



Note:

- VLCD (pad 20) must be connected to VCCA2 (pad 21) in the PCB layout for the application at $V_{DD} \leq V_{LCD}$ or $V_{LCD} \leq V_{DD}$.

Internal Voltage Adjustment (IVA) Set Command		VLCD (Pad 20)	SEG71 (Pad 13)	Note
DE bit	VE bit			
0	0	Input	Null	• VLCD support internal bias voltage.
0	1	Input	Null	• Internal Voltage Adjustment is null • VLCD support internal bias voltage
1	0	Input	Output	• VLCD support internal bias voltage
1	1	Input	Output	• VLCD support internal bias voltage

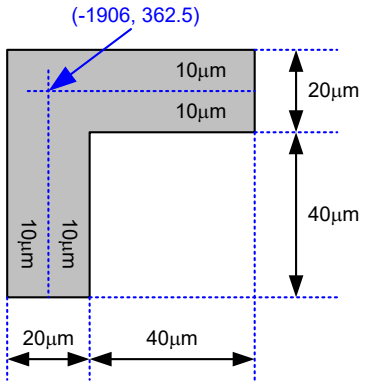
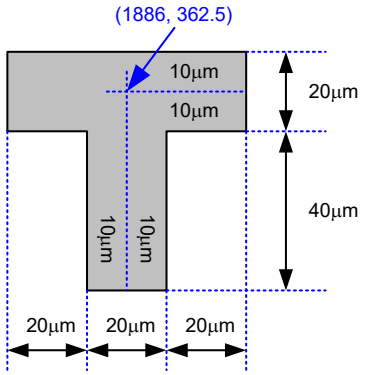
- VDD (pad 18) must be connected to VCCA2 (pad 21) in the PCB layout for the application at $V_{LCD} \leq V_{DD}$.

Internal Voltage Adjustment (IVA) Set Command		VLCD (Pad 20)	SEG71 (Pad 13)	Note
DE bit	VE bit			
0	0	Input	Null	• VLCD support internal bias voltage.
0	1	Output	Null	• Detect the internal bias voltage • VDD support internal bias voltage
1	0	Floating	Output	• VDD support internal bias voltage
1	1	Floating	Output	• VDD support internal bias voltage

Pad Dimensions for COG

Item	Number		Size		Unit
			X	Y	
Chip size	—		3948	1070	μm
Chip thickness	—		508		μm
Pad pitch	1, 3~15, 46~58, 60~121		60		μm
	16~45		87		μm
Bump size	Output pad	62~120	40	60	μm
		5~13, 48~55	60	40	μm
	Input pad	16~21	67	67	μm
	Dummy pad	1, 60, 61, 121	40	60	μm
		3, 4, 14, 15, 46, 47, 56, 57, 58	60	40	μm
		22~45	67	67	μm
Bump height	All pad		18±3		μm

Alignment Mark Dimensions for COG

Item	Number	Size	Unit
ALIGN_A	2		μm
ALIGN_B	59		μm

Pad Coordinates for COG

Unit: μm

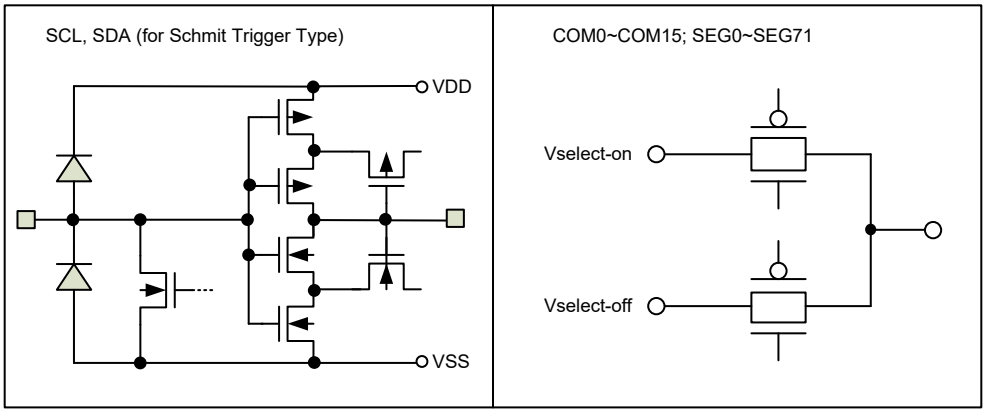
No	Name	X	Y	No	Name	X	Y
1	DUMMY	-1866.85	444.5	62	COM8/SEG4	1733.15	444.5
2	ALIGN_A	-1906.0	362.5	63	COM9/SEG5	1673.15	444.5
3	DUMMY	-1884.5	269.566	64	COM10/SEG6	1613.15	444.5
4	DUMMY	-1884.5	209.566	65	COM11/SEG7	1553.15	444.5
5	SEG63	-1884.5	149.566	66	COM12/SEG8	1493.15	444.5
6	SEG64	-1884.5	89.566	67	COM13/SEG9	1433.15	444.5
7	SEG65	-1884.5	29.566	68	COM14/SEG10	1373.15	444.5
8	SEG66	-1884.5	-30.434	69	COM15/SEG11	1313.15	444.5
9	SEG67	-1884.5	-90.434	70	SEG12	1253.15	444.5
10	SEG68	-1884.5	-150.434	71	SEG13	1193.15	444.5
11	SEG69	-1884.5	-210.434	72	SEG14	1133.15	444.5
12	SEG70	-1884.5	-270.434	73	SEG15	1073.15	444.5
13	SEG71	-1884.5	-330.434	74	SEG16	1013.15	444.5
14	DUMMY	-1884.5	-390.434	75	SEG17	953.15	444.5
15	DUMMY	-1884.5	-450.434	76	SEG18	893.15	444.5
16	SDA	-1381.81	-436.691	77	SEG19	833.15	444.5
17	SCL	-1294.81	-436.691	78	SEG20	773.15	444.5
18	VDD	-1023.81	-436.691	79	SEG21	713.15	444.5

No	Name	X	Y	No	Name	X	Y
19	VSS	-936.81	-436.691	80	SEG22	653.15	444.5
20	VLCD	-750.81	-436.691	81	SEG23	593.15	444.5
21	VCCA2	-663.81	-436.691	82	SEG24	533.15	444.5
22	DUMMY	-477.81	-436.691	83	SEG25	473.15	444.5
23	DUMMY	-390.81	-436.691	84	SEG26	413.15	444.5
24	DUMMY	-303.81	-436.691	85	SEG27	353.15	444.5
25	DUMMY	-216.81	-436.691	86	SEG28	293.15	444.5
26	DUMMY	-129.81	-436.691	87	SEG29	233.15	444.5
27	DUMMY	-42.81	-436.691	88	SEG30	173.15	444.5
28	DUMMY	44.19	-436.691	89	SEG31	113.15	444.5
29	DUMMY	131.19	-436.691	90	SEG32	53.15	444.5
30	DUMMY	218.19	-436.691	91	SEG33	-6.85	444.5
31	DUMMY	305.19	-436.691	92	SEG34	-66.85	444.5
32	DUMMY	392.19	-436.691	93	SEG35	-126.85	444.5
33	DUMMY	479.19	-436.691	94	SEG36	-186.85	444.5
34	DUMMY	566.19	-436.691	95	SEG37	-246.85	444.5
35	DUMMY	653.19	-436.691	96	SEG38	-306.85	444.5
36	DUMMY	740.19	-436.691	97	SEG39	-366.85	444.5
37	DUMMY	827.19	-436.691	98	SEG40	-426.85	444.5
38	DUMMY	914.19	-436.691	99	SEG41	-486.85	444.5
39	DUMMY	1001.19	-436.691	100	SEG42	-546.85	444.5
40	DUMMY	1088.19	-436.691	101	SEG43	-606.85	444.5
41	DUMMY	1175.19	-436.691	102	SEG44	-666.85	444.5
42	DUMMY	1262.19	-436.691	103	SEG45	-726.85	444.5
43	DUMMY	1349.19	-436.691	104	SEG46	-786.85	444.5
44	DUMMY	1436.19	-436.691	105	SEG47	-846.85	444.5
45	DUMMY	1523.19	-436.691	106	SEG48	-906.85	444.5
46	DUMMY	1884.5	-450.434	107	SEG49	-966.85	444.5
47	DUMMY	1884.5	-390.434	108	SEG50	-1026.85	444.5
48	COM0	1884.5	-330.434	109	SEG51	-1086.85	444.5
49	COM1	1884.5	-270.434	110	SEG52	-1146.85	444.5
50	COM2	1884.5	-210.434	111	SEG53	-1206.85	444.5
51	COM3	1884.5	-150.434	112	SEG54	-1266.85	444.5
52	COM4/SEG0	1884.5	-90.434	113	SEG55	-1326.85	444.5
53	COM5/SEG1	1884.5	-30.434	114	SEG56	-1386.85	444.5
54	COM6/SEG2	1884.5	29.566	115	SEG57	-1446.85	444.5
55	COM7/SEG3	1884.5	89.566	116	SEG58	-1506.85	444.5
56	DUMMY	1884.5	149.566	117	SEG59	-1566.85	444.5
57	DUMMY	1884.5	209.566	118	SEG60	-1626.85	444.5
58	DUMMY	1884.5	269.566	119	SEG61	-1686.85	444.5
59	ALIGN_B	1886.0	362.5	120	SEG62	-1746.85	444.5
60	DUMMY	1853.15	444.5	121	DUMMY	-1806.85	444.5
61	DUMMY	1793.15	444.5				

Pin Description

Pin Name	Type	Description
SDA	I/O	Serial Data Input/Output for I^2C interface
SCL	I	Serial Clock Input for I^2C interface
VDD	—	Positive power supply
VSS	—	Negative power supply, ground
VCCA2	—	Power supply for LCD bias generator
VLCD	—	Power supply for LCD driver
COM0~COM3	O	LCD Common outputs
COM4/SEG0~ COM15/SEG11	O	LCD Common/Segment multiplexed driver outputs
SEG12~SEG71	O	LCD Segment outputs

Approximate Internal Connections



Absolute Maximum Ratings

Supply Voltage ..... V_{SS}-0.3V to V_{SS}+6.5V

Input Voltage ..... V_{SS}-0.3V to V_{DD}+0.3V

Storage Temperature ..... -60°C to 150°C

Operating Temperature ..... -40°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

V_{SS}=0V, V_{DD}=2.4V~5.5V, V_{LCD}=2.4V~5.5V, Ta=-40°C~85°C, VCCA2 pad is connected to VLCD pad

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{DD}	Operating Voltage	—	—	2.4	—	5.5	V
V_{LCD}	Operating Voltage	—	—	2.4	—	5.5	V
I_{DD}	Operating Current	3V	No load, V_{LCD}=V_{DD}, 1/3 bias, f_{LCD}=80Hz, LCD display on, internal system oscillator on, DA0~DA3 are set to "0000"	—	30	45	μA
		5V		—	40	60	μA
I_{DD1}	Operating Current	3V	No load, V_{LCD}=V_{DD}, 1/3 bias f_{LCD}=80Hz, LCD display off, internal system oscillator on, DA0~DA3 are set to "0000"	—	2	5	μA
		5V		—	4	10	μA
I_{STB}	Standby Current	3V	No load, V_{LCD}=V_{DD}, LCD display off, internal system oscillator off	—	—	1	μA
		5V		—	—	2	μA
V_{IH}	Input High Voltage	—	SDA ,SCL	0.7V_{DD}	—	V_{DD}	V
V_{IL}	Input Low Voltage	—	SDA, SCL	0	—	0.3V_{DD}	V
I_{IL}	Input Leakage Current	—	V_{IN}=V_{SS} or V_{DD}	-1	—	1	μA
I_{OL}	Low Level Output Current	3V	V_{OL}=0.4V for SDA	3	—	—	mA
		5V		6	—	—	mA
I_{OL1}	LCD COM Sink Current	3V	V_{LCD}=3V, V_{OL}=0.3V	250	400	—	μA
		5V	V_{LCD}=5V, V_{OL}=0.5V	500	800	—	μA
I_{OH1}	LCD COM Source Current	3V	V_{LCD}=3V, V_{OH}=2.7V	-140	-230	—	μA
		5V	V_{LCD}=5V, V_{OH}=4.5V	-300	-500	—	μA
I_{OL2}	LCD SEG Sink Current	3V	V_{LCD}=3V, V_{OL}=0.3V	250	400	—	μA
		5V	V_{LCD}=5V, V_{OL}=0.5V	500	800	—	μA
I_{OH2}	LCD SEG Source Current	3V	V_{LCD}=3V, V_{OH}=2.7V	-140	-230	—	μA
		5V	V_{LCD}=5V, V_{OH}=4.5V	-300	-500	—	μA

A.C. Characteristics

V_{SS}=0V, V_{DD}=2.4V~5.5V, V_{LCD}=2.4V~5.5V, Ta=-40°C~85°C, VCCA2 pad is connected to VLCD pad

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
f_{LCD1}	LCD Frame Frequency	4V	1/4 duty, Ta=25°C	72	80	88	Hz
			1/4 duty, Ta=-40~85°C	52	80	124	Hz
f_{LCD2}	LCD Frame Frequency	4V	1/4 duty, Ta=25°C	144	160	176	Hz
			1/4 duty, Ta=-40~85°C	104	160	248	Hz
V_{POR}	V_{DD} Start Voltage to Ensure Power-on Reset	—	—	—	—	100	mV
R_{RVDD}	V_{DD} Rise Rate to Ensure Power-on Reset	—	—	0.05	—	—	V/ms
t_{POR}	Minimum Time for VDD to Remain at V_{POR} to Ensure Power-on Reset	—	—	10	—	—	ms

A.C. Characteristics – I²C Interface

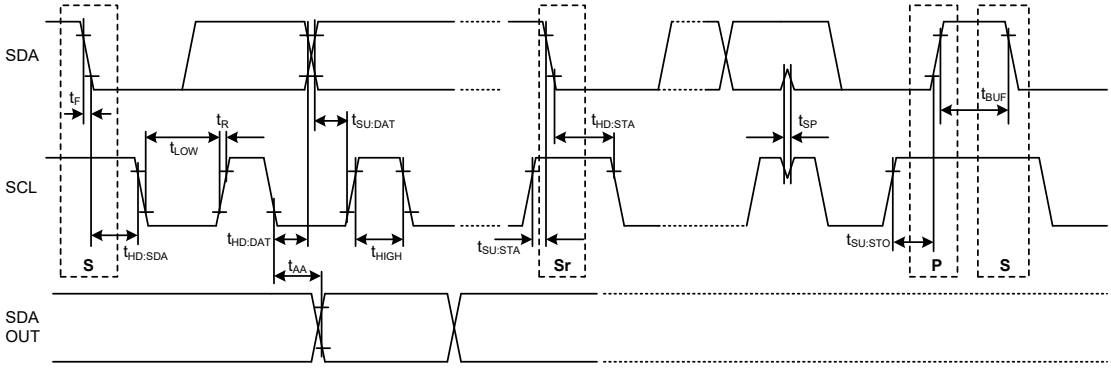
Ta=-40°C~85°C

Symbol	Parameter	Condition	V_{DD}=2.4V~5.5V		V_{DD}=3.0V~5.5V		Unit
			Min.	Max.	Min.	Max.	
f_{SCL}	Clock Frequency	—	—	100	—	400	KHz
t_{BUF}	Bus Free Time	Time in which the bus must be free before a new transmission can start	4.7	—	1.3	—	μs
$t_{HD: STA}$	Start Condition Hold Time	After this period, the first clock pulse is generated	4.0	—	0.6	—	μs
t_{LOW}	SCL Low Time	—	4.7	—	1.3	—	μs
t_{HIGH}	SCL High Time	—	4.0	—	0.6	—	μs
$t_{SU: STA}$	Start Condition Setup Time	Only relevant for repeated START condition	4.7	—	0.6	—	μs
$t_{HD: DAT}$	Data Hold Time	—	0	—	0	—	ns
$t_{SU: DAT}$	Data Setup Time	—	250	—	100	—	ns
t_R	SDA and SCL Rising Time	Note	—	1.0	—	0.3	μs
t_F	SDA and SCL Falling Time	Note	—	0.3	—	0.3	μs
$t_{SU: STO}$	Stop Condition Setup Time	—	4.0	—	0.6	—	μs
t_{AA}	Output Valid from Clock	—	—	3.5	—	0.9	μs
t_{SP}	Input Filter Time Constant (SDA and SCL Pins)	Noise suppression time	—	100	—	50	ns

Note: These parameters are periodically sampled but not 100% tested.

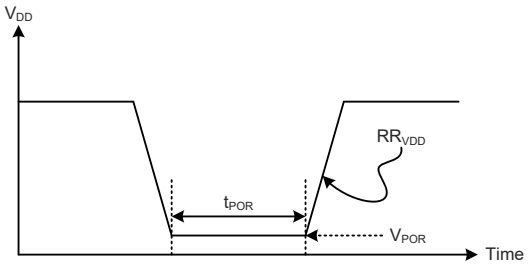
Timing Diagrams

I²C Timing



Power On Reset Timing

The devices must be powered up under certain conditions to ensure correct operation as shown in the accompanying diagram.



Note that if the powers on reset timing conditions are not satisfied during the power on/off sequence, the internal power on reset (POR) circuit will not operate normally. Also if VDD drops below the operating voltage minimum voltage specification during operation, the power on reset timing conditions must be also satisfied. This means that VDD must fall to 0V and remain at 0V for a minimum time of 10ms before rising to the normal operating voltage.

Functional Description

Power-On Reset

When the power is applied, the devices are initialized by an internal power-on reset circuit. The status of the internal circuits after initialization is as follows:

- All common/segment outputs are set to V_{DD} when VCCA2 pad is connected to VDD pad
- All common/segment outputs are set to V_{LCD} when VCCA2 pad is connected to VLCD pad
- The drive mode 1/4 duty output and 1/3 bias is selected
- The system oscillator and the LCD bias generator are both off
- LCD display is off
- Internal voltage adjustment function is enabled
- The Segment/VLCD shared pin is set as the Segment pin
- Detection switch for the VLCD pin is disabled
- Frame Frequency is set to 80Hz
- Blinking function is switched off

Data transfers on the I^2C bus should be avoided for 1ms following power-on to allow completion of the reset action.

Display Memory – RAM Structure

The display RAM is static 60×16 bits RAM which stores the LCD data. Logic "1" in the RAM bit-map indicates the "on" state of the corresponding LCD segment; similarly, logic "0" indicates the "off" state.

The contents of the RAM data are directly mapped to the LCD data. The first RAM column corresponds to the segments operated with respect to COM0. In multiplexed LCD applications the segment data from 2nd to 16th column of the display RAM are time-multiplexed from COM1 to COM15 respectively. The following is a mapping from the RAM data to the LCD pattern:

Output	COM3	COM2	COM1	COM0	Output	COM3	COM2	COM1	COM0	Address
SEG1					SEG0					00H
SEG3					SEG2					01H
SEG5					SEG4					02H
SEG7					SEG6					03H
SEG9					SEG8					04H
SEG11					SEG10					05H
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
SEG71					SEG70					23H
	D7	D6	D5	D4		D3	D2	D1	D0	Data

RAM Mapping of 72×4 Display Mode

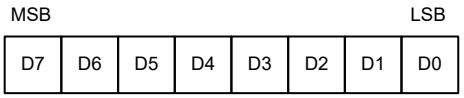
Output	COM7/ SEG3	COM6/ SEG2	COM5/ SEG1	COM4/ SEG0	COM3	COM2	COM1	COM0	Address
SEG4									00H
SEG5									01H
SEG6									02H
SEG7									03H
SEG8									04H
SEG9									05H
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
SEG71									43H
	D7	D6	D5	D4	D3	D2	D1	D0	Data

RAM Mapping of 68×8 Display Mode

Output	COM15/SEG11	COM14/SEG10	COM13/SEG9	COM12/SEG8	COM11/SEG7	COM10/SEG6	COM9/SEG5	COM8/SEG4	Addr.	COM7/SEG3	COM6/SEG2	COM5/SEG1	COM4/SEG0	COM3	COM2	COM1	COM0	Addr.
SEG12									01H									00H
SEG13									03H									02H
SEG14									05H									04H
SEG15									07H									06H
SEG16									09H									08H
SEG17									0BH									0AH
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
SEG71									77H									76H
	D7	D6	D5	D4	D3	D2	D1	D0	Data	D7	D6	D5	D4	D3	D2	D1	D0	Data

RAM Mapping of 60×16 Display Mode

Display data transfer format for I²C bus:



System Oscillator

The timing for the internal logic and the LCD drive signals are generated by an internal oscillator. The system clock frequency (f_{SYS}) determines the LCD frame frequency. During initial system power-on the system oscillator will be in the stop state.

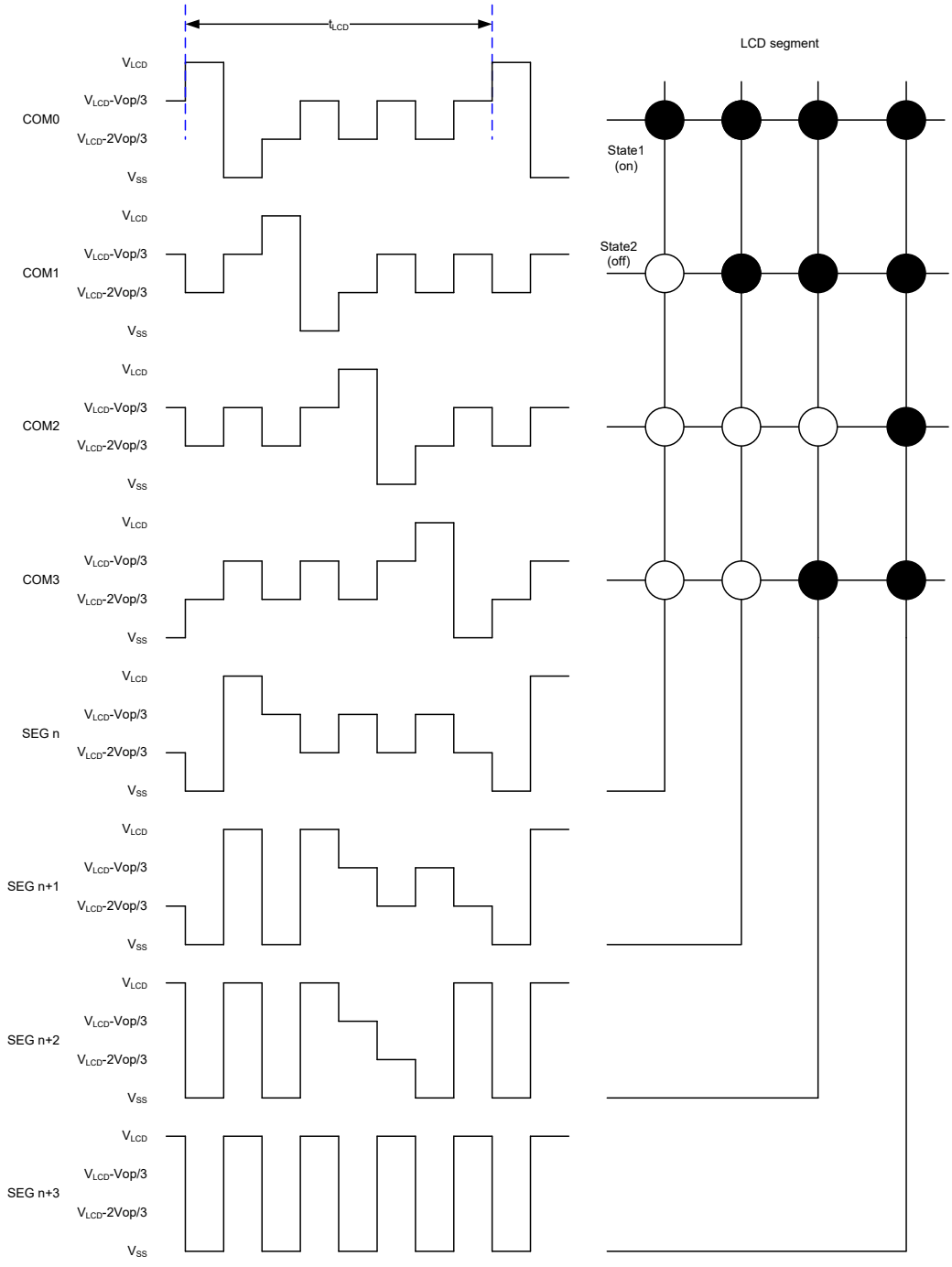
LCD Bias Generator

The full-scale LCD voltage (V_{OP}) is obtained from (V_{LCD}–V_{SS}). The LCD voltage may be temperature compensated externally through the voltage supply to the VLCD pin.

Fractional LCD biasing voltages, known as 1/3, 1/4 or 1/5 bias voltage, are obtained from an internal voltage divider of five serial resistors connected between the VLCD and VSS pins. The specific resistor can be switched out of circuits to provide a 1/3, 1/4 or 1/5 bias voltage level configuration.

LCD Drive Mode Waveforms

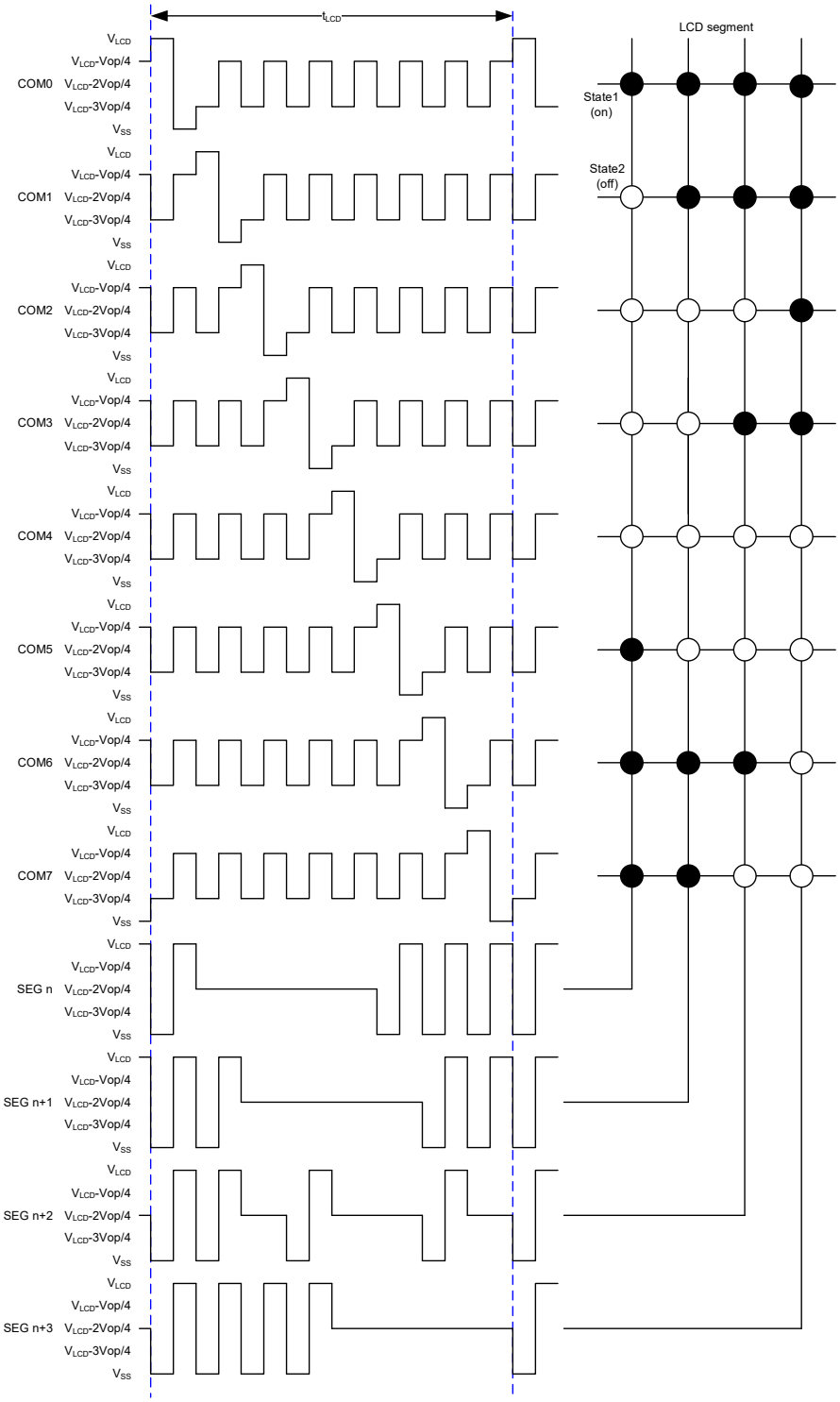
- When the LCD drive mode is selected as 1/4 duty and 1/3 bias, the waveform and LCD display is shown as follows:



Waveforms for 1/4 Duty Drive Mode with 1/3 Bias (V_{OP}=V_{LCD}-V_{SS})

Note: t_{LCD}=1/f_{LCD}

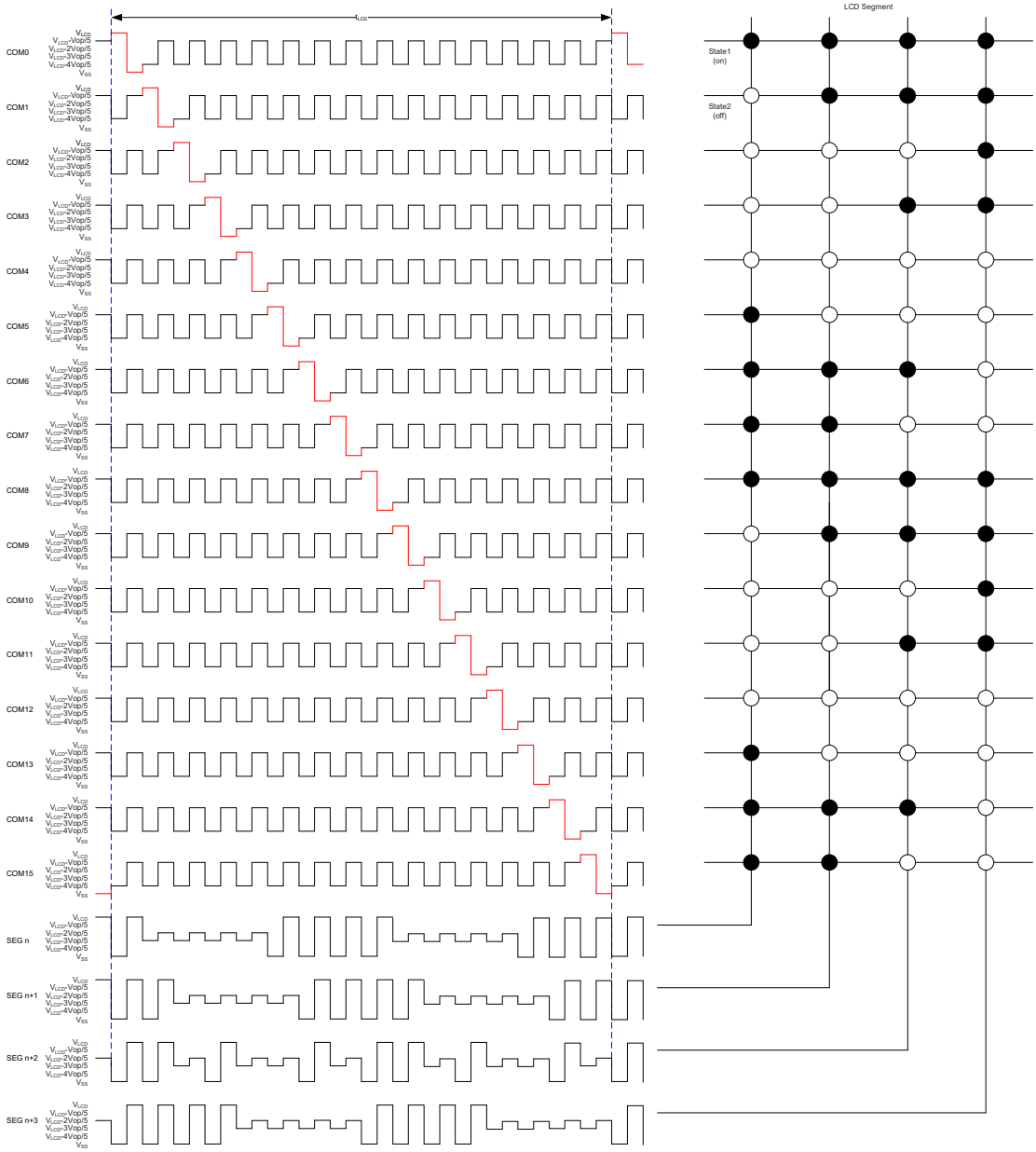
- When the LCD drive mode is selected as 1/8 duty and 1/4 bias, the waveform and LCD display is shown as follows:



Waveforms for 1/8 Duty Drive Mode with 1/4 Bias (V_{OP}=V_{LCD}-V_{SS})

Note: t_{LCD}=1/f_{LCD}

- When the LCD drive mode is selected as 1/16 duty and 1/5 bias, the waveform and LCD display is shown as follows:



Waveforms for 1/16 Duty Drive Mode with 1/5 Bias (V_{OP}=V_{LCD}-V_{SS})

Note: $t_{LCD}=1/f_{LCD}$

Segment Driver Outputs

The LCD drive section includes up to 72 segment outputs which should be connected directly to the LCD panel. The segment output signals are generated in accordance with the multiplexed column signals and with the data resident in the display latch. The unused segment outputs should be left open-circuit.

Column Driver Outputs

The LCD drive section includes up to 16 column outputs which should be connected directly to the LCD panel. The column output signals are generated in accordance with the selected LCD drive mode. The unused column outputs should be left open-circuit.

Address Pointer

The addressing mechanism for the display RAM is implemented using the address pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the address pointer by the address pointer command.

Blinker Function

The devices contain versatile blinking capabilities. The whole display can be blinked at frequencies selected by the Blink command. The blinking frequency is a subdivided ratio of the system frequency. The ratio between the system oscillator and blinking frequencies depends on the blinking mode in which the devices are operating, as shown in the following table.

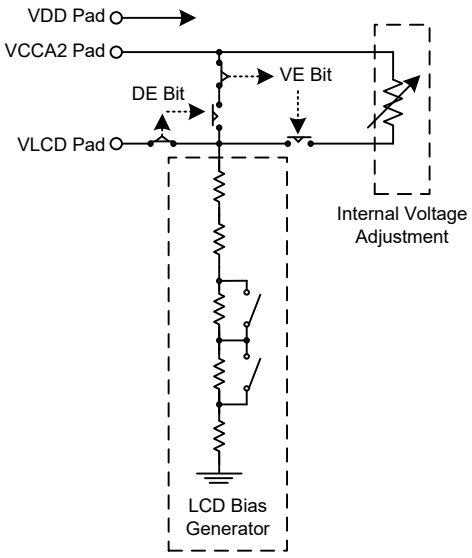
Frame Frequency

The devices provide two frame frequencies selected with mode setting command known as 80Hz and 160Hz respectively.

Blinking Mode	Operating Mode Ratio	Blinking Frequency (Hz)
0	0	Blink off
1	f_{SYS}/16384	2
2	f_{SYS}/32768	1
3	f_{SYS}/65536	0.5

Internal V_{LCD} Voltage Adjustment

- The internal V_{LCD} adjustment contains four resistors in series and a 4-bit programmable analog switch which can provide sixteen voltage adjustment options using the V_{LCD} voltage adjustment command.
- The internal V_{LCD} adjustment structure is shown in the diagram:



- The relationship between the programmable 4-bit analog switch and the VLCD output voltage is shown in the table:

1. When VCCA2 pad is connected to VDD pad

Bias / DA3~DA0	1/3	1/4	1/5	Note
00H	1.000×V_{DD}	1.000×V_{DD}	1.000×V_{DD}	Default value
01H	0.944×V_{DD}	0.957×V_{DD}	0.966×V_{DD}	
02H	0.894×V_{DD}	0.918×V_{DD}	0.934×V_{DD}	
03H	0.849×V_{DD}	0.882×V_{DD}	0.904×V_{DD}	
04H	0.808×V_{DD}	0.849×V_{DD}	0.875×V_{DD}	
05H	0.771×V_{DD}	0.818×V_{DD}	0.849×V_{DD}	
06H	0.738×V_{DD}	0.789×V_{DD}	0.824×V_{DD}	
07H	0.707×V_{DD}	0.763×V_{DD}	0.801×V_{DD}	
08H	0.678×V_{DD}	0.738×V_{DD}	0.779×V_{DD}	
09H	0.652×V_{DD}	0.714×V_{DD}	0.758×V_{DD}	
0AH	0.628×V_{DD}	0.692×V_{DD}	0.738×V_{DD}	
0BH	0.605×V_{DD}	0.672×V_{DD}	0.719×V_{DD}	
0CH	0.584×V_{DD}	0.652×V_{DD}	0.701×V_{DD}	
0DH	0.565×V_{DD}	0.634×V_{DD}	0.684×V_{DD}	
0EH	0.547×V_{DD}	0.616×V_{DD}	0.668×V_{DD}	
0FH	0.529×V_{DD}	0.600×V_{DD}	0.652×V_{DD}	

2. When VCCA2 pad is connected to VLCD pad

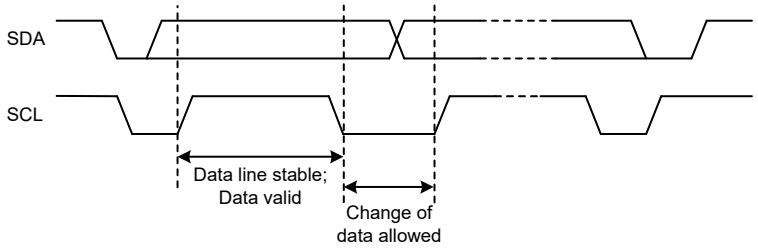
Bias / DA3~DA0	1/3	1/4	1/5	Note
00H	1.000×V_{LCD}	1.000×V_{LCD}	1.000×V_{LCD}	Default value
01H	0.944×V_{LCD}	0.957×V_{LCD}	0.966×V_{LCD}	
02H	0.894×V_{LCD}	0.918×V_{LCD}	0.934×V_{LCD}	
03H	0.849×V_{LCD}	0.882×V_{LCD}	0.904×V_{LCD}	
04H	0.808×V_{LCD}	0.849×V_{LCD}	0.875×V_{LCD}	
05H	0.771×V_{LCD}	0.818×V_{LCD}	0.849×V_{LCD}	
06H	0.738×V_{LCD}	0.789×V_{LCD}	0.824×V_{LCD}	
07H	0.707×V_{LCD}	0.763×V_{LCD}	0.801×V_{LCD}	
08H	0.678×V_{LCD}	0.738×V_{LCD}	0.779×V_{LCD}	
09H	0.652×V_{LCD}	0.714×V_{LCD}	0.758×V_{LCD}	
0AH	0.628×V_{LCD}	0.692×V_{LCD}	0.738×V_{LCD}	
0BH	0.605×V_{LCD}	0.672×V_{LCD}	0.719×V_{LCD}	
0CH	0.584×V_{LCD}	0.652×V_{LCD}	0.701×V_{LCD}	
0DH	0.565×V_{LCD}	0.634×V_{LCD}	0.684×V_{LCD}	
0EH	0.547×V_{LCD}	0.616×V_{LCD}	0.668×V_{LCD}	
0FH	0.529×V_{LCD}	0.600×V_{LCD}	0.652×V_{LCD}	

I²C Serial Interface

The devices support I²C serial interface. The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line, SDA, and a serial clock line, SCL. Both lines are connected to the positive supply via pull-up resistors with a typical value of 4.7kΩ. When the bus is free, both lines are high. Devices connected to the bus must have open-drain or open-collector outputs to implement a wired-or function. Data transfer is initiated only when the bus is not busy.

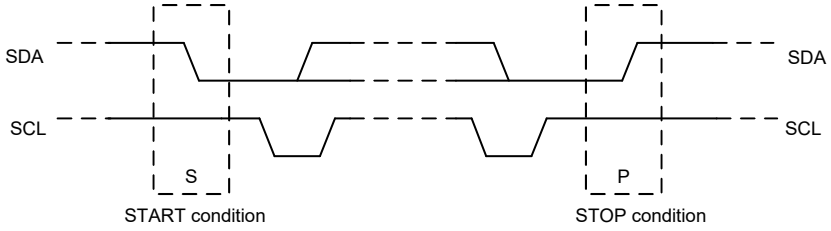
Data Validity

The data on the SDA line must be stable during the high period of the serial clock. The high or low state of the data line can only be changed when the clock signal on the SCL line is low as shown in the diagram.



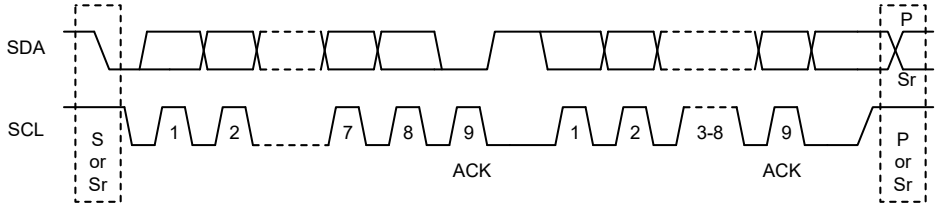
START and STOP Conditions

- A high to low transition on the SDA line while SCL is high defines a START condition.
- A low to high transition on the SDA line while SCL is high defines a STOP condition.
- START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.
- The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. In some respects, the START (S) and repeated START (Sr) conditions are functionally identical.



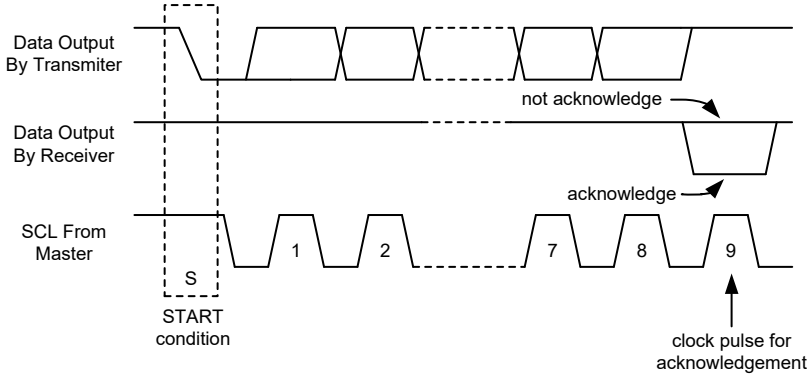
Byte Format

Every byte put on the SDA line must be 8-bit long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit, MSB, first.



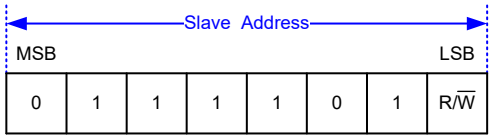
Acknowledge

- Each bytes of eight bits is followed by one acknowledge bit. The acknowledge bit is a low level placed on the bus by the receiver. The master generates an extra acknowledge related clock pulse.
- A slave receiver which is addressed must generate an acknowledge bit, ACK, after the reception of each byte.
- The devices that acknowledge must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the high period of this clock pulse.
- A master receiver must signal an end of data to the slave by generating a not-acknowledge, NACK, bit on the last byte that has been clocked out of the slave. In this case, the master receiver must leave the data line high during the 9th pulse to not acknowledge. The master will generate a STOP or repeated START condition.



Slave Addressing

- The slave address byte is the first byte received following the START condition form the master device. The first seven bits of the first byte make up the slave address. The eighth bit defines a read or write operation to be performed. When the R/$\overline{W}$ bit is "1", then a read operation is selected. A "0" selects a write operation.
- The devices address bits are "0111101". When an address byte is sent, the devices compare the first seven bits after the START condition. If they match, the devices output an acknowledge signal on the SDA line.

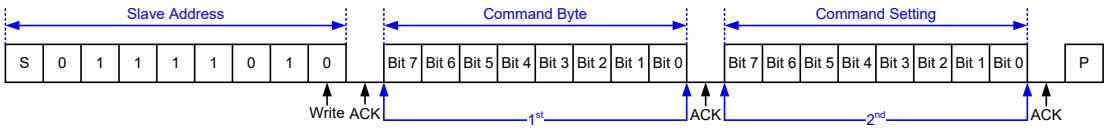


Write Operation

Byte Writes Operation

- **Command Byte**

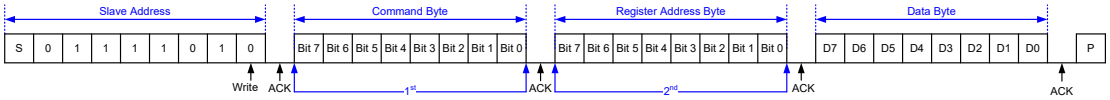
A Command Byte write operation requires a START condition, a slave address with an R/$\overline{W}$ bit, a command byte, a command setting byte and a STOP condition for a command byte write operation.



Command Byte Write Operation

- **Display RAM Single Data Byte**

A display RAM data byte write operation requires a START condition, a slave address with an R/$\overline{W}$ bit, a command byte, a valid Register Address byte, a Data byte and a STOP condition.

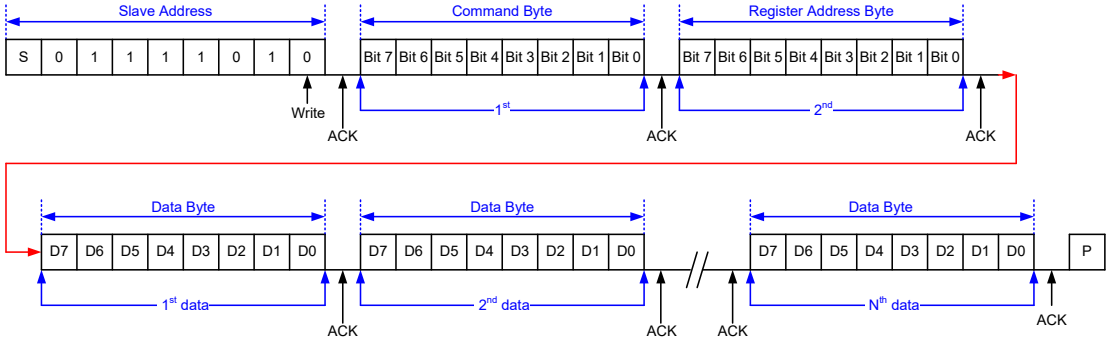


Display RAM Single Data Byte Write Operation

Note: If the byte following the slave address is a command code, the byte following the command code will be ignored.

Display RAM Page Write Operation

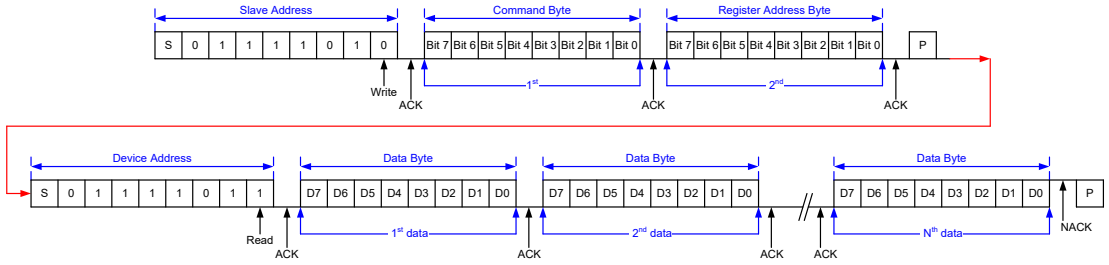
After a START condition the slave address with the R/$\overline{W}$ bit is placed on the bus followed with a command byte and the specified display RAM Register Address of which the contents are written to the internal address pointer. The data to be written to the memory will be transmitted next and then the internal address pointer will be incremented by 1 to indicate the next memory address location after the reception of an acknowledge clock pulse. After the internal address point reaches the maximum memory address, which is 23H for 1/4 duty drive mode, 43H for 1/8 duty drive mode or 77H for 1/16 duty drive mode, the address pointer will be reset to 00H.



N Bytes Display RAM Data Write Operation

Display RAM Read Operation

- In this mode, the master reads the devices data after setting the slave address. Following the R/$\overline{W}$ bit (="0") is an acknowledge bit, a command byte and the register address byte which is written to the internal address pointer. After the start address of the Read Operation has been configured, another START condition and the slave address transferred on the bus followed by the R/$\overline{W}$ bit (="1"). Then the MSB of the data which was addressed is transmitted first on the I^{2}C bus. The address pointer is only incremented by 1 after the reception of an acknowledge clock. That means that if the devices are configured to transmit the data at the address of A_{N+1}, the master will read and acknowledge the transferred new data byte and the address pointer is incremented to A_{N+2}. After the internal address pointer reaches the maximum memory address, which is 23H for 1/4 duty drive mode, 43H for 1/8 duty drive mode or 77H for 1/16 duty drive mode, the address pointer will be reset to 00H.
- This cycle of reading consecutive addresses will continue until the master sends a STOP condition.



Command Summary

Display Data Read/Write Command

This command can write data from MCU to memory MAP of the devices or can read from the devices.

Function	Byte	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Note	R/W	Def
Display Data Read/ Write Command	1st	1	0	0	0	0	0	0	0		W	80H
Address pointer	2nd	X	A6	A5	A4	A3	A2	A1	A0	Display data start address of memory map	W	00H
Display Write/Read Data	3th	D7	D6	D5	D4	D3	D2	D1	D0		R/W	

Note:
- Power-on status: the address is set to 00H.
- If the programmed command is not defined, the function will not be affected.
- For 1/4 duty drive mode after reaching the memory location 23H, the pointer will reset to 00H.
- For 1/8 duty drive mode after reaching the memory location 43H, the pointer will reset to 00H.
- For 1/16 duty drive mode after reaching the memory location 77H, the pointer will reset to 00H.

Drive Mode Command

This command controls the bias select and duty select.

Function	Byte	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Note	R/W	Def
Driver mode setting command	1st	1	0	0	0	0	0	1	0		W	82H
Duty and Bias setting	2nd	X	X	X	X	Duty1	Bias1	Duty0	Bias0		W	00H

Note:

Duty1	Duty0	Duty
0	0	1/4 duty
0	1	1/8 duty
1	X	1/16 duty

Bias1	Bias0	Bias
0	0	1/3 bias
0	1	1/4 bias
1	X	1/5 bias

- Power-on status: The drive mode 1/4 duty output and 1/3 bias is selected.
- If the programmed command is not defined, the function will not be affected.

System Mode Command

This command controls the internal system oscillator on/off and display on/off.

Function	Byte	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Note	R/W	Def
System mode setting command	1st	1	0	0	0	0	1	0	0		W	84H
System oscillator and Display on/off Setting	2nd	X	X	X	X	X	X	S	E		W	00H

Note:

Bit		Internal System Oscillator	LCD Display
S	E		
0	X	off	off
1	0	on	off
1	1	on	on

- Power-on status: Display off and disable the internal system oscillator.
- If the programmed command is not defined, the function will not be affected.

Frame Frequency Command

This command selects the frame frequency.

Function	Byte	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Note	R/W	Def
Frame frequency command	1st	1	0	0	0	0	1	1	0		W	86H
Frame frequency setting	2nd	X	X	X	X	X	X	X	F		W	00H

Note:

Bit	Frame Frequency
F	
0	80Hz
1	160Hz

- Power-on status: Frame frequency is set to 80Hz.
- If the programmed command is not defined, the function will not be affected.

Blinking Frequency Command

This command defines the blinking frequency of the display modes.

Function	Byte	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Note	R/W	Def
Blinking Frequency command	1st	1	0	0	0	1	0	0	0		W	88H
Blinking Frequency setting	2nd	X	X	X	X	X	X	BK1	BK0		W	00H

Note:

Bit		Blinking Frequency
BK1	BK0	
0	0	Blinking off
0	1	2Hz
1	0	1Hz
1	1	0.5Hz

- Power-on status: Blinking function is switched off.
- If the programmed command is not defined, the function will not be affected.

Internal Voltage Adjustment (IVA) Setting Command

The internal voltage (V_{LCD}) adjustment can provide sixteen kinds of regulator voltage adjustment options by setting the LCD operating voltage adjustment command.

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
IVA Command	1st	1	0	0	0	1	0	1	0		W	8AH
IVA Control	2nd	X	X	DE	VE	DA3	DA2	DA1	DA0	• The Segment/VLCD shared pin can be programmed via the "DE" bit. • The "VE" bit is used to enable or disable the internal voltage adjustment is supply voltage to bias voltage. • The DA3~DA0 bits can be used to adjust the V_{LCD} output voltage.	W	30H

Note:

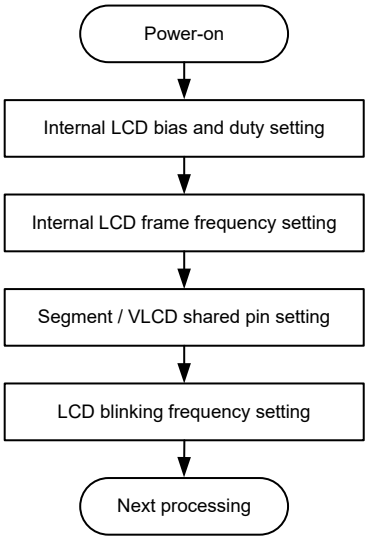
Bit		Segment 71/ VLCD shared Pin Select	Internal Voltage Adjustment	Note
DE	VE			
0	0	VLCD	off	• The bias voltage is supplied by the external VLCD pin when VCCA2 is connected to VLCD. • The bias voltage is supplied by the external VLCD pin when VCCA2 is connected to VDD. • If the VLCD pin is connected to the VDD pin, the internal voltage follower (OP4) must be disabled by setting the DA3~DA0 bits as "0000".
0	1	VLCD	on	• When VCCA2 is connected to VLCD, internal voltage adjustment can not be used to adjust internal bias voltage. (Bias voltage is supplied by the external VLCD pin) • When VCCA2 is connected to VDD, internal voltage adjustment can not be used to adjust internal bias voltage when VLCD pin is supplies with external voltage.(Recommend: can not be used) • When VCCA2 is connected to VDD, internal voltage adjustment can be used to adjust internal bias voltage when VLCD pin is floating and internal voltage adjustment is enable.(Bias voltage is supplied by the internal voltage adjustment)
1	0	Segment 71	off	• The bias voltage is supplied by the external VLCD pin when VCCA2 is connected to VLCD. • The bias voltage is supplied by the external VDD power when VCCA2 is connected to VDD. • The internal voltage-follower (OP4) is disabled automatically and DA3~DA0 don't care.
1	1	Segment 71	on	• When VCCA2 is connected to VLCD, internal voltage adjustment can be used to adjust internal bias voltage when VLCD pin is supplies with external voltage and internal voltage adjustment is enable. (Bias voltage is supplied by the internal voltage adjustment) • When VCCA2 is connected to VDD, internal voltage adjustment can be used to adjust internal bias voltage when internal voltage adjustment is enable.(Bias voltage is supplied by the internal voltage adjustment)

- Power-on status: Enable the internal voltage Adjustment and the Segment/VLCD pin is set as the segment pin.
- When the DA0~DA3 bits are set to "0000", the internal voltage-follower (OP4) is disabled. When the DA0~DA3 bits are set to other values except "0000", the internal voltage follower (OP4) is enabled.
- If the programmed command is not defined, the function will not be affected.

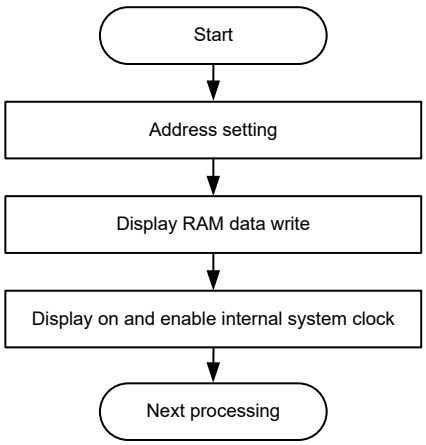
Operation Flow Chart

Access procedures are illustrated below by means of the flowcharts.

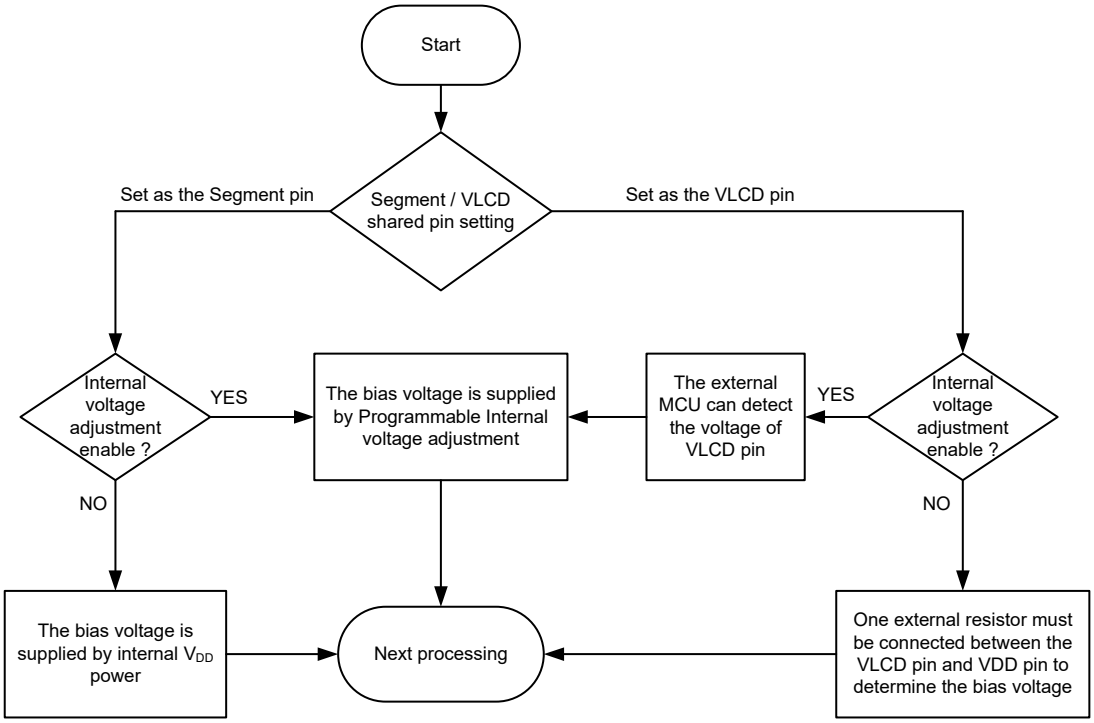
Initialization



Display Data Read/Write (Address Setting)



Segment/VLCD Shared Pin and Internal Voltage Adjustment Setting



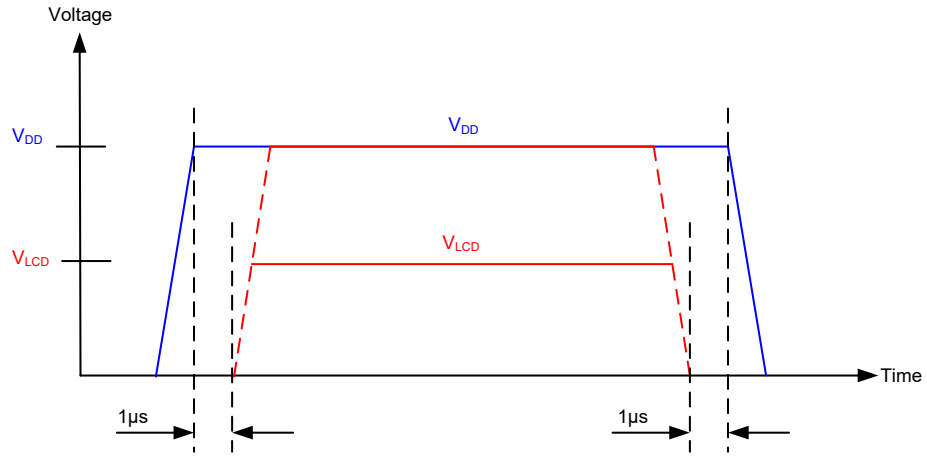
Power Supply Sequence

- If the power is individually supplied on the VLCD and VDD pins, it is strongly recommended to follow the Holtek power supply sequence requirement.
- If the power supply sequence requirement is not followed, it may result in malfunction.

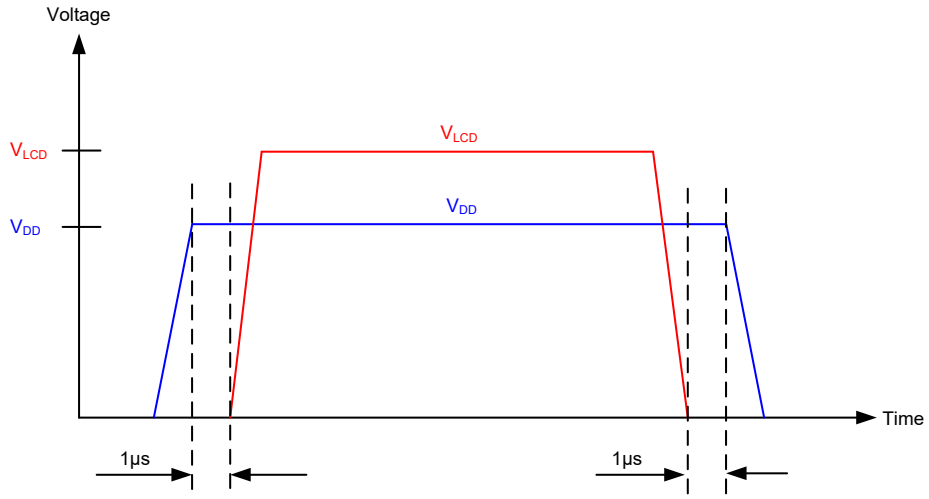
Holtek Power Supply Sequence Requirement:

1. Power-on sequence:
   Turn on the logic power supply V_{DD} first and then turn on the LCD driver power supply V_{LCD}.
2. Power-off sequence:
   Turn off the LCD driver power supply V_{LCD} first and then turn off the logic power supply V_{DD}.
3. The Holtek Power Supply Sequence Requirement must be followed no matter whether the V_{LCD} voltage is higher than the V_{DD} voltage.

- When the V_{LCD} voltage is less than or is equal to V_{DD} voltage application



- When the V_{LCD} voltage is greater than V_{DD} voltage application



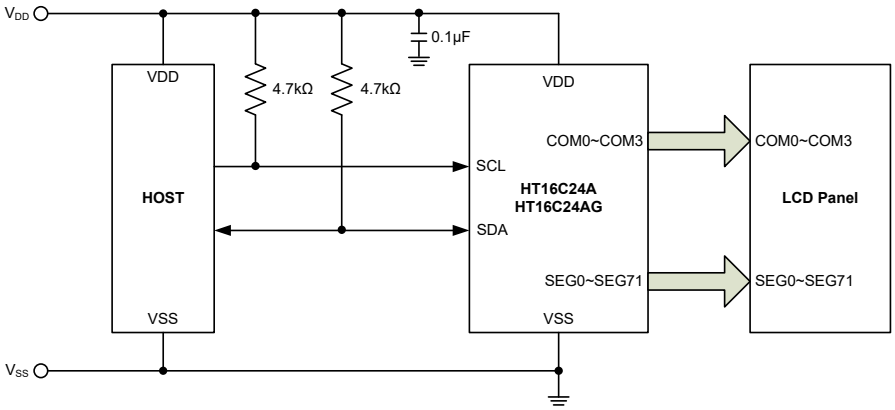
Application Circuits

Set as Segment Pin

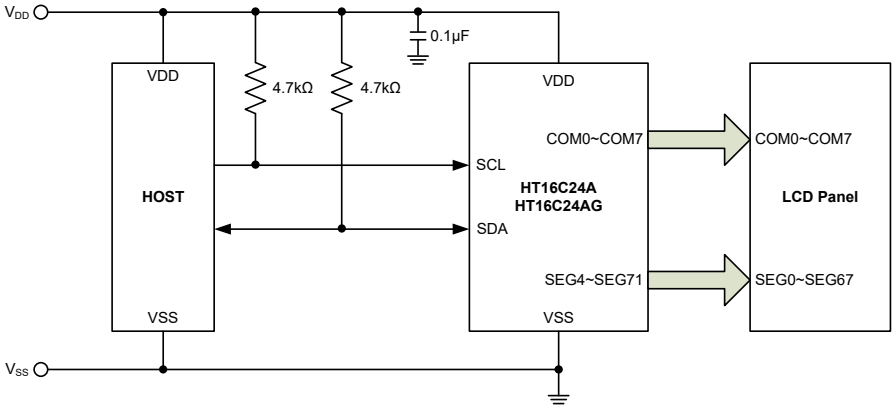
Case1

- Disable the internal V_{LCD} voltage adjustment.
- The bias voltage is supplied by internal V_{DD} power.

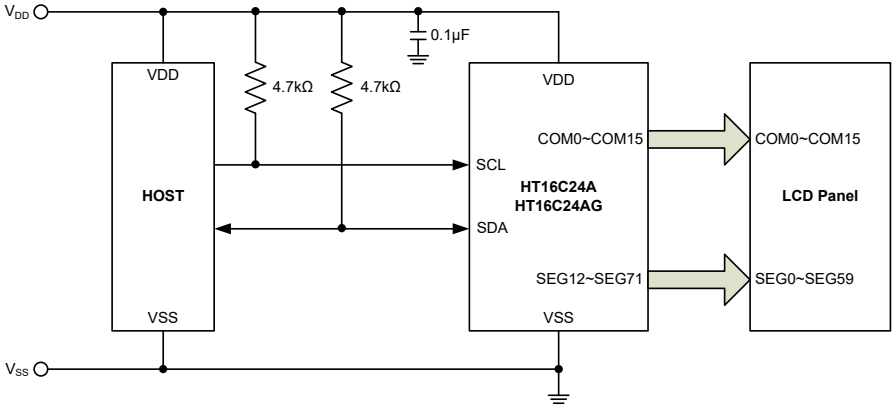
1/4 Duty (COM0~COM3, SEG0~SEG71)



1/8 Duty (COM0~COM7, SEG4~SEG71)



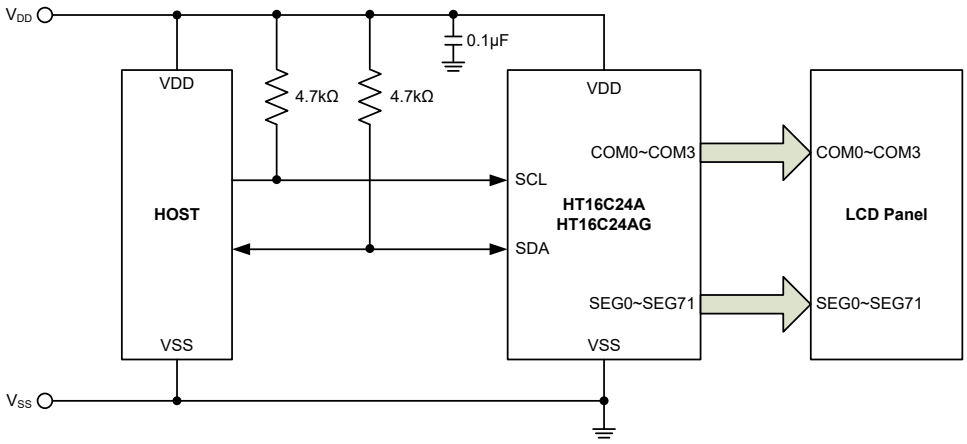
1/16 Duty (COM0~COM15, SEG12~SEG71)



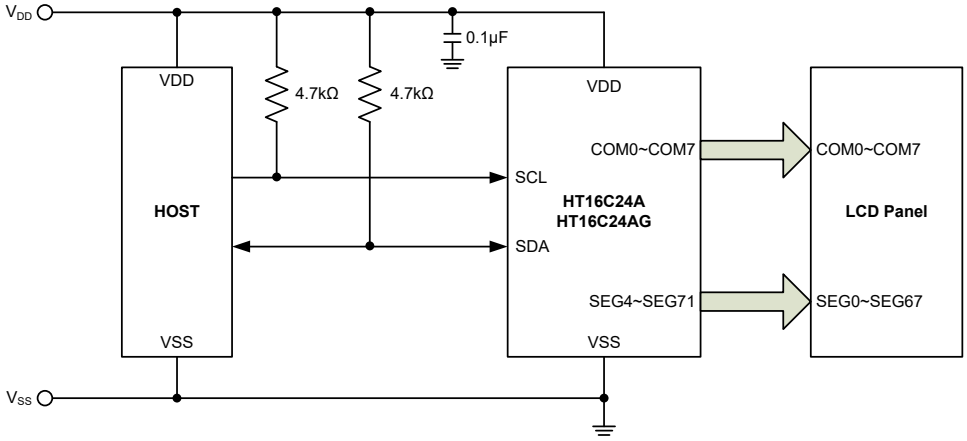
Case2

- Enable the internal V_{LCD} voltage adjustment.
- The bias voltage is supplied by internal V_{LCD} voltage adjustment power.

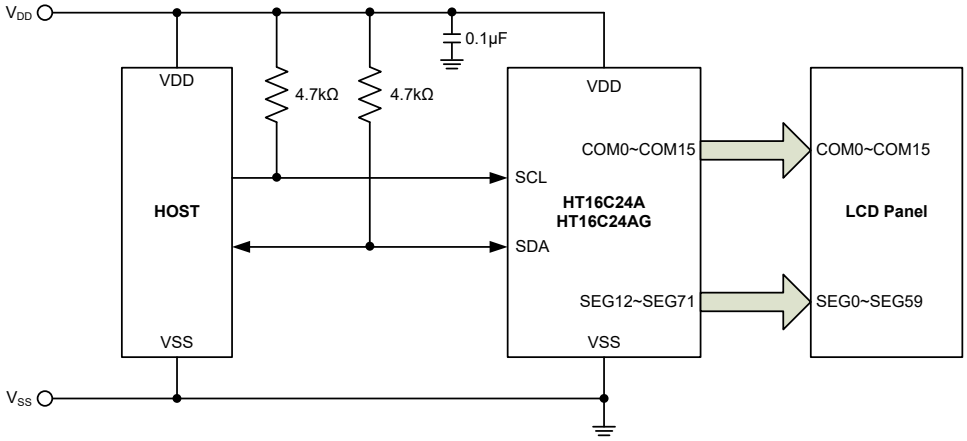
1/4 Duty (COM0~COM3, SEG0~SEG71)



1/8 Duty (COM0~COM7, SEG4~SEG71)



1/16 Duty (COM0~COM15, SEG12~SEG71)



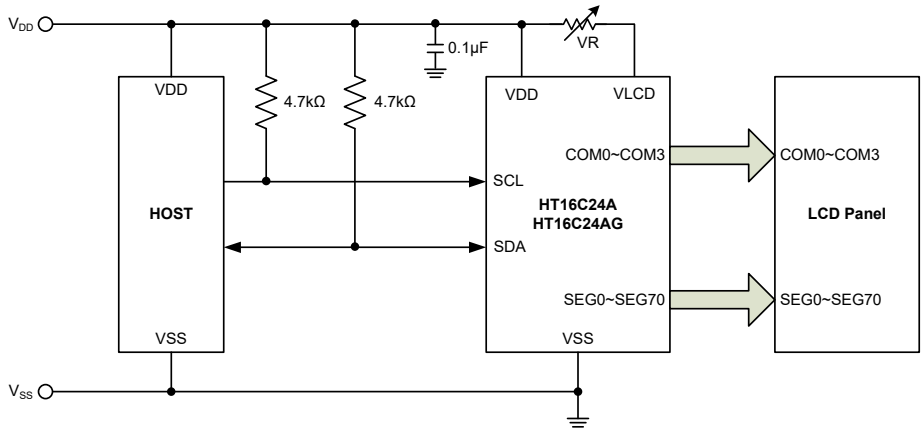
Set as VLCD Pin

Case1

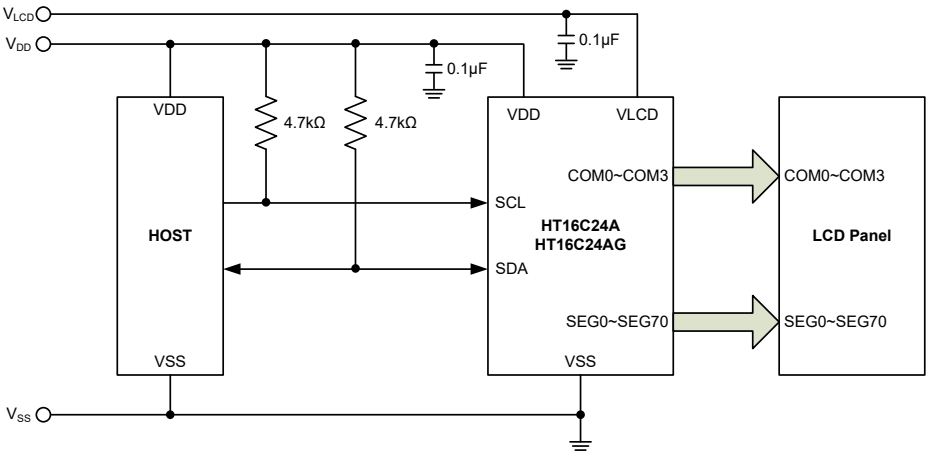
- Disable the internal V_{LCD} voltage adjustment.

1/4 Duty (COM0~COM3, SEG0~SEG70)

1. One external resister must be connected between VLCD pin and VDD pin to determine the bias voltage.

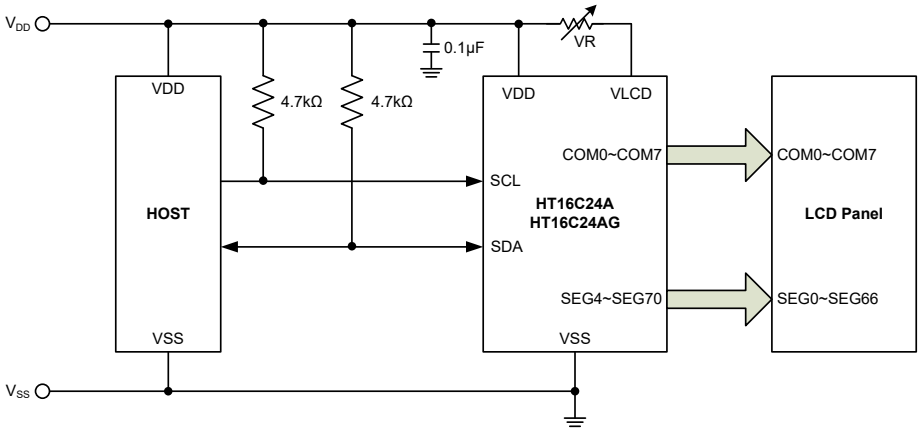


2. Support external V_{LCD} to determine the bias voltage.

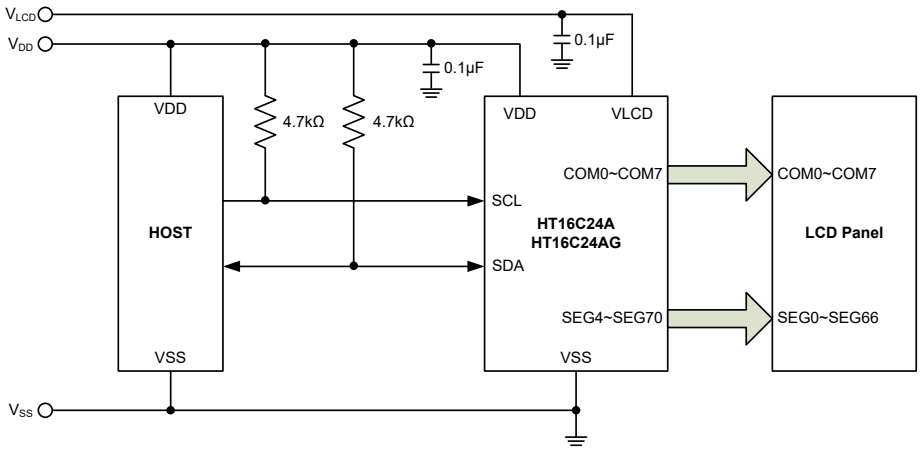


1/8 Duty (COM0~COM7, SEG4~SEG70)

1. One external resister must be connected between VLCD pin and VDD pin to determine the bias voltage.

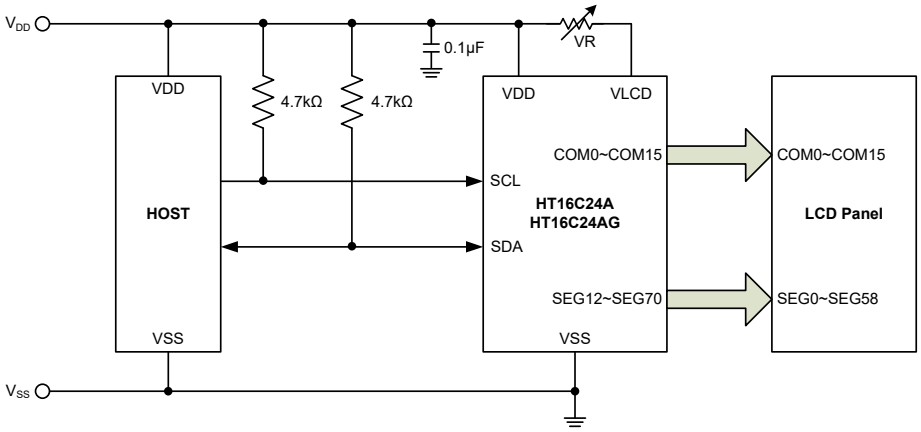


2. Support external V_{LCD} to determine the bias voltage.

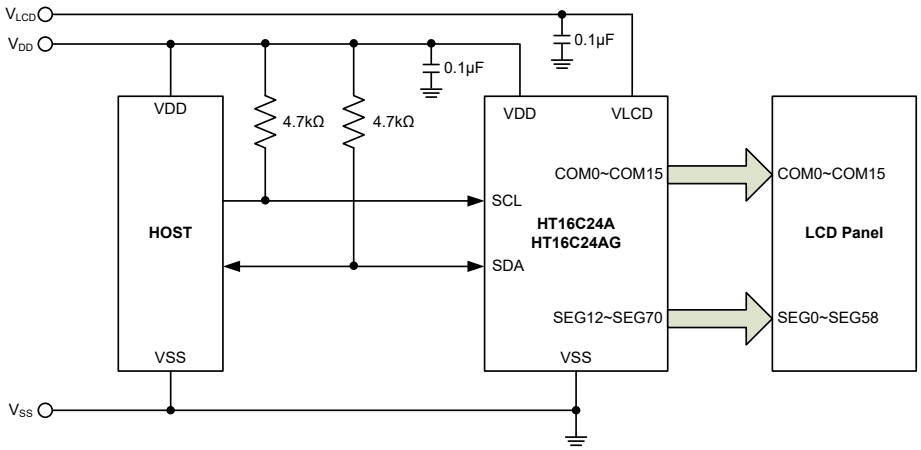


1/16 Duty (COM0~COM15, SEG12~SEG70)

1. One external resister must be connected between VLCD pin and VDD pin to determine the bias voltage.



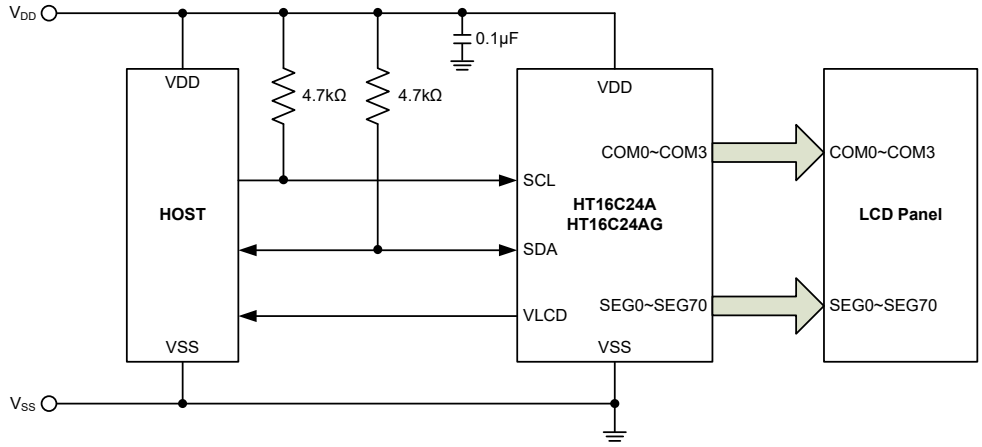
2. Support external V_{LCD} to determine the bias voltage.



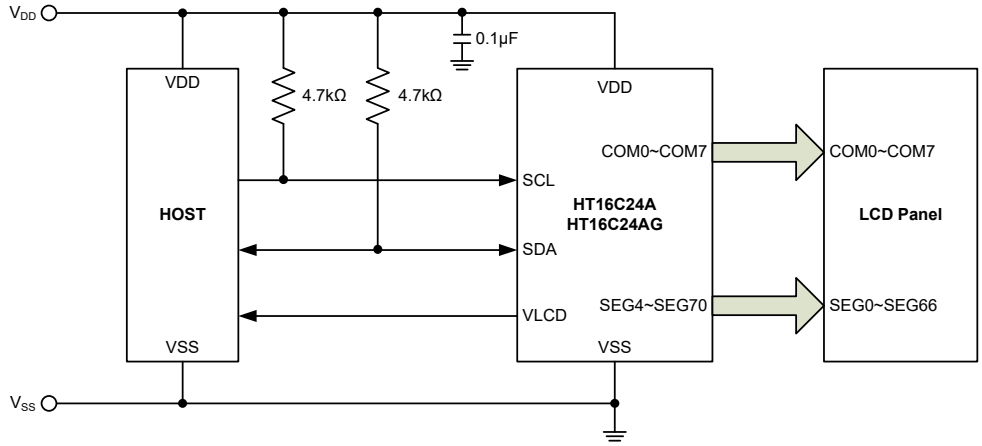
Case2

- Enable the internal VLCD voltage adjustment.
- The external MCU can detect the voltage of VLCD pin.

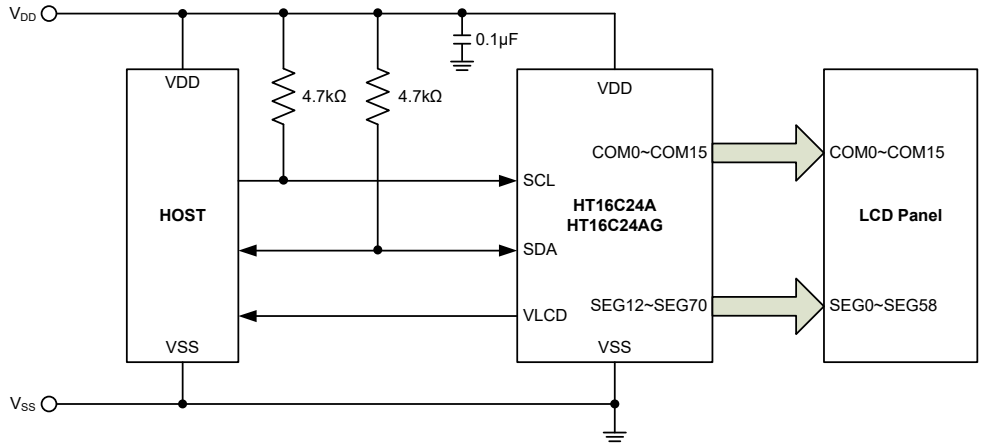
1/4 Duty (COM0~COM3, SEG0~SEG70)



1/8 Duty (COM0~COM7, SEG4~SEG70)



1/16 Duty (COM0~COM15, SEG12~SEG70)



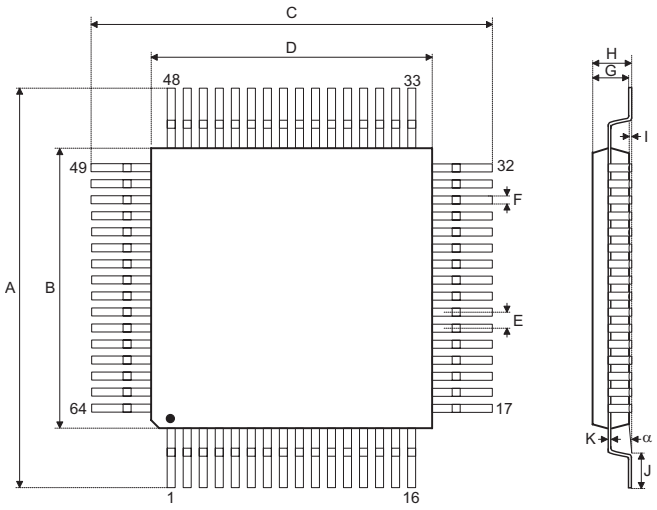
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

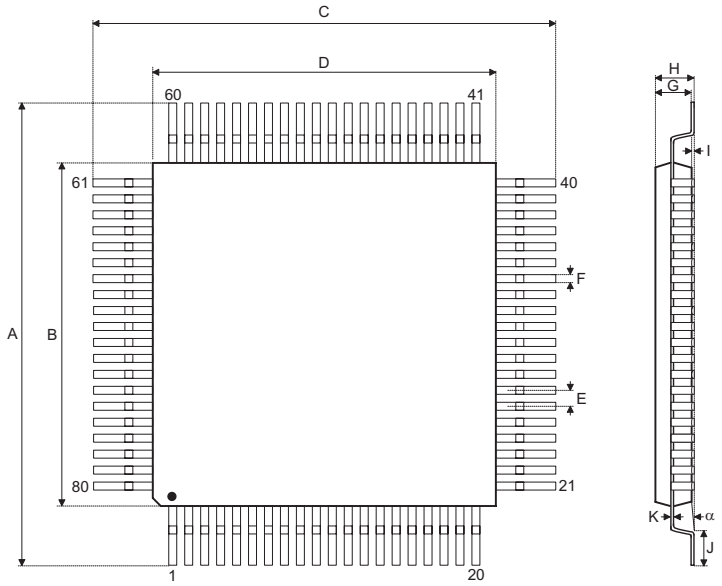
64-pin LQFP (7mm×7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.016 BSC	—
F	0.005	0.007	0.009
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.0 BSC	—
B	—	7.0 BSC	—
C	—	9.0 BSC	—
D	—	7.0 BSC	—
E	—	0.4 BSC	—
F	0.13	0.18	0.23
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

80-pin LQFP (10mm×10mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.472 BSC	—
B	—	0.394 BSC	—
C	—	0.472 BSC	—
D	—	0.394 BSC	—
E	—	0.016 BSC	—
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	12 BSC	—
B	—	10 BSC	—
C	—	12 BSC	—
D	—	10 BSC	—
E	—	0.4 BSC	—
F	0.13	0.18	0.23
G	1.35	1.4	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°