SENSYLINK Microelectronics

(CA9555V)

Low Voltage 16-bit I²C and SMBus I/O Expander with Interrupt

CA9555V is a 16-bit remote GPIO expander. It provides remote GPIO expansion for most MCU families via the I²C or SMBus interface.
It is ideally used in Server and Telecom equipment.

Table of Contents

Figures and Tables

Low Voltage 16-bit I²C and SMBus I/O Expander with Interrupt

1. Description

The chip is a 16-bit I/O expander. It provides remote GPIO expansion for most MCU families via the I²C or SMBus interface. The CA9555V has two 8-bit Input Port register, Output Port register, Configuration register (setup as input or output), and Polarity Inversion register (active high or active low). After power on, the 16 I/O pins are configured as inputs with an internal weak pull-up to V_{CC}. However, the master can enable the I/O pins as either inputs or outputs individually by setup the configuration register bits. If no external signals are applied to the CA9555V I/O pins, the voltage level is high due to the internal pull-up resistors. The data for each input or output is stored in the corresponding input or output port register. The polarity of the Input Port register can be inverted with the Polarity Inversion register.

The master can reset the chip probably caused by timeout or other improper operation using the power-on reset feature, which resets all registers in their default state and initializes the I²C/SMBus state machine. The chip has outputs latch feature, which can protect the chip when driving LEDs directly with high-current capability.

The CA9555V open-drain interrupt output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed.

Available Package: TSSOP-24, QFN4x4-24A package.

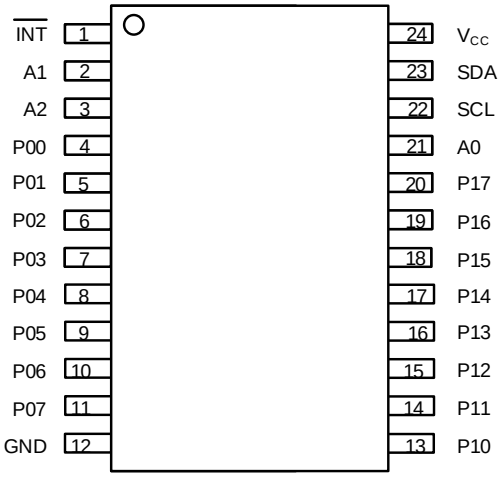
2. Features

- Operation Voltage: 1.65V to 5.5V
- Standby Current: 3.5μA (Max. 5.5V)
- 5.5V Tolerance I/O Port
- Remote 16-bit GPIO Expander
- Compatible with SMBus and I²C interface
- I²C Speed up to 1.0MHz (Fast-mode Plus)
- Up to 8 slave addresses
- Open-drain Interrupt output with active low to indicate input state changed.
- Input, Output, and Configuration Register
- Polarity Inversion Register
- Built-in Power-on Reset
- No Glitch during Power-up
- Noise Filter on SCL/SDA inputs
- 16 I/O pins
  - As Input with internal 100k pull-up resistor (default)
  - As Output with internal push-pull
- Latch feature when driving LEDs directly with high current capability
- Temperature Range: -40°C to 85°C

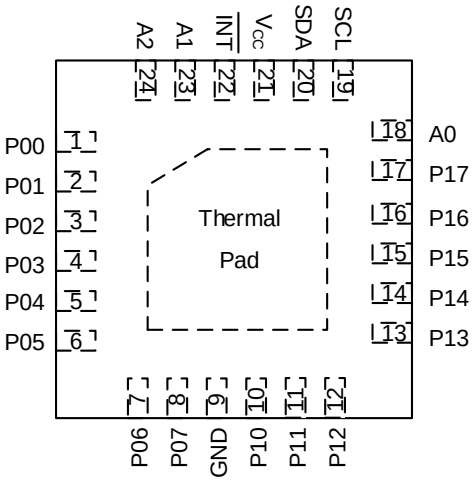
3. Applications

- Server, Notebook PC
- Telecom equipment
- Products with GPIO-Limited Processors
- Industrial Automation Equipment

4. PIN Configurations (Top View)

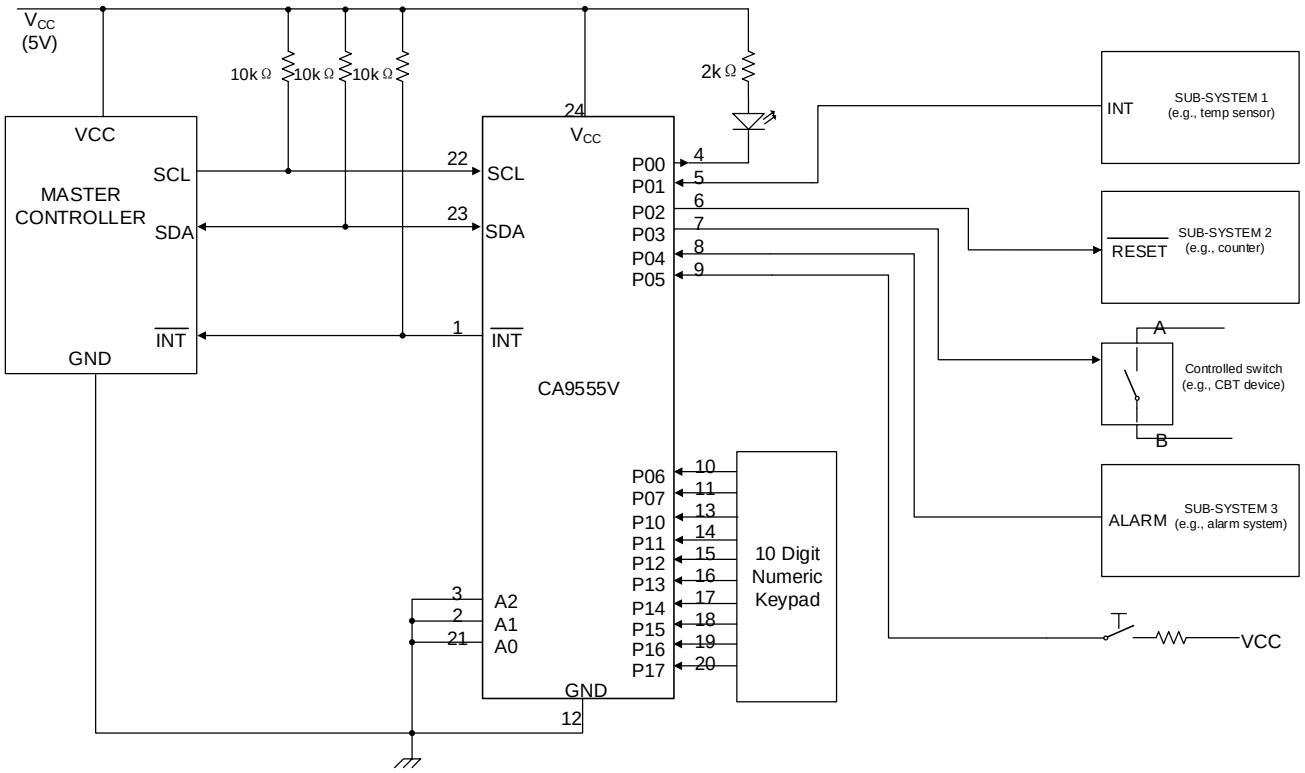


TSSOP-24 (Package Code MT)



QFN4x4-24A(Package Code QN)

5. Typical Application



A. Device address configured as 0100 000xb for this example.
B. P00,P02, P03 configured as outputs.
C. P01, P04-P07, and P10-P17 configured as inputs.
D. Pin numbers shown are for the MT package.

Figure 1. Typical Application of CA9555V

6. Pin Description

PIN Name	PIN No.		Description
	TSSOP-24	QFN4x4-24A	
$\overline{INT}$	1	22	Interrupt output with active low. Connect to VCC through a pull-up resistor.
A1	2	23	Slave addresses setup pin1, combined with A0, A2, which can generate 8 kinds of slave addresses by connecting these pins to GND or V_{CC} respectively.
A2	3	24	Slave addresses setup pin2, combined with A0, A1, which can generate 8 kinds of slave addresses by connecting these pins to GND or V_{CC} respectively.
P00	4	1	GPIO bit0 of Port0, output: push-pull structure; input: internal weakly pull-up structure.
P01	5	2	GPIO bit1 of Port0, output: push-pull structure; input: internal weakly pull-up structure.
P02	6	3	GPIO bit2 of Port0, output: push-pull structure; input: internal weakly pull-up structure.
P03	7	4	GPIO bit3 of Port0, output: push-pull structure; input: internal weakly pull-up structure.
P04	8	5	GPIO bit4 of Port0, output: push-pull structure; input: internal weakly pull-up structure.
P05	9	6	GPIO bit5 of Port0, output: push-pull structure; input: internal weakly pull-up structure.
P06	10	7	GPIO bit6 of Port0, output: push-pull structure; input: internal weakly pull-up structure.
P07	11	8	GPIO bit7 of Port0, output: push-pull structure; input: internal weakly pull-up structure.
GND	12	9	Ground pin.
P10	13	10	GPIO bit0 of Port1, output: push-pull structure; input: internal weakly pull-up structure.
P11	14	11	GPIO bit1 of Port1, output: push-pull structure; input: internal weakly pull-up structure.
P12	15	12	GPIO bit2 of Port1, output: push-pull structure; input: internal weakly pull-up structure.
P13	16	13	GPIO bit3 of Port1, output: push-pull structure; input: internal weakly pull-up structure.
P14	17	14	GPIO bit4 of Port1, output: push-pull structure; input: internal weakly pull-up structure.
P15	18	15	GPIO bit5 of Port1, output: push-pull structure; input: internal weakly pull-up structure.
P16	19	16	GPIO bit6 of Port1, output: push-pull structure; input: internal weakly pull-up structure.
P17	20	17	GPIO bit7 of Port1, output: push-pull structure; input: internal weakly pull-up structure.
A0	21	18	Slave addresses setup pin0, combined with A1, A2, which can generate 8 kinds of slave addresses by connecting these pins to GND or V_{CC} respectively.
SCL	22	19	Digital interface clock input pin, need a pull-up resistor to V_{CC}.
SDA	23	20	Digital interface data input or output pin, need a pull-up resistor to V_{CC}.
V_{CC}	24	21	Power supply input pin, using 0.1uF low ESR ceramic capacitor to ground

7. Function Block

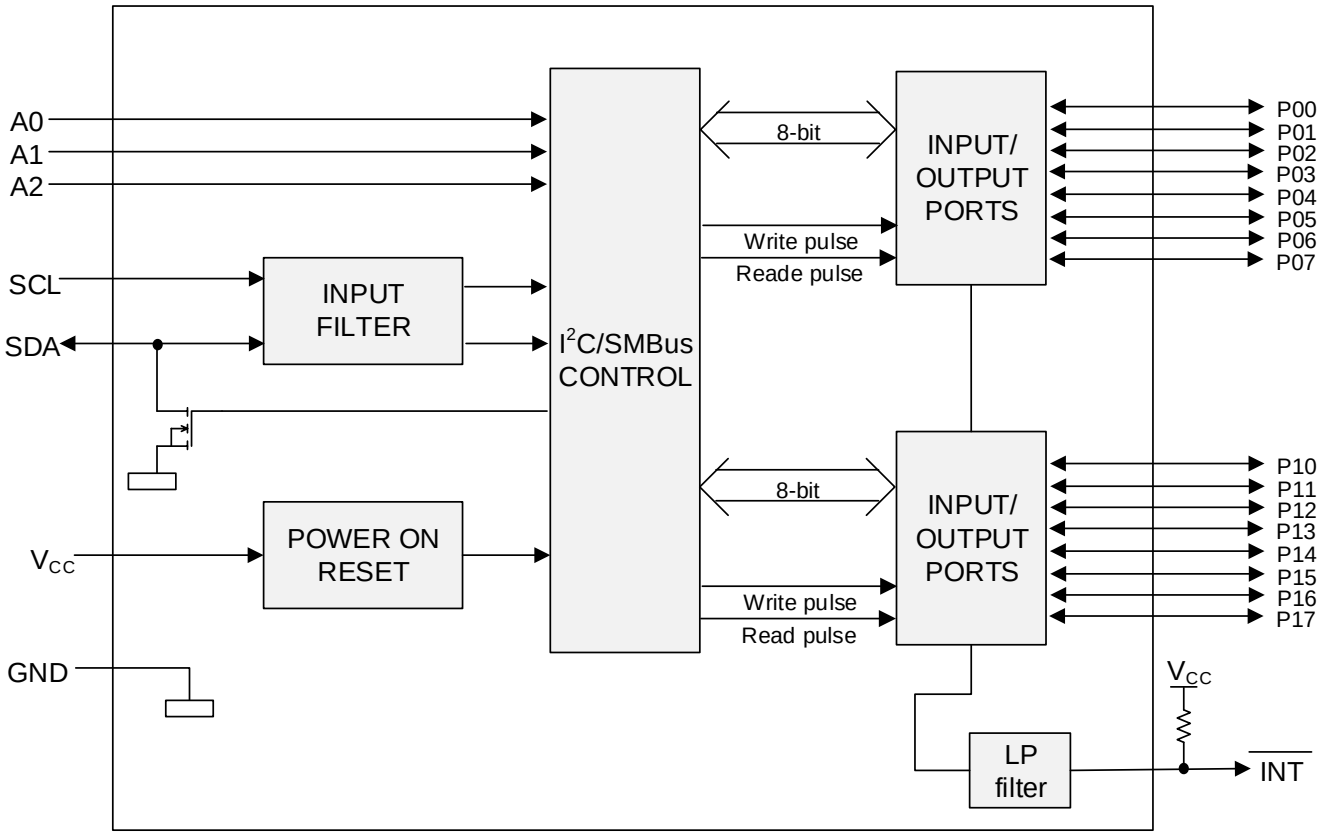
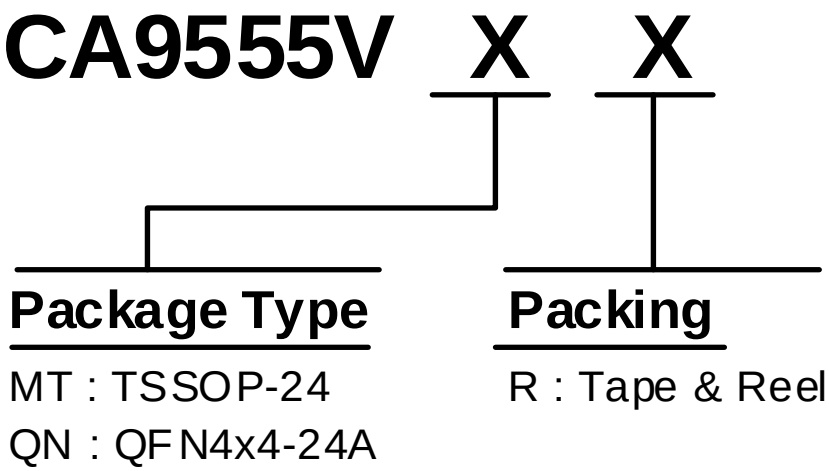


Figure 2. CA9555V function block

8. Ordering Information



Order PN	Green[1]	Package	Marking ID[2]	Packing	MPQ	Operation Temperature
CA9555VMTR	Halogen free	TSSOP-24	9555V YWWAXX	Tape & Reel	4,000	-40°C ~ +85°C
CA9555VQNR	Halogen free	QFN4x4-24A	9555V YWWAXX	Tape & Reel	5,000	-40°C ~ +85°C

Note

1. Based on ROHS Y2012 spec, Halogen free covers lead free. So, most package types Sensylink offers only states halogen free, instead of lead free.
2. Marking ID includes 2 rows of characters. In general, the 1st row of characters is part number, and the 2nd row of characters are date code plus production information.

9. Specification

9.1. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC} to GND	-0.5 to 6	V
SDA, SCL, P00-P17 Voltage	V_{SDA}/V_{SCL}/V_{P00-17} to GND	-0.5 to 6	V
A0 - A2 Voltage	V_{A0}/V_{A1}/V_{A2} to GND	-0.5 to 6	V
$\overline{INT}$ Voltage	V_{INT} to GND	-0.5 to 6	V
P00-P17 Output Current		±50	mA
Storage temperature Range	T_{STG}	-65 to 150	ºC
Lead Temperature (Soldering, 10 Seconds)	T_{LEAD}	260	ºC
Junction Temperature	$T_{j\ (max)}$	125	ºC
ESD MM	ESD_{MM}	±200	V
ESD HBM	ESD_{HBM}	±4000	V
ESD CDM	ESD_{CDM}	±1000	V

Note

1) Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at the "Absolute Maximum Ratings" conditions or any other conditions beyond those indicated under "Recommended Operating Conditions" is not recommended. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

9.2. Recommended Operating Conditions

Parameter	Symbol	Condition	Min	Max	Unit
Supply Voltage	V_{CC}		1.65	5.5	V
High-level input voltage	V_{IH}	SCL, SDA	0.7×V_{CC}	V_{CC} (1)	V
		A2–A0, P07–P00, P17–P10	0.7×V_{CC}	5.5	V
Low-level input voltage	V_{IL}	SCL, SDA	-0.5	0.3×V_{CC}	V
		A2–A0, P07–P00, P17–P10	-0.5	0.3×V_{CC}	V
High-level output current	I_{OH}	P07–P00, P17–P10		-10	mA
Low-level output current	I_{OL}	V_{OL}=0.4V P07–P00, P17–P10		25	mA
		V_{OL}=0.4V $\overline{INT}$, SDA		25	mA
Ambient Operation Temperature Range	T_A		-40	+85	°C

Note

1) For voltages applied above V_{CC}, an increase in I_{CC} will result.

9.3. Electrical Characteristics

Test Conditions: C_{IN} = 0.1uF, V_{CC} = 1.65V to 5.5V, T_A = -40 to 85°C unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ (1)	Max	Unit
Supply Voltage	V_{CC}		1.65		5.5	V
Supply Current	I_{CC}	V_{CC} = 5.5 V; no load; IO floating f_{SCL} = 400 kHz		35	50	μA
		V_{CC} = 3.6 V; no load; IO floating f_{SCL} = 400 kHz		20	30	μA
		V_{CC} = 2.7 V; no load; IO floating f_{SCL} = 400 kHz		13	19	μA
		V_{CC} = 1.65 V; no load; IO floating f_{SCL} = 400 kHz		8	11	μA
Standby current	I_{STB}	V_{CC} = 5.5 V; no load; VI = GND; f_{SCL} = 0 kHz; I/O = inputs		0.8	1.5	mA
		V_{CC}= 3.6 V; no load; VI = GND; f_{SCL} = 0 kHz; I/O = inputs		0.6	1.3	mA
		V_{CC} = 2.7 V; no load; VI = GND; f_{SCL} = 0 kHz; I/O = inputs		0.42	1.0	mA
		V_{CC} = 1.65 V; no load; VI = GND; f_{SCL} = 0 kHz; I/O = inputs		0.25	0.9	mA
		V_{CC} = 5.5 V; no load; VI = V_{CC}; f_{SCL} = 0 kHz; I/O = inputs		1.0	3.5	μA
		V_{CC} = 3.6 V; no load; VI = V_{CC}; f_{SCL} = 0 kHz; I/O = inputs		0.7	1.8	μA
		V_{CC} = 2.7 V; no load; VI = V_{CC}; f_{SCL} = 0 kHz; I/O = inputs		0.5	1.6	μA
		V_{CC} = 1.65 V; no load; VI = V_{CC}; f_{SCL} = 0 kHz; I/O = inputs		0.2	1.0	μA
Power-on reset voltage	V_{POR}	no load; VI = V_{CC} or GND		1.4	1.55	V
High-level input voltage	V_{IH}	SCL, SDA	0.7×V_{CC}		V_{CC} (2)	V
		A2–A0, P07–P00, P17–P10	0.7×V_{CC}		5.5	V
Low-level input voltage	V_{IL}	SCL, SDA	-0.5		0.3×V_{CC}	V
		A2–A0, P07–P00, P17–P10	-0.5		0.3×V_{CC}	V
P-port high-level output voltage (3)	V_{OH}	I_{OH} = -8 mA; V_{CC} = 1.65 V	1.2			V
		I_{OH} = -10 mA; V_{CC} = 1.65 V	1.0			V
		I_{OH} = -8 mA; V_{CC} = 2.3 V	1.8			V
		I_{OH} = -10 mA; V_{CC} = 2.3 V	1.7			V
		I_{OH} = -8 mA; V_{CC} = 3.0 V	2.6			V
		I_{OH} = -10 mA; V_{CC} = 3.0 V	2.5			V
		I_{OH} = -8 mA; V_{CC} = 4.75 V	4.1			V
		I_{OH} = -10 mA; V_{CC} = 4.75 V	4.0			V
Low-level output current	I_{OL}	SDA V_{OL} = 0.4 V	3			mA
		P port (4) V_{OL} = 0.5 V	8			mA
		P port (4) V_{OL} = 0.7 V	10			mA
		$\overline{INT}$ V_{OL} = 0.4 V	3			mA

Electrical Characteristics (continued)

Parameter	Symbol	Test Conditions	Min	Typ (1)	Max	Unit
Input high leakage current	I_{IH}	P port; V_I = V_{CC}; V_{CC} = 1.65 V to 5.5 V			1	μA
Input low leakage current	I_{IL}	P port; V_I = GND; V_{CC} = 1.65 V to 5.5 V			-100	μA
Input capacitance	C_I	SCL; VI = V_{CC} or GND V_{CC} = 1.65 V to 5.5 V		3		pF
Input-output pin capacitance	C_{IO}	SDA; VI = V_{CC} or GND V_{CC} = 1.65 V to 5.5 V		3		pF
		P port; VI = V_{CC} or GND V_{CC} = 1.65 V to 5.5 V		3.7		pF
Input leakage current	I_I	V_{CC} = 1.65 V to 5.5 V SCL, SDA; VI = V_{CC} or GND			±1	μA
		V_{CC} = 1.65 V to 5.5 V A0, A1, A2; VI = V_{CC} or GND			±1	μA

Note:
(1) All typical values are at nominal supply voltage (1.8-, 2.5-, 3.3-, or 5-V V_{CC}) and T_A = 25°C.
(2) For voltages applied above V_{CC}, an increase in I_{CC} results.
(3) Each I/O must be externally limited to a maximum of 25 mA, and each octal (P07–P00 and P17–P10) must be limited to a maximum current of 100 mA, for a device total of 200 mA.
(4) The total current sourced by all I/Os must be limited to 160 mA (80 mA for P07–P00 and 80 mA for P17–P10).

9.4. Switching Characteristics

over recommended operating free-air temperature range, $C_L \leqslant$ 100 pF (unless otherwise noted).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Interrupt valid time	t_{IV}	From P port to $\overline{INT}$			4	us
Interrupt reset delay time	t_{IR}	From SCL to $\overline{INT}$			4	us
Output data valid; For V_{CC} = 2.3 V–5.5 V	t_{PV}	From SCL to P port			200	ns
Output data valid; For V_{CC} = 1.65 V–2.3 V					300	ns
Input data setup time	t_{PS}	From P port to SCL	150			ns
Input data hold time	t_{PH}	From P port to SCL	1			us

9.5. I²C Interface Timing Requirements

Over recommended operating free-air temperature range (unless otherwise noted).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
I²C clock frequency	f_{SCL}	Standard-mode	0		100	kHz
		Fast-mode (1)	0		400	kHz
		Fast-mode Plus (2)	0		1000	kHz
I²C bus free time between stop and start	t_{BUF}	Standard-mode	4.7			us
		Fast-mode	1.3			us
		Fast-mode Plus	0.5			us
I²C start or repeated start condition hold	$t_{HD:STA}$	Standard-mode	4.0			us
		Fast-mode	0.6			us
		Fast-mode Plus	0.26			us
I²C start or repeated start condition setup	$t_{SU:STA}$	Standard-mode	4.7			us
		Fast-mode	0.6			us
		Fast-mode Plus	0.26			us
I²C stop condition setup	$t_{SU:STO}$	Standard-mode	4.0			us
		Fast-mode	0.6			us
		Fast-mode Plus	0.26			us
Valid data time of ACK condition (ACK signal from SCL low to SDA (out) low)	$t_{VD:ACK}$	Standard-mode			3.45	us
		Fast-mode			0.9	us
		Fast-mode Plus			0.45	us
I²C serial-data hold time	$t_{HD:DAT}$	Standard-mode	0			us
		Fast-mode	0			us
		Fast-mode Plus	0			us
I²C Valid data time (SCL low to SDA output valid)	$t_{VD:DAT}$	Standard-mode			3.45	us
		Fast-mode			0.9	us
		Fast-mode Plus			0.45	us
I²C serial-data setup time	$t_{SU:DAT}$	Standard-mode	250			ns
		Fast-mode	100			ns
		Fast-mode Plus	50			ns
I²C clock low time	t_{LOW}	Standard-mode	4.7			us
		Fast-mode	1.3			us
		Fast-mode Plus	0.5			us
I²C clock high time	t_{HIGH}	Standard-mode	4.0			us
		Fast-mode	0.6			us
		Fast-mode Plus	0.26			us
I²C input fall time	t_F	Standard-mode			300	ns
		Fast-mode			300	ns
		Fast-mode Plus			120	ns

I²C Interface Timing Requirements (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
I²C output fall time (SDA out, 4.7kΩ R_{pull} ,10-pF to 400-pF bus)	t_{OF}	Standard-mode			300	ns
		Fast-mode			300	ns
		Fast-mode Plus			120	ns
I²C input rise time	t_R	Standard-mode			1000	ns
		Fast-mode			300	ns
		Fast-mode Plus			120	ns
I²C spike time	t_{SP}	Standard-mode			50	ns
		Fast-mode			50	ns
		Fast-mode Plus			50	ns

Note:
(1) In Fast-mode, the external pull-up resistance of SDA and SCL is typically 4.7 kOhm.
(2) In Fast-mode Plus, the external pull-up resistance of SDA and SCL is typically 0.51kOhm.

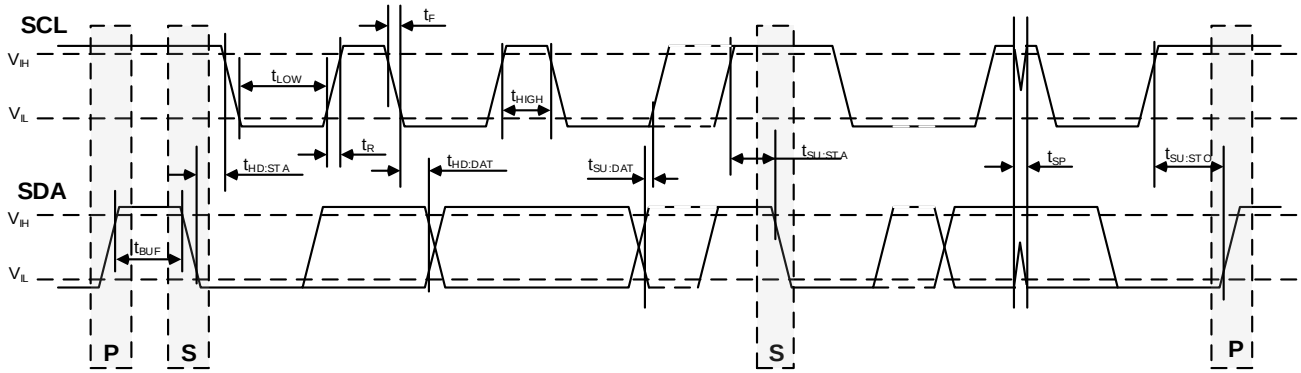


Figure 3. Definition of timing on the I²C-bus (part A)

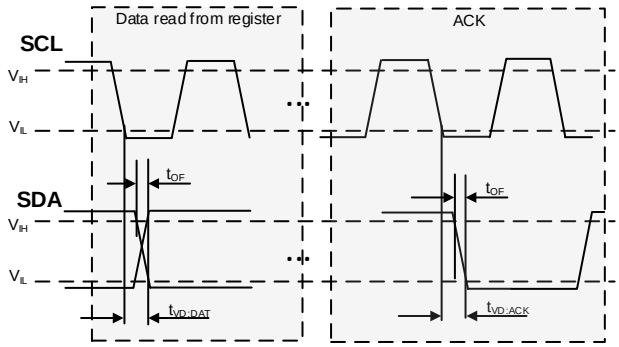


Figure 4. Definition of timing on the I²C-bus (part B)

10. Function Descriptions

The CA9555V is a 16-bit I/O expander for the two-line bidirectional bus (I^2C) is designed for 1.65-V to 5.5-V V_{CC} operation. It provides general-purpose remote I/O expansion for most microcontroller families via the I^2C interface. One of the features of the CA9555V, is that the $\overline{INT}$ output can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I^2C bus. Thus, the CA9555V can remain a simple slave device.

10.1. Device address

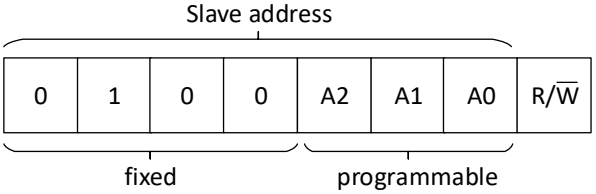


Figure 5. CA9555V device address

A2, A1 and A0 are the hardware address package pins and are held to either HIGH (logic 1) or LOW (logic 0) to assign one of the 8 possible slave addresses. The last bit of the slave address (R/W) defines the operation (read or write) to be performed. A HIGH (logic 1) selects a read operation, while a LOW (logic 0) selects a write operation.

10.2. Registers

10.2.1. Command byte

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

Table 1. Command byte

Command	Access	Default value	Description
0x00	Read only	XX (1)	Input port 0
0x01	Read only	XX (1)	Input port 1
0x02	Read or Write	0xFF	Output port 0
0x03	Read or Write	0xFF	Output port 1
0x04	Read or Write	0x00	Polarity Inversion port 0
0x05	Read or Write	0x00	Polarity Inversion port 1
0x06	Read or Write	0xFF	Configuration port 0
0x07	Read or Write	0xFF	Configuration port 1

Note: (1) XX is not care.

10.2.2. Registers 0 and 1: Input port registers

This register is an input-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

The default value 'X' is determined by the externally applied logic level.

Table 2. Input port 0 Register (register 0, 0x00)

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

Table 3. Input port 1 Register (register 1, 0x01)

Bit	7	6	5	4	3	2	1	0
Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

10.2.3. Registers 2 and 3: Output port registers

This register is an output-only port. It reflects the outgoing logic levels of the pins defined as outputs by Registers 6 and 7. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Table 4. Output port 0 Register (register 2, 0x02)

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

Table 5. Output port 1 Register (register 3, 0x03)

Bit	7	6	5	4	3	2	1	0
Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

10.2.4. Registers 4 and 5: Polarity Inversion registers

This register allows the user to invert the polarity of the Input port register data. If a bit in this register is set (written with '1'), the Input port data polarity is inverted. If a bit in this register is cleared (written with a '0'), the Input port data polarity is retained.

Table 6. Polarity Inversion port 0 register (register 4, 0x04)

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

Table 7. Polarity Inversion port 1 register (register 5, 0x05)

Bit	7	6	5	4	3	2	1	0
Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

10.2.5. Registers 6 and 7: Configuration registers

This register configures the directions of the I/O pins. If a bit in this register is set (written with '1'), the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared (written with '0'), the corresponding port pin is enabled as an output. Note that there is a high value resistor tied to V_{CC} at each pin. At reset, the device's ports are inputs with a pull-up to V_{CC}.

Table 8. Configuration port 0 register (register 6, 0x06)

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

Table 9. Configuration port 1 register (register 7, 0x07)

Bit	7	6	5	4	3	2	1	0
Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

10.3. Power-on reset

When power is applied to V_{CC}, an internal power-on reset holds the CA9555V in a reset condition until V_{CC} has reached V_{POR}. At that point, the reset condition is released and the CA9555V registers and SMBus state machine will initialize to their default states. The power-on reset typically completes the reset and enables the part by the time the power supply is above V_{POR}.

10.4. Interrupt output

The open-drain interrupt output is activated when one of the port pins changes states and the pin is configured as an input. The interrupt is deactivated when the input returns to its previous state or the Input Port register is read (see Figure 10). A pin configured as an output cannot cause an interrupt. Since each 8-bit port is read independently, the interrupt caused by Port 0 will not be cleared by a read of Port 1 or the other way around.

Remark: Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

11. I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input with a weak pull-up to V_{CC}. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.

If the I/O is configured as an output, then either Q1 or Q2 is on, depending on the state of the Output Port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low-impedance path that exists between the pin and either V_{CC} or GND.

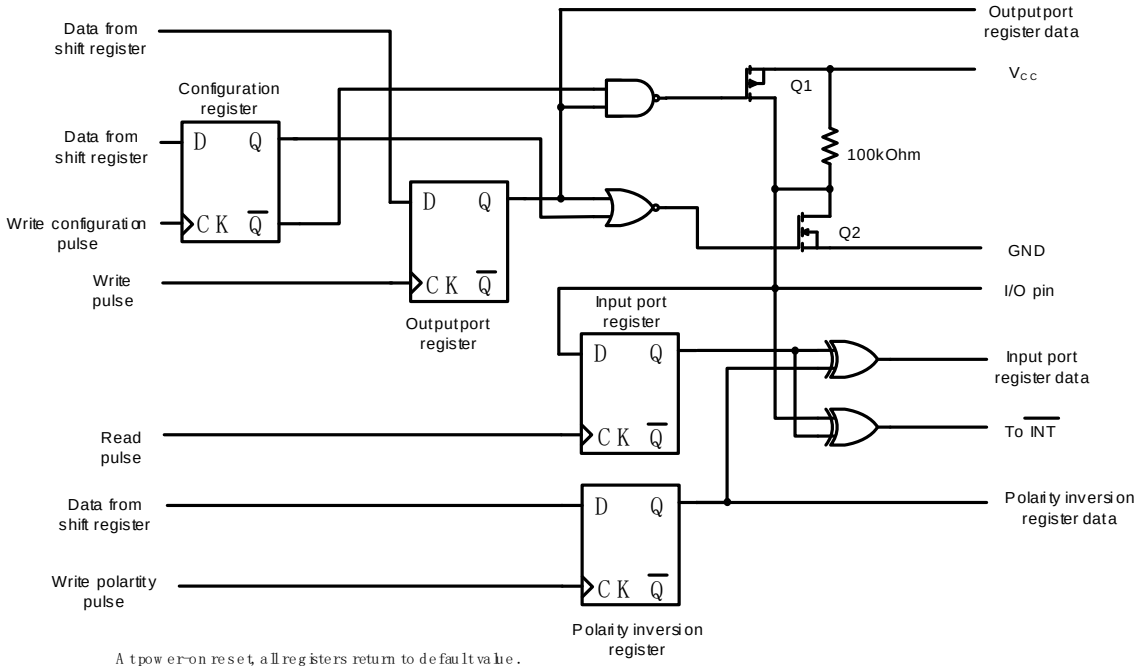


Figure 6. Simplified schematic of I/Os

11.1. Bus transactions

11.1.1. Writing to the port registers

Data is transmitted to the CA9555V by sending the device address and setting the least significant bit to a logic 0 (see Figure 5 “CA9555V device address”). The command byte is sent after the address and determines which register will receive the data following the command byte.

The eight registers within the CA9555V are configured to operate as four register pairs. The four pairs are Input Ports, Output Ports, Polarity Inversion Ports, and Configuration Ports. After sending data to one register, the next data byte will be sent to the other register in the pair (see Figure 7 and Figure 8). For example, if the first byte is sent to Output Port 1 (register 3), then the next byte will be stored in Output Port 0 (register 2).

There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register may be updated independently of the other registers.

11.1.2. Reading the port registers

In order to read data from the CA9555V, the bus master must first send the CA9555V address with the least significant bit set to a logic 0 (see Figure 5). The command byte is sent after the address and determines which register will be accessed. After a restart, the device address is sent again, but this time the least significant bit is set to a logic 1. Data from the register defined by the command byte will then be sent by the CA9555V (see Figure 9 and Figure 10). Data is clocked into the register on the falling edge of the acknowledge clock pulse. After the first byte is read, additional bytes may be read but the data will now reflect the information in the other register in the pair. For example, if you read Input Port 1, then the next byte read would be Input Port 0. There is no limitation on the number of data bytes received in one read transmission but the final byte received, the bus master must not acknowledge the data.

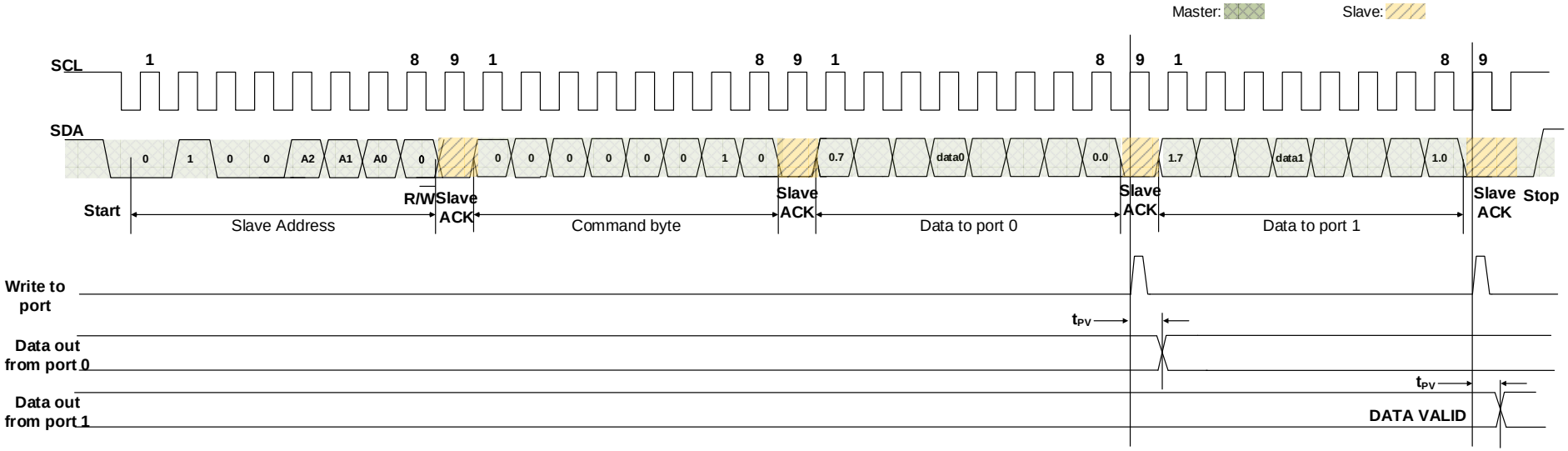


Figure 7. Write to Output port registers

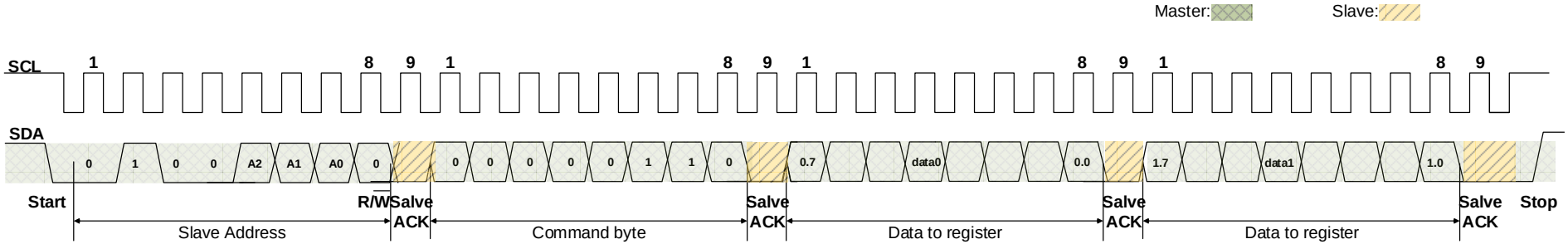
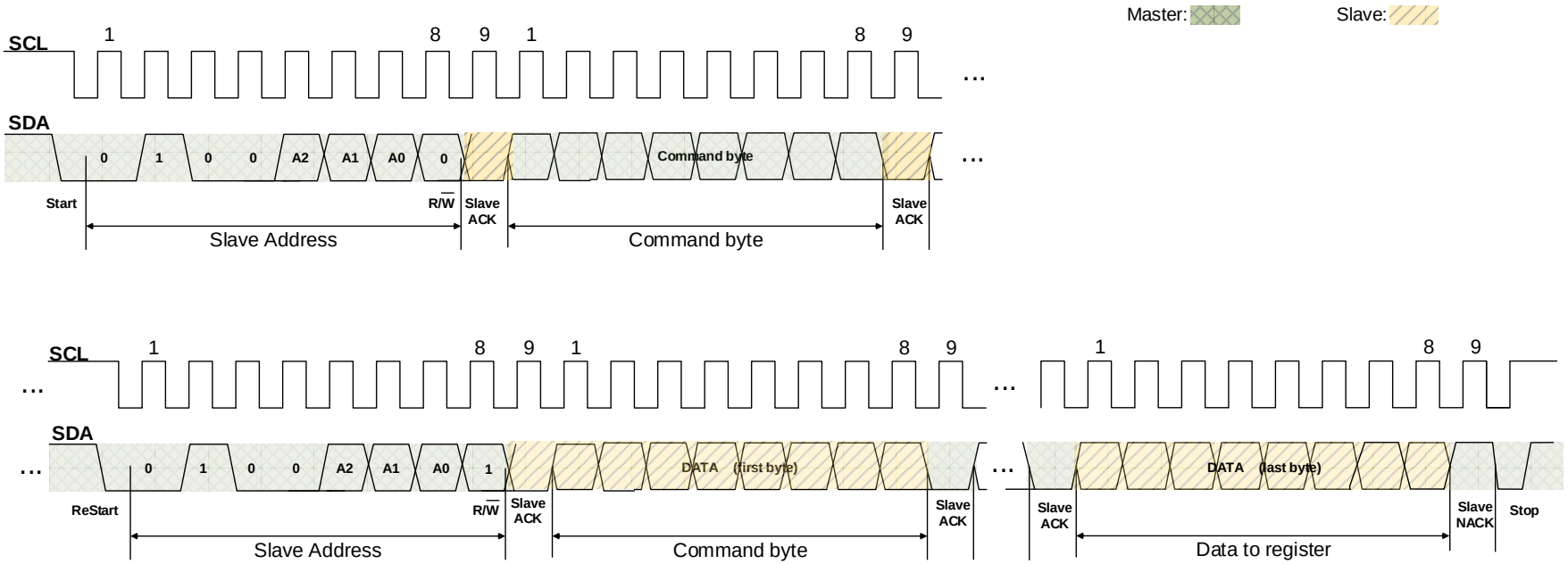
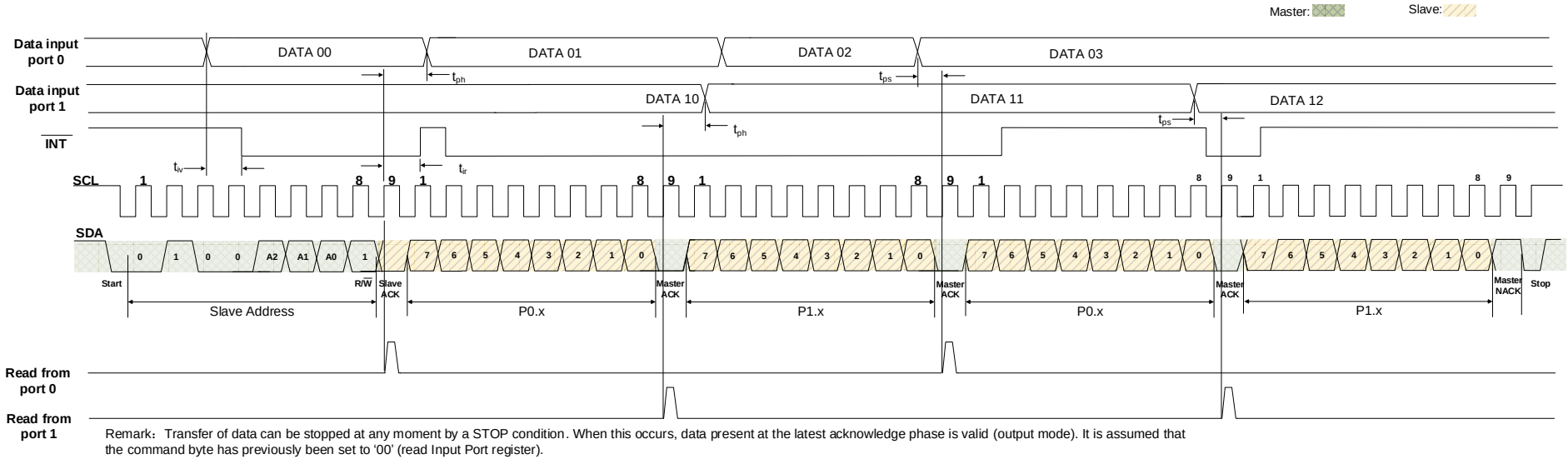


Figure 8. Write to Configuration registers



Remark：Transfer can be stopped at any time by a STOP condition.

Figure 9. Read from register



Remark：Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read Input Port register).

Figure 10. Read input port register

11.2. Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

11.2.1. Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 11).

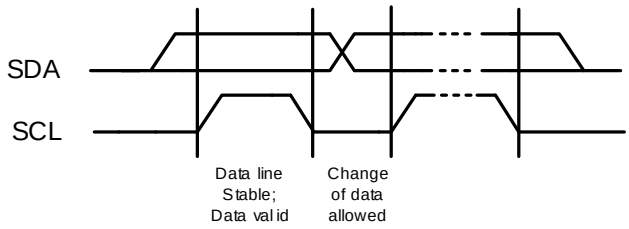


Figure 11. Bit transfer

11.2.2. START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 12).

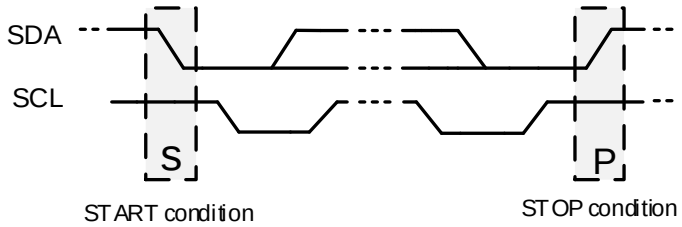


Figure 12. Definition of START and STOP conditions

11.2.3. System configuration

A device generating a message is a ‘transmitter’; a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Figure 13).

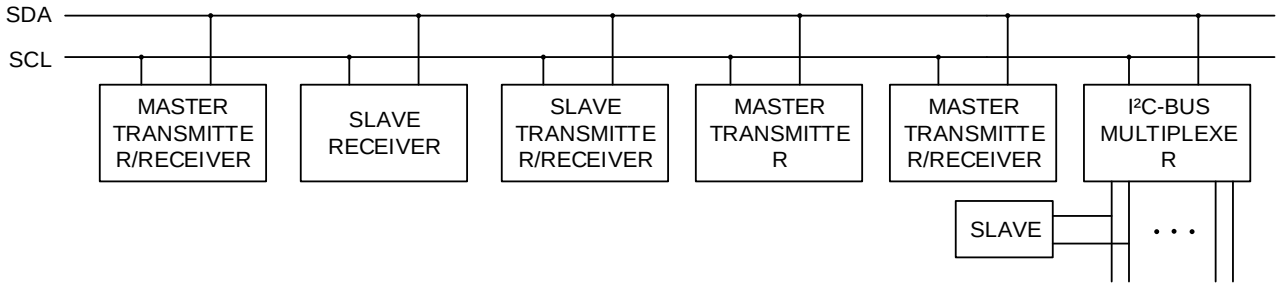


Figure 13. System configuration

11.2.4. Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an ACK after the reception of each byte. Also, a master must generate an ACK after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the ACK related clock pulse; set-up time and hold time must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an ACK on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

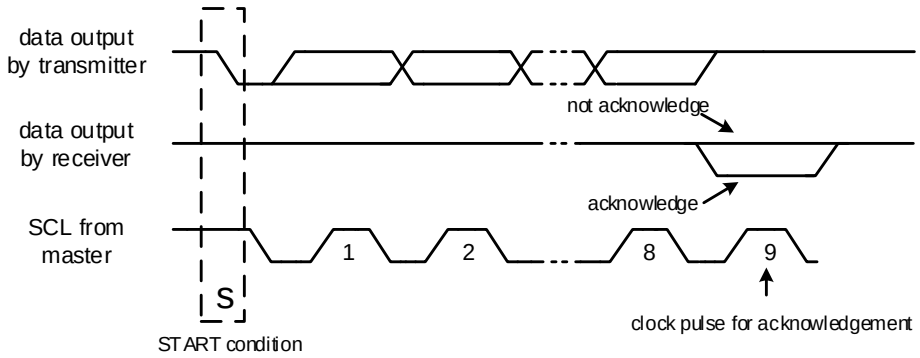


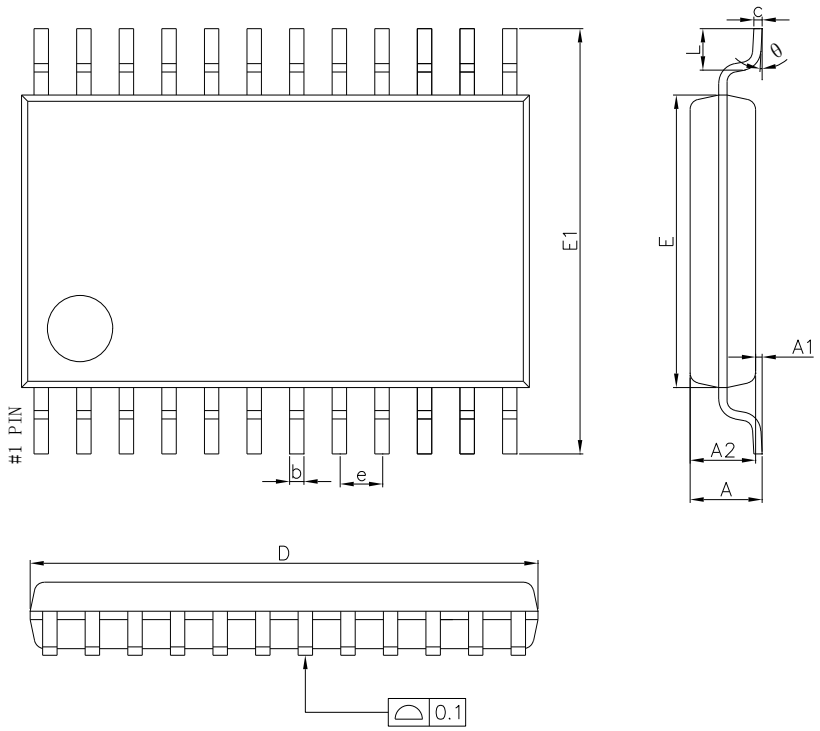
Figure 14. Acknowledgement on the I²C-bus

12. Package Outline Dimensions Information and Recommend Land Pattern Layout

12.1. TSSOP-24

Package Outline Dimensions (TSSOP-24)

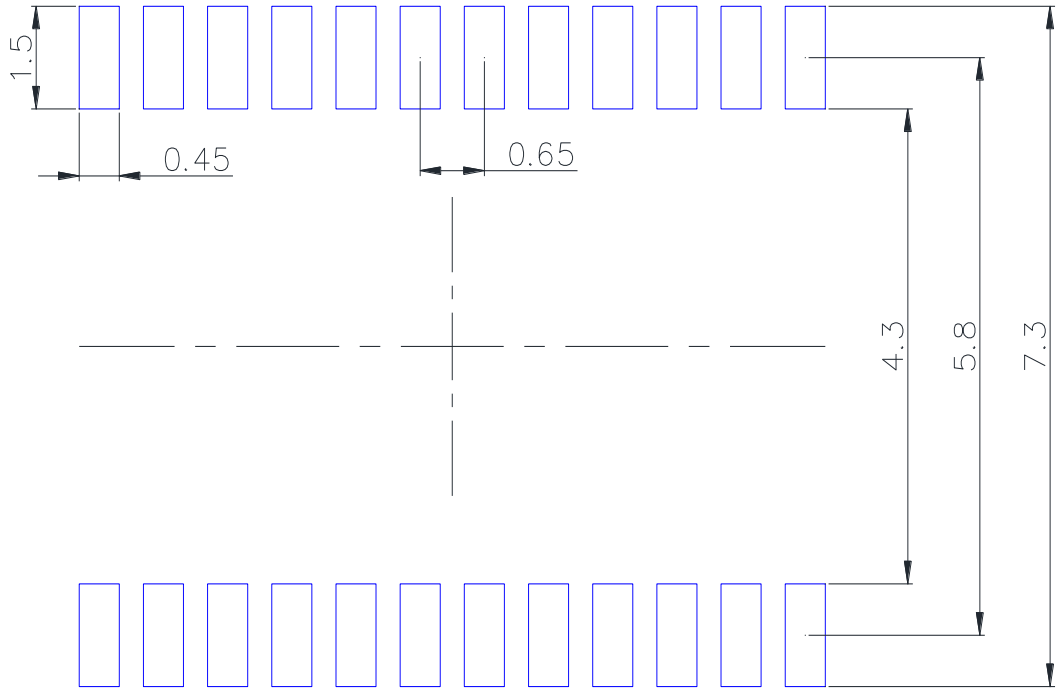
TSSOP-24 Unit (mm)



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	7.700	7.900	0.303	0.311
E	4.300	4.500	0.169	0.177
E1	6.200	6.600	0.244	0.260
e	0.650（BSC）		0.026（BSC）	
L	0.400	0.800	0.016	0.031
θ	0°	8°	0°	8°

Recommend Land Pattern Layout (TSSOP-24)

TSSOP-24 Unit (mm)



Note:

(1) All dimensions are in millimeter

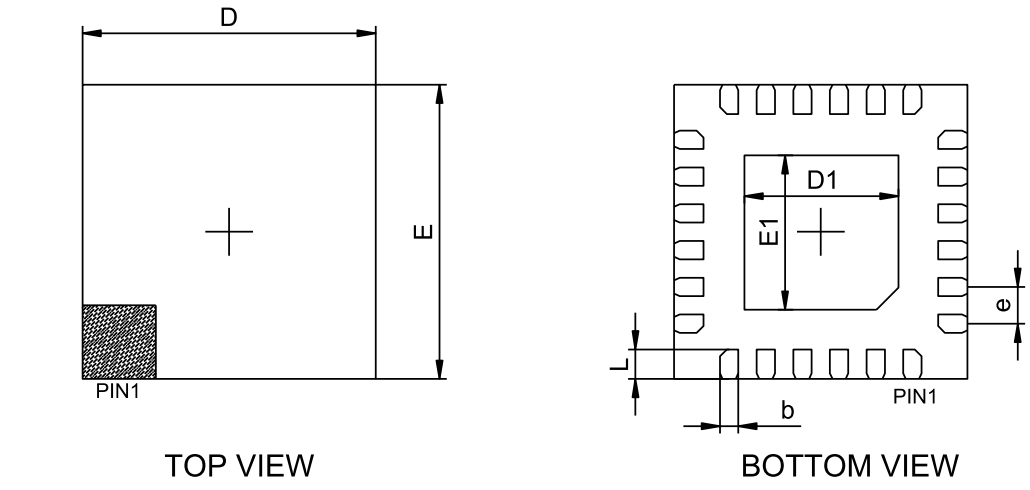
(2) Recommend tolerance is within ±0.1mm

(3) Change without notice

12.2. QFN4x4-24A

Package Outline Dimensions (QFN4x4-24A)

QFN4x4-24A Unit (mm)

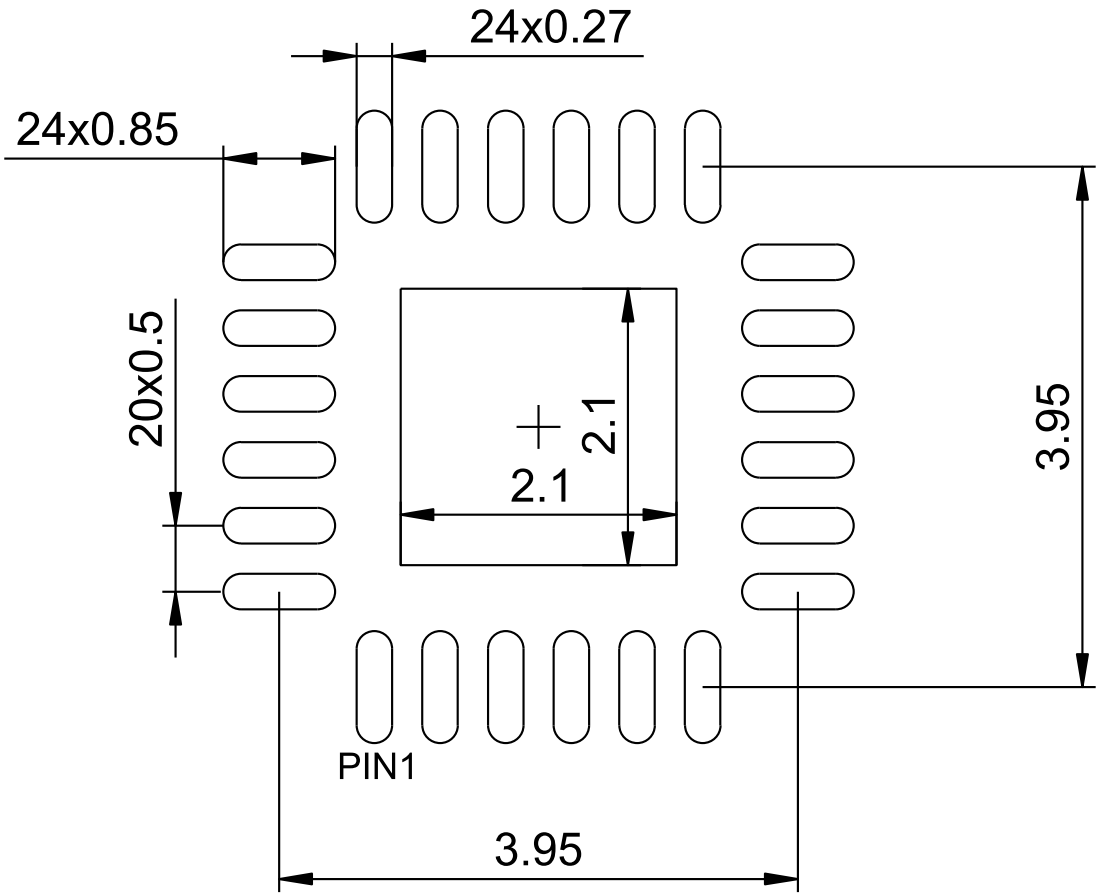


Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF	
D	3.900	4.100	0.154	0.161
E	3.900	4.100	0.154	0.161
D1	2.000	2.200	0.079	0.087
E1	2.000	2.200	0.079	0.087
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP	
L	0.300	0.500	0.012	0.020

Note： Pin 1 shape for thermal pad on backside is not limited to bevel, it can be a notch or arch

Recommend Land Pattern Layout (QFN4x4-24A)

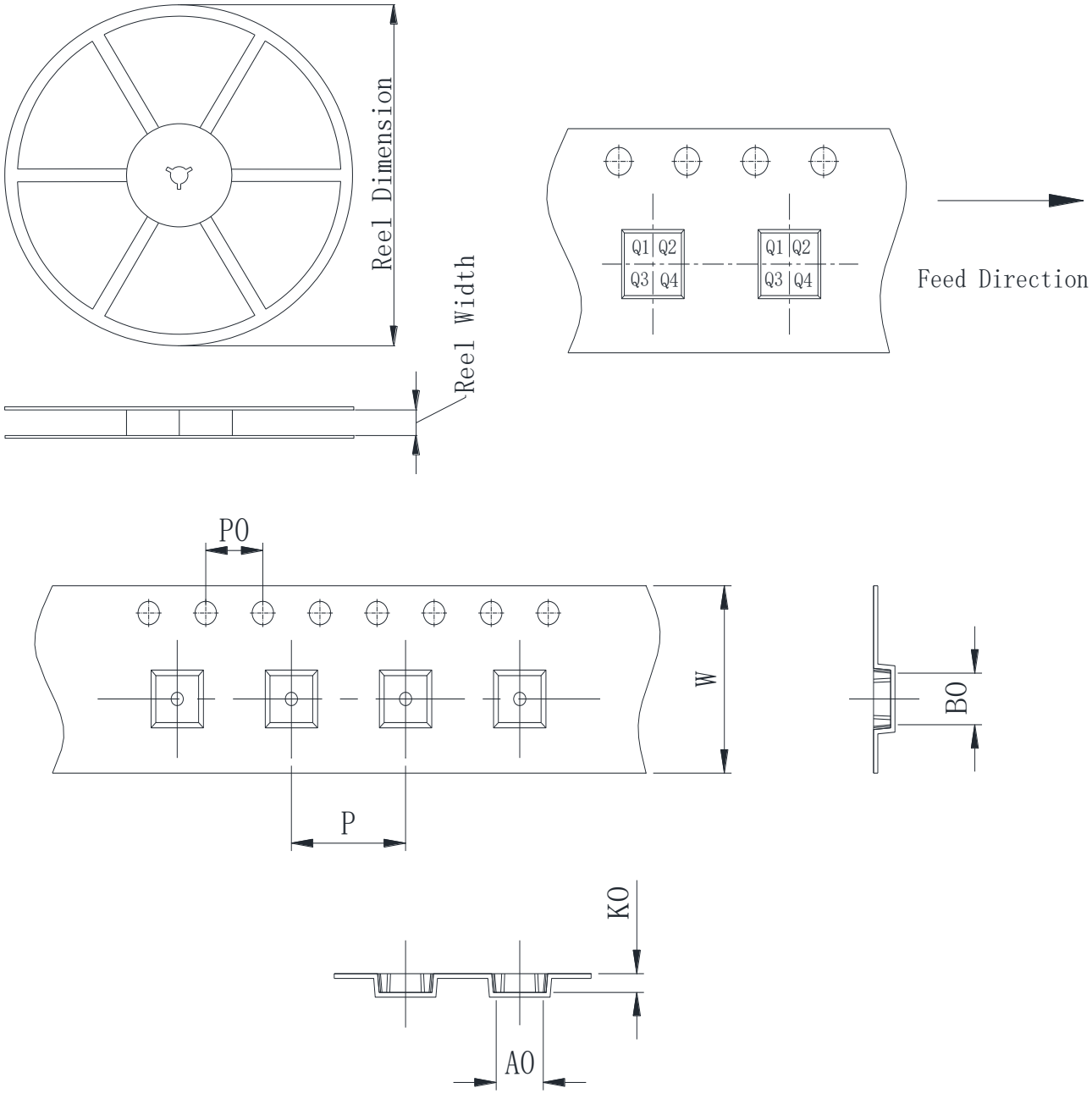
QFN4x4-24A Unit (mm)



Note:

1. All dimensions are in millimeter
2. Recommend tolerance is within ±0.1mm
3. If the thermal pad is not necessary, designer can leave the land pattern area blank
4. Change without notice

13. Packing information



Package type	Reel size	Reel dimension (±3.0mm)	Reel width (±1.0mm)	A0 (±0.1mm)	B0 (±0.1mm)	K0 (±0.1mm)	P (±0.1mm)	P0 (±0.1mm)	W (±0.3mm)	Pin1
TSSOP-24	13'	330	16.4	6.8	8.3	1.6	8.0	4.0	16.0	Q1
QFN4x4-24A	13'	330	12.4	4.3	4.3	1.1	8.0	4.0	12.0	Q1

Revision History

Version	Date	Change Content
Ver1.0	2024/08	Initial Version

SENSYLINK Microelectronics Inc.

www.sensylink.com

IMPORTANT NOTICE

SENSYLINK Microelectronics Inc. reserves the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein or to discontinue any product or service. Customers should obtain the latest relevant information before placing orders and should verify the latest and complete information. SENSYLINK Microelectronics does not assume any responsibility for use of any product, nor does SENSYLINK Microelectronics any liability arising out of the application or use of this document or any product or circuit described herein. SENSYLINK Microelectronics assumes no liability for applications assistance or the design of Customers' products. Customers are responsible for their products and applications using SENSYLINK Microelectronics components. SENSYLINK Microelectronics does not convey any license under its patent or trademark rights nor the other rights.