Features

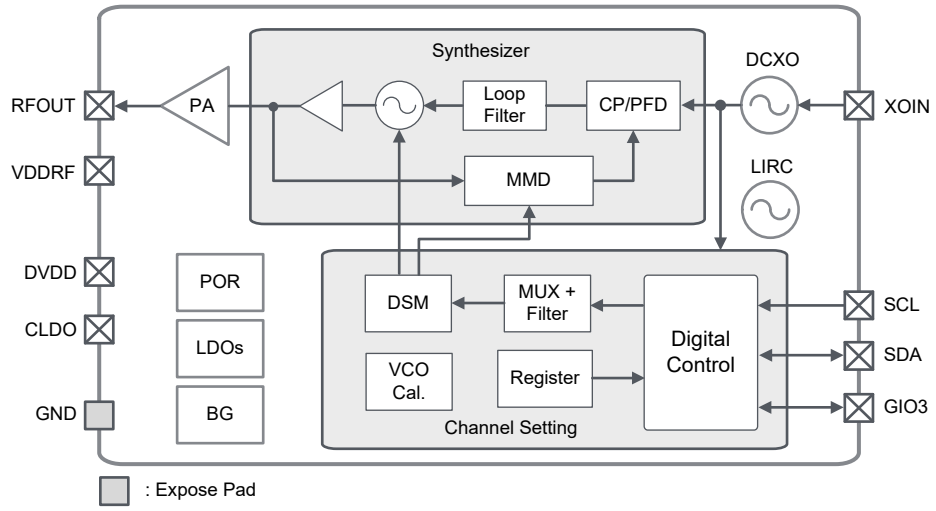
- Supports GFSK (BT=0.5) modulation with 1Mbps data rate, compliant with BLE standard
- Operating frequency: 2402/2426/2480MHz
- Operating voltage range: 2.0V~3.6V
- Programmable TX power
  - High power matching: -10/-5/-2/+5dBm (Max. +8dBm)
  - Low power matching: -10/-5/0/+2dBm (Max. +5dBm)
- Low current consumption
  - Low deep sleep current: 0.35μA
  - TX current consumption: 19mA @ 5dBm TX power
  - TX current consumption: 12mA @ -5dBm TX power
- Supports 32MHz crystal
- FCC/ETSI compliant
- Package types: 8-pin SOP-EP, 10-pin MSOP-EP

General Description

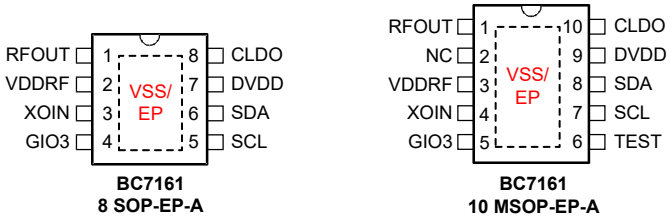
Bluetooth Beacon adopts BLE advertising feature to support new applications such as indoor navigation, healthcare, etc. The advertised packets are placed in the Channel 37, 38 and 39 to avoid the interference from WiFi channels at ISM band. The BC7161 is aimed for the Beacon device for various proximity aware applications.

The BC7161 is a low-cost 2.4GHz BLE Beacon transmitter. With an external 32MHz crystal (XO), an MCU and a few ceramic capacitors, it can implement a complete Beacon device. The output power level can be programmed from -10dBm to +5dBm for various applications. Maximum of +8dBm with 24mA current consumption can be achieved even for a low-cost 8-pin SOP-EP package.

Block Diagram



Pin Assignment



Pin Description

Pin No.		Pin Name	Type	Pin Description
8SOP-EP	10MSOP-EP			
1	1	RFOUT	AO	RF output signal from PA, connected to a matching circuit
2	3	VDDRF	PWR	RF analog power supply
3	4	XOIN	AI	Crystal input
4	5	GIO3	DI/DO	General purpose pin
–	6	TEST	—	Not connected, leave floating
5	7	SCL	DI	I²C clock input
6	8	SDA	DI/DO	I²C data
7	9	DVDD	PWR	RF digital power supply
8	10	CLDO	PWR	LDO output, connected to a bypass capacitor
—	2	NC	—	No connection
—	—	VSS/EP	PWR	Exposed pad, must be connected to ground

Legend: DI: Digital Input; DI/DO: Digital Input/Output; AI: Analog Input;
AO: Analog Output; PWR: Power

The backside plate of EP shall be well soldered to ground on PCB, otherwise it will downgrade RF performance.

Absolute Maximum Ratings

Supply Voltage ..... V_{SS}-0.3V to V_{SS}+3.6V

Voltage on I/O Ports ..... V_{SS}-0.3V to V_{DD}+0.3V

Storage Temperature ..... -60°C to 150°C

Operating Temperature ..... -40°C to 85°C

ESD HBM ..... ±2kV

The device is ESD sensitive. HBM (Human Body Mode) is based on MIL-STD-883.

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C, V_{DD}=3.3V, f_{XTAL}=32MHz,
GFSK modulation with matching circuit, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_{OP}	Operating Temperature	—	-40	—	85	°C
V_{DD}	Supply Voltage	—	2.0	3.3	3.6	V
Digital I/Os						
V_{IH}	High Level Input Voltage	—	0.7×V_{DD}	—	V_{DD}	V
V_{IL}	Low Level Input Voltage	—	0	—	0.3×V_{DD}	V
V_{OH}	High Level Output Voltage	I_{OH}=-5mA	0.8×V_{DD}	—	V_{DD}	V
V_{OL}	Low Level Output Voltage	I_{OL}=5mA	0	—	0.2×V_{DD}	V
Current Consumption						
$I_{DeepSleep}$	Deep Sleep Mode Current	—	—	0.35	1.00	μA
I_{Idle}	Idle Mode Current	LIRC on	—	1.6	—	μA
$I_{LightSleep}$	Light Sleep Mode Current	X'tal on	—	1	—	mA

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{TX}	TX Mode Current (High Power Matching)	RF output power=-10dBm	—	10.5	—	mA
		RF output power=-5dBm	—	12.5	—	
		RF output power=-2dBm (Note)	—	15.5	—	
		RF output power=5dBm	—	19	—	
		RF output power=8dBm	—	24	—	
	TX Mode Current (Low Power Matching)	RF output power=-10dBm	—	10.5	—	mA
		RF output power=-5dBm	—	11.5	—	
		RF output power=0dBm	—	15.5	—	
		RF output power=2dBm	—	17.5	—	
		RF output power=5dBm	—	19.5	—	

Note: Measured at the 8-pin SOP-EP package.

A.C. Characteristics

Ta=25°C, V_{DD}=3.3V, f_{XTAL}=32MHz,
GFSK modulation with matching circuit, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Transmitter Characteristics						
f_{RF}	RF Operating Frequency	CH37	—	2402	—	MHz
		CH38	—	2426	—	
		CH39	—	2480	—	
DR	Data Rate	GFSK@f_{DEV}=250kHz	—	1	—	Mbps
f_{DEV}	Frequency Deviation	—	—	250	—	kHz
P_{OUT}	RF Transmit Output Power	—	-10	-2	8	dBm
$f_{channel}$	Channel Spacing	Non-overlapping channel spacing	—	2	—	MHz
	Occupied Bandwidth	—	—	1	—	MHz
SE_{TX}	TX Spurious Emission (P_{OUT}=5dBm)	f < 1GHz	—	—	-36	dBm
		47MHz < f < 74MHz	—	—	-54	
		87.5MHz < f < 108MHz				
		174MHz < f < 230MHz				
		470MHz < f < 862MHz				
		f > 1GHz	—	—	-30	
	Adjacent Channel Power	f_{RF} ± 2MHz	—	—	-20	dBm
		f_{RF} ± (3+n)MHz; n=0, 1, 2...	—	—	-30	
LO Characteristics						
f_{LO}	Frequency Coverage Range	—	2400	—	2500	MHz
f_{STEP}	Frequency Synthesizer Step	—	—	—	10	kHz
PN	2.4GHz Phase Noise	PN@100k offset	—	-85	—	dBc/Hz
		PN@1M offset	—	-105	—	
Crystal (X'tal) Osicillator						
f_{XTAL}	X'tal Frequency	General case	—	32	—	MHz
ESR	X'tal Equivalent Series Resistance	—	—	—	100	Ω
C_{LOAD}	X'tal Capacitor Load	—	12	—	16	pF
	X'tal Tolerance	—	-20	—	+20	ppm
$t_{Startup}$	X'tal Settling Time	49US with a 12pF C_{LOAD}	—	—	0.8	ms
		3225 SMD with a 12pF C_{LOAD}	—	—	1	

I²C Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_{SCL}	Serial clock frequency	—	—	—	1	MHz
t_{BUF}	Bus free time between stop and start condition	SCL=1MHz	250	—	—	ns
t_{LOW}	SCL low time	SCL=1MHz	500	—	—	ns
t_{HIGH}	SCL high time	SCL=1MHz	500	—	—	ns
$t_{su(DAT)}$	Setup time SDA → SCL	SCL=1MHz	100	—	—	ns
$t_{su(STA)}$	Start condition setup time	SCL=1MHz	250	—	—	ns
$t_{su(STO)}$	Stop condition setup time	SCL=1MHz	250	—	—	ns
$t_{h(DAT)}$	Hold time SDA → SCL	SCL=1MHz	100	—	—	ns
$t_{h(STA)}$	Start condition hold time	SCL=1MHz	250	—	—	ns
$t_{r(SCL)}$	Rise time of SCL signal	SCL=1MHz	—	—	100	ns
$t_{f(SCL)}$	Fall time of SCL signal	SCL=1MHz	—	—	100	ns
$t_{r(SDA)}$	Rise time of SDA signal	SCL=1MHz	—	—	100	ns
$t_{f(SDA)}$	Fall time of SDA signal	SCL=1MHz	—	—	100	ns

Functional Description

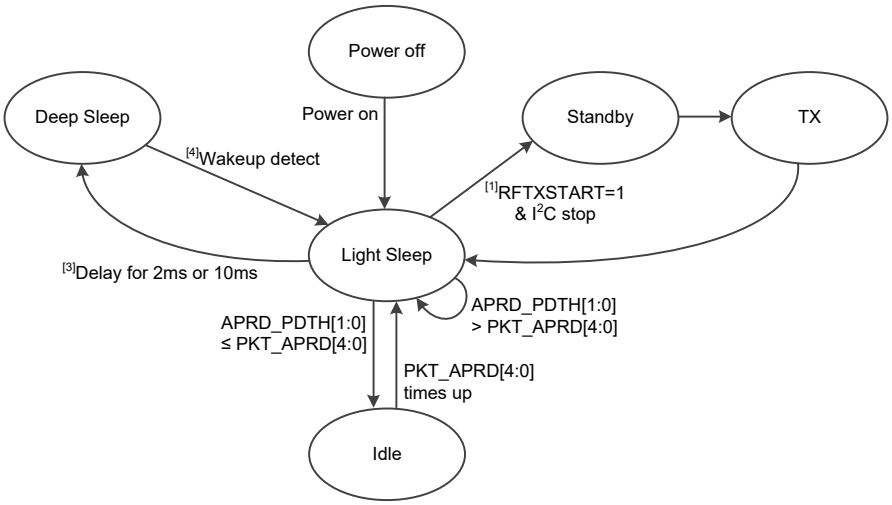
2.4GHz RF Transmitter

The BC7161 is a fully integrated 2.4GHz transmitter. It consists of a fractional-N synthesizer, a programmable power amplifier (PA) and power management. The synthesizer loop filter, 4.8GHz VCO and Digital Controlled XO (DCXO) are all integrated.

The transmitting session is an enhanced VCO direct modulation architecture. The GFSK modulation signal is fed into the PLL loop to take advantage of the fractional-N synthesizer. Another signal path is fed into the VCO directly to compensate the PLL loop response. As a result, it can generate a low FSK error GFSK signal. The modulated signal is fed into a power amplifier (PA) and the maximum output power can be up to +8dBm.

State Machine

The device provides five operating modes, Power Off mode, Deep Sleep mode, Light Sleep mode, Standby mode and TX mode. An external MCU can set RF parameters, transmit data and wake up the RF chip via the I²C interface.

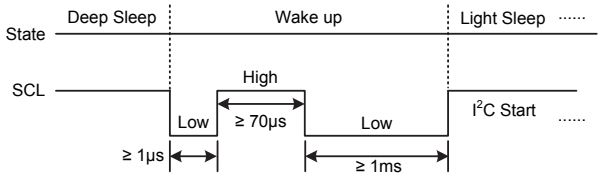


Note: 1. Once the RFTXSTART control bit is enabled, the I²C will stop and the RF chip will start transmiting data.

2. Deep Sleep mode: X'tal off.

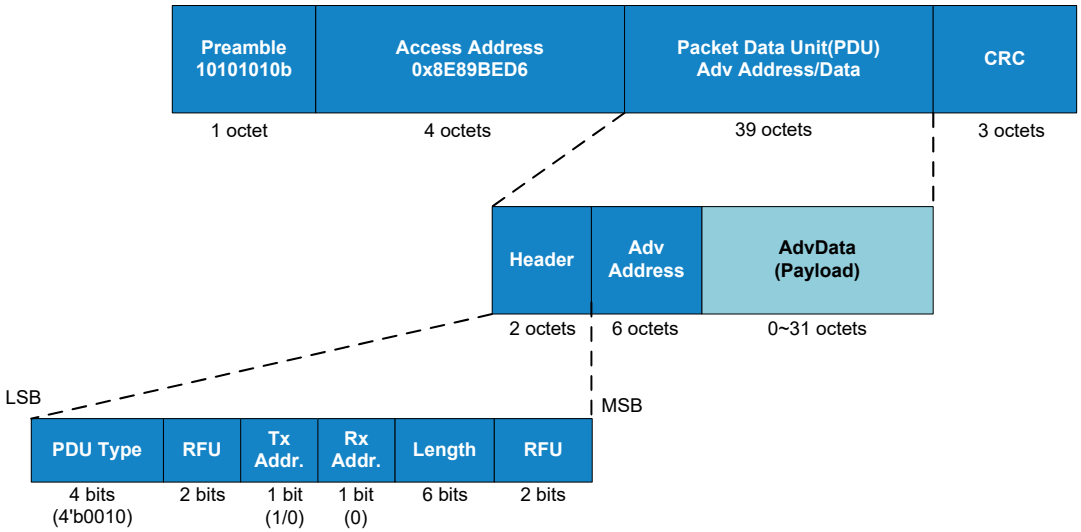
Light Sleep mode: X'tal on, RF frequency synthesizer off.
Standby mode: X'tal on, RF frequency synthesizer on, RF PA off.
TX mode: X'tal on, RF frequency synthesizer on, RF PA on.
Idle mode: X'tal off, LIRC on.

3. In the Light Sleep mode, if the SDA and SCL pin states both keep unchanged for 10ms, the device state will change to the Deep Sleep mode. If the SDA or SCL pin state has been toggled and then keeps unchanged, the timer will reset and recount until the 10ms time is up and then enter the Deep Sleep mode.
4. The device will be woken up from the Deep Sleep mode if a falling edge is detected on the SCL pin and the low pulse width should be maintained at least 1ms to return to Light Sleep state. After this, the master MCU can control the device based on the I²C format.

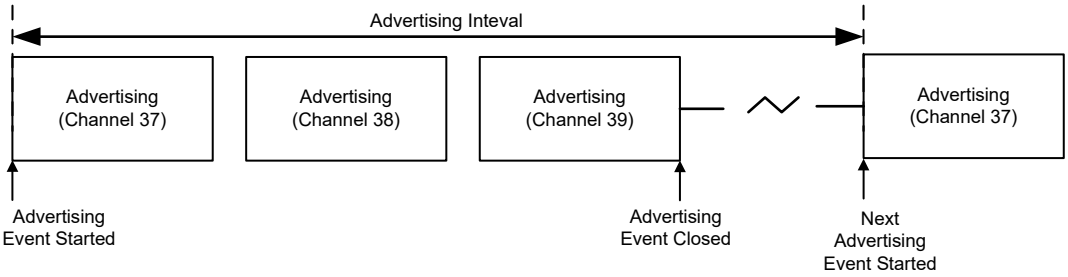


5. Each frame will be sent consecutively until the frame counter (PKT_AUTORS) is finished then enter the Light Sleep mode.

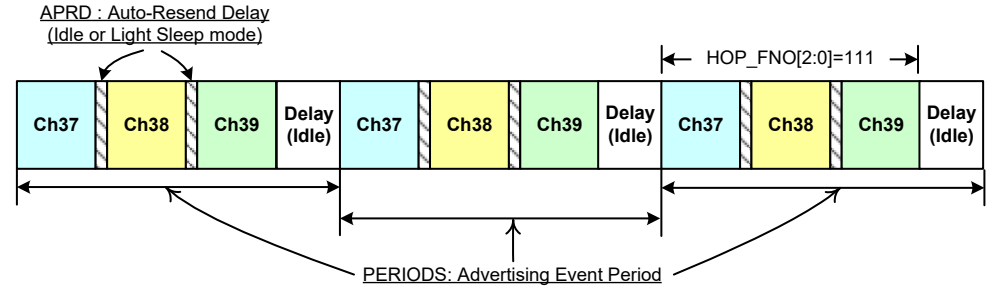
Packet Format



Packet Event Timing



Advertising Inteval = Advertising Event Period + Random



PKT_APRD[4:0]: Packet format auto-resend delay, 250μs (Min.) ~ 8ms (Max.)

PKT_AUTORS[7:0]: Packet event auto-resend times

0: No resend (auto-resend disabled)

1: Resend 1 time

2: Resend 2 times

:

254: Resend 254 times

255: Always resend periodicly until the MCU forcibly turns off the TX transmitter.

During the TX transmission, if the MCU clears the RFTXSTART bit to zero, the TX transmitter will stop after the current advertising event is completed.

PKT_PERIODS[9:0]: Advertising event period

Period=10ms×(1+PKT_PERIODS[9:0])

00-0000-0000: 10ms

00-0000-0001: 20ms

…

11-1111-1111: 10240ms (10.24s)

HOP_FNO[2:0]: Hopping frequency number

Bit0/Bit1/Bit2 indicates the enable bit for Ch37/Ch38/Ch39 respectively

It is not recommended to set these bits to “000”. Ensure that there is at least one channel enabled.

For example:

001: Ch37 enabled, Ch38/Ch39 disabled; each advertising event only includes Ch37

110: Ch38/Ch39 enabled, Ch37 disabled; each advertising event only includes Ch38 and Ch39

101: Ch37/Ch39 enabled, Ch38 disabled; each advertising event only includes Ch37 and Ch39

111: Ch37/Ch38/Ch39 enabled; each advertising event includes Ch37, Ch38 and Ch39.

I²C Serial Programming

The device supports the I²C format for byte write, page write, byte read and page read formats. Regarding the page write/read, register address will not automatically increase for the FIFO port (address: 10h) when continuously writing/reading data to/from the FIFO.

It should be noted that the I²C is a non-standard I²C interface, which only supports a single device for connection.

Byte Write

Page Write

Byte Read

Page Read

Bus Direction: : Host to device; : Device to host

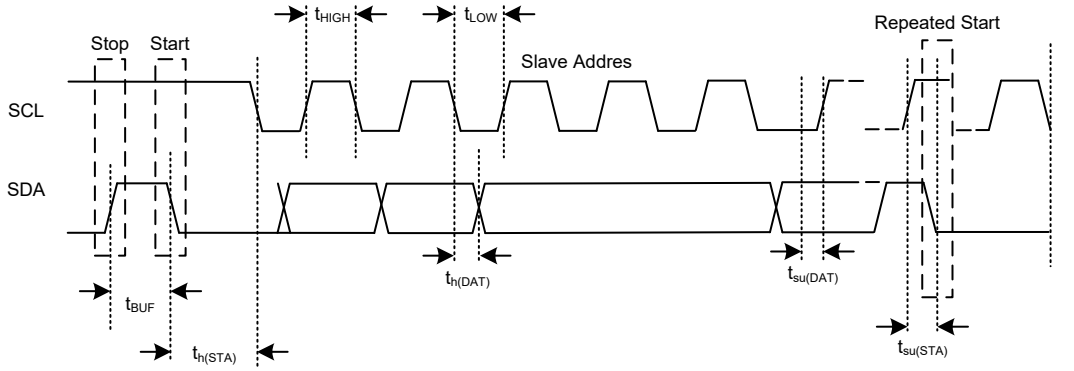
Symbol Definitions: S: Start; RS: Repeated Start; P: Stop

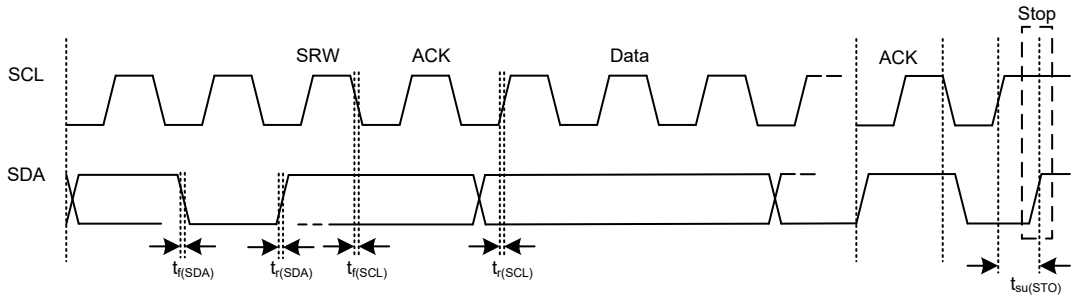
DADDR[6:0]: Device Address, 71h

R/W: Read/Write select; R: Read(1); W: Write(0)

RADDR[7:0]: register address

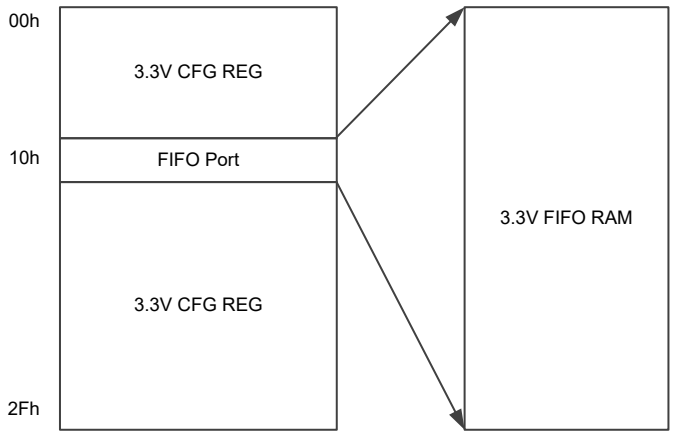
A: ACK(0); NA: NAK(1)





S = Start (1 bit)
SA = Slave Address (7 bits)
SR = SRW bit (1 bit)
M = Slave device send acknowledge bit (1 bit)
D = Data (8 bits)
A = ACK (RXAK bit for transmitter, TXAK for receiver, 1 bit)
P = Stop (1 bit)

Memory Mapping



The steps for writing data to the FIFO via the I²C are described below:

1. Set the RSTPDUFF bit to 1 and clear the FIFO pointer. When the FIFO has been cleared the RSTPDUFF bit will be cleared to zero automatically.
2. Write data continuously to the address 10h. The I²C register address will stay at 10h without increament.
3. Configure the PDULEN bit field with a PDU data length to be transmitted.
4. To re-configure the PDU data, repeat step 1~3.

Configuration Registers

Addr.	Name	Bit							
		7	6	5	4	3	2	1	0
00h	CFG0	—		XO_TRIM[5:0]					
07h	CFG7	Setting1							
0Ch	CFGC	RFTXP_1							
0Dh	CFGD	RFTXP_2							
10h	CFG10	PDUDATA[7:0]							
11h	CFG11	RSTPDUFF	PDULEN[6:0]						
12h	CFG12	—		PDUDPTR[5:0]					
15h	CFG15	PKT_AUTORS[7:0]							
16h	CFG16	APRD_PDTH[1:0]		RNDDLY_EN	PKT_APRD[4:0]				
17h	CFG17	PKT_PERIODS[7:0]							
18h	CFG18	—							PKT_PERIODS[9:8]
1Ah	CFG1A	RFTXSTART	—				HOP_FNO[2:0]		
1Dh	CFG1D	Cal1	—						
1Eh	CFG1E	—							Cal2
25h	CFG25	—	GIO3S[2:0]			—			
26h	CFG26	—				GIOPU	—		
27h	CFG27	—	LSTOS	LSTOM[1:0]		—			
2Ah	CFG2A	Setting2							
30h	CFG30	CHIPID[7:0]							
31h	CFG31	CHIPID[15:8]							
33h	CFG33	RMSOUT	—						RST_RF

Note that for the addresses which are not listed in this table, it is suggested not to change their initial values.

- **CFG0: Configuration Register 0**

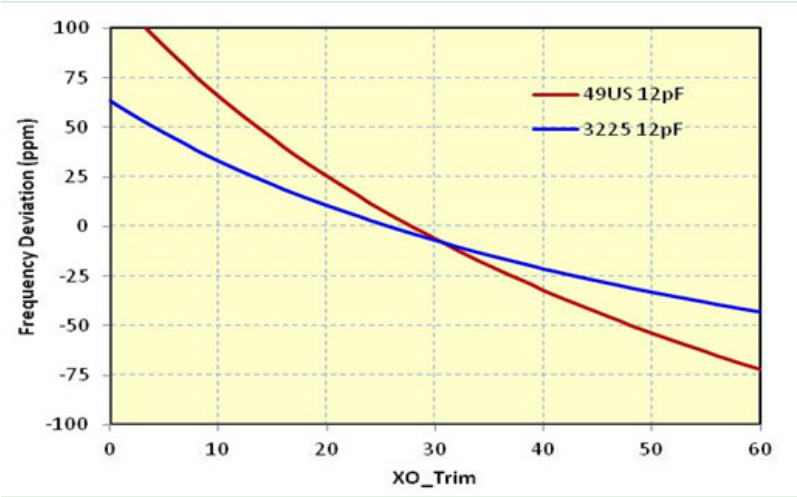
Bit	7	6	5	4	3	2	1	0
Name	—	—	XO_TRIM[5:0]					
R/W	—	—	R/W					
POR	0	0	1	0	0	0	0	0

Bit 7~6 Reserved bits, cannot be changed

Bit 5~0 **XO_TRIM[5:0]**: Trim value for the internal capacitor load of the crystal

49US 32MHz XO with a 12pF C_{LOAD}: The seggested setting is 1CH. Within ±25ppm frequency error, 1 trim code shifts -2.95ppm.

3225SMD 32MHz XO with a 12pF C_{LOAD}: The seggested setting is 1AH. Within ±25ppm frequency error, 1 trim code shifts -1.75ppm.



- **CFG7: Configuration Register 7**

Bit	7	6	5	4	3	2	1	0
Name	Setting1							
R/W	R/W							
POR	1	0	0	1	1	0	0	1

Bit 7~0 Reserved bits, must be set to “10010101” after power on

- **CFGC: Configuration Register C**

Bit	7	6	5	4	3	2	1	0
Name	RFTXP_1							
R/W	R/W							
POR	0	0	1	0	0	0	0	1

- **CFGD: Configuration Register D**

Bit	7	6	5	4	3	2	1	0
Name	RFTXP_2							
R/W	R/W							
POR	1	0	0	0	0	1	1	1

The recommended setting values (hexadecimal) for the CFGC and CFGD registers are listed below.

8-pin SOP-EP

TX Power	High Power Matching		Low Power Matching	
	CFGC (RFTXP_1)	CFGD (RFTXP_2)	CFGC (RFTXP_1)	CFGD (RFTXP_2)
8dBm	A1	AF		
5dBm	A2	67	A1	A7
2dBm			A2	A1
0dBm			AF	D7
-2dBm	AF	D7		
-5dBm	AF	77	AF	73
-10dBm	AF	71	AF	71

10-pin MSOP-EP

TX Power	High Power Matching	
	CFGC (RFTXP_1)	CFGD (RFTXP_2)
8dBm	A4	87
5dBm	A2	83
2dBm		
0dBm	AF	D7
-5dBm	AF	73
-10dBm	AF	71

- **CFG10: Configuration Register 10**

Bit	7	6	5	4	3	2	1	0
Name	PDUDATA[7:0]							
R/W	W							
POR	x	x	x	x	x	x	x	x

Bit 7~0 **PDUDATA[7:0]**: PDU data FIFO write port

- **CFG11: Configuration Register 11**

Bit	7	6	5	4	3	2	1	0
Name	RSTPDUFF	PDULEN[6:0]						
R/W	R/W	R/W						
POR	0	0	0	1	1	1	1	1

Bit 7 **RSTPDUFF**: Reset PDU data FIFO, automatically cleared after completion

Bit 6~0 **PDULEN[6:0]**: PDU data length (unit: octet); maximum: 39 octets

- **CFG12: Configuration Register 12**

Bit	7	6	5	4	3	2	1	0
Name	—	—	PDUDPTR[5:0]					
R/W	—	—	R/W					
POR	0	0	0	0	0	0	0	0

Bit 7~6 Reserved bits, cannot be changed

Bit 5~0 **PDUDPTR[5:0]**: PDU data pointer, points to the start address to execute CRC/whitening operations in PDU FIFO

- **CFG15: Configuration Register 15**

Bit	7	6	5	4	3	2	1	0
Name	PKT_AUTORS[7:0]							
R/W	R/W							
POR	1	1	1	1	1	1	1	1

Bit 7~0 **PKT_AUTORS[7:0]**: Packet event auto-resend times

00h: No resend, auto-resend disabled

01h: Resend 1 time

02h: Resend 2 times

...

FFh: Always resend until RFTXSTART=0

- **CFG16: Configuration Register 16**

Bit	7	6	5	4	3	2	1	0
Name	APRD_PDTH[1:0]		RNDDLY_EN	PKT_APRD[4:0]				
R/W	R/W		R/W	R/W				
POR	0	0	1	1	1	1	1	1

Bit 7~6 **APRD_PDTH[1:0]**: Time threshold for automatically entering Idle mode

00: 1ms

01: 1.5ms

10: 2ms

11: 3ms

These bits define the time threshold that the device should automatically enter the Idle mode. The device will stay in the Light Sleep mode if the automatic retransmission interval defined by PKT_APRD[4:0] is less than the time threshold defined by APRD_PDTH[1:0]. Otherwise, the device will enter the Idle mode.

APRD_PDTH[1:0] > PKT_APRD[4:0] → Enter light sleep mode

APRD_PDTH[1:0] ≤ PKT_APRD[4:0] → Enter Idle mode

Bit 5 **RNDDLY_EN**: Enable random delay (250~8000μs) per advertising event period

0: Disable

1: Enable

Bit 4~0 **PKT_APRD[4:0]**: Packet format auto-resend delay

00000: 250μs

00001: 500μs

00010: 750μs

…

11111: 8000μs (8ms)

- **CFG17: Configuration Register 17**

Bit	7	6	5	4	3	2	1	0
Name	PKT_PERIODS[7:0]							
R/W	R/W							
POR	0	1	1	0	0	0	1	1

Bit 7~0 **PKT_PERIODS[7:0]**: Advertising event period low byte

- **CFG18: Configuration Register 18**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	PKT_PERIODS[9:8]	
R/W	—	—	—	—	—	—	R/W	
POR	0	0	0	0	0	0	0	0

Bit 7~2 Reserved bits, cannot be changed

Bit 1~0 **PKT_PERIODS[9:8]**: Advertising event period high byte

Delay=10ms×(1+PKT_PERIODS[9:0]); range: 10ms (000h) ~ 10240ms (3FFh)

- **CFG1A: Configuration Register 1A**

Bit	7	6	5	4	3	2	1	0
Name	RFTXSTART	—	—	—	—	HOP_FNO[2:0]		
R/W	R/W	—	—	—	—	R/W		
POR	0	0	0	0	0	1	1	1

Bit 7 **RFTXSTART**: RF layer2 transmission start control

0: RF layer2 transmission stops

1: RF layer2 transmission starts

This bit will be cleared to zero by hardware when the automatic retransmission count is full and all the payloads are completed. If this bit is cleared by the MCU, the RF TX will stop transmission.

Note: When the RFTXSTART bit changes from 1 to 0, which means to finish the WOT mode, the device needs an additional 70μs to exit the WOT mode. During this time any I^2C commands including WAKEUP would not be accepted.

Bit 6~3 Reserved bits, cannot be changed

Bit 2~0 **HOP_FNO[2:0]**: Hopping frequency number

HOP_FNO[0]: Enable channel 37 (2402MHz)

HOP_FNO[1]: Enable channel 38 (2426MHz)

HOP_FNO[2]: Enable channel 39 (2480MHz)

It is not recommended to set these bits to “000”. Ensure that there is at least one channel enabled.

- **CFG1D: Configuration Register 1D**

Bit	7	6	5	4	3	2	1	0
Name	Cal1	—	—	—	—	—	—	—
R/W	R/W	—	—	—	—	—	—	—
POR	0	0	0	1	1	1	1	0

Bit 7 **Cal1**: Described in the CFG1E register

Bit 6~0 Reserved bits, cannot be changed

- **CFG1E: Configuration Register 1E**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	Cal2
R/W	—	—	—	—	—	—	—	R/W
POR	0	0	1	1	0	1	0	0

Bit 7~1 Reserved, must be set to “0011111” after power on

Bit 0 **Cal2**: Cal1 and Cal2 both should be set to “1” during every power on, then wait until both are cleared to “0”, which means IC calibration has finished.

- **CFG25: Configuration Register 25**

Bit	7	6	5	4	3	2	1	0
Name	—	GIO3S[2:0]			—	—	—	—
R/W	—	R/W			—	—	—	—
POR	0	0	0	0	0	0	0	0

Bit 7 Reserved bit, cannot be changed

Bit 6~4 **GIO3S[2:0]**: GIO3 pin function selection
000: No function, input
001~100: Reserved
101: RFTXSTART output
110: Reserved
111: TXACT, output

Bit 3~0 Reserved bits, cannot be changed

- **CFG26: Configuration Register 26**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	GIOPU	—	—	—
R/W	—	—	—	—	R/W	—	—	—
POR	0	0	0	0	1	1	1	1

Bit 7~4 Reserved bits, cannot be changed

Bit 3 **GIOPU**: GIO3 pull-up resistor control
0: Disable
1: Enable

Bit 2~0 Reserved bits, cannot be changed

- **CFG27: Configuration Register 27**

Bit	7	6	5	4	3	2	1	0
Name	—	LSTOS	LSTOM[1:0]		–	–	–	–
R/W	—	R/W	R/W		–	–	–	–
POR	1	0	0	0	0	0	0	0

Bit 7 Reserved bit, cannot be changed

Bit 6 **LSTOS**: Light sleep time-out selection
0: 2ms
1: 10ms

Bit 5~4 **LSTOM[1:0]**: Light sleep time-out mode selection
00: I^2C time-out turned on with 2ms/10ms delay, TX time-out turned on with 0s delay
01/10: I^2C time-out turned on with 2ms/10ms delay, TX time-out turned on with 2ms/10ms delay
11: Time-out off, always in light sleep mode

Bit 3~0 Reserved bits, cannot be changed

- **CFG2A: Configuration Register 2A**

Bit	7	6	5	4	3	2	1	0
Name	Setting2							
R/W	R/W							
POR	0	1	0	1	0	0	0	0

Bit 7~0 Reserved bits, must be set to "01000111" after power on

- **CFG30: Configuration Register 30**

Bit	7	6	5	4	3	2	1	0
Name	CHIPID[7:0]							
R/W	R							
POR	0	1	1	0	0	0	0	1

Bit 7~0 **CHIPID[7:0]**: Chip ID low byte, 0x61

- **CFG31: Configuration Register 31**

Bit	7	6	5	4	3	2	1	0
Name	CHIPID[15:8]							
R/W	R							
POR	0	1	1	1	0	0	0	1

Bit 7~0 **CHIPID[15:8]**: Chip ID high byte, 0x71

- **CFG33: Configuration Register 33**

Bit	7	6	5	4	3	2	1	0
Name	RMSOUT	—	—	—	—	—	—	RST_RF
R/W	R	—	—	—	—	—	—	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **RMSOUT**: VCO oscillation detection (read only)

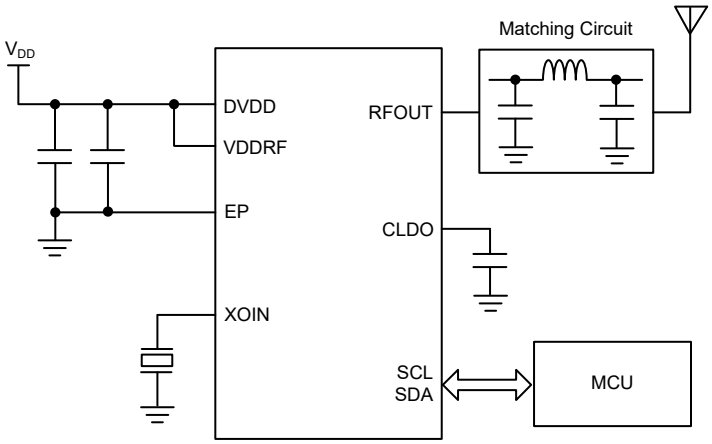
When the VCO oscillates and becomes stable, the RMSOUT bit will be set high by hardware. Otherwise the bit will be cleared to zero.

Bit 6~1 Reserved bits, cannot be changed

Bit 0 **RST_RF**: Registers reset control

Setting this bit high will reset the registers in the addresses 30h~3Fh. This bit will be cleared to zero after the reset is completed.

Application Circuits



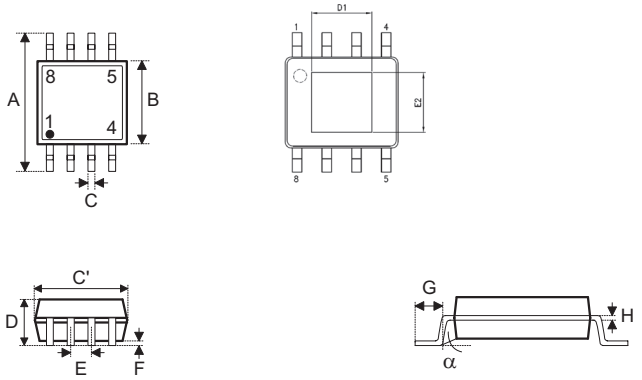
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

8-pin SOP-EP (150mil) Outline Dimensions

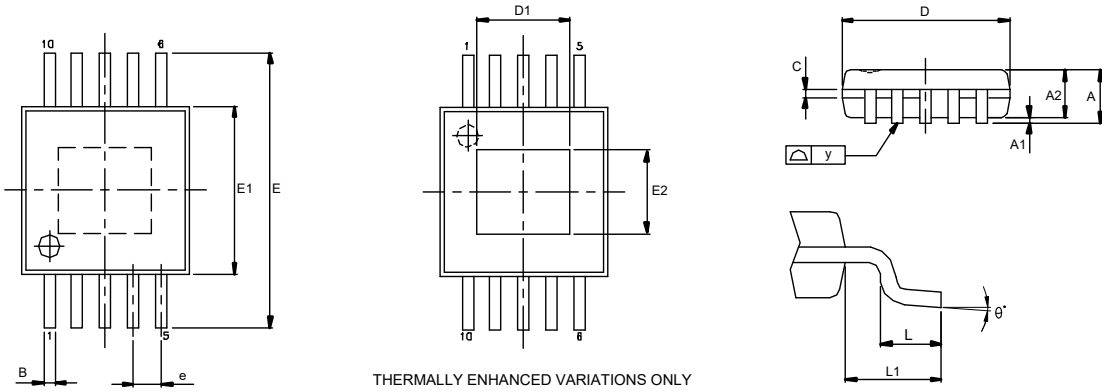


Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.236 BSC	—
B	—	0.154 BSC	—
C	0.012	—	0.020
C'	—	0.193 BSC	—
D	—	—	0.069
D1	0.076	—	0.090
E	—	0.050 BSC	—
E2	0.076	—	0.090
F	0.000	—	0.006
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	6.00 BSC	—
B	—	3.90 BSC	—
C	0.31	—	0.51
C'	—	4.90 BSC	—
D	—	—	1.75
D1	1.94	—	2.29
E	—	1.27 BSC	—
E2	1.94	—	2.29
F	0.00	—	0.15
G	0.40	—	1.27
H	0.10	—	0.25
α	0°	—	8°

Note: For this package type, refer to the package information provided here, which will not be updated by the Holtek website.

10-pin MSOP-EP (118mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	—	0.043
A1	0.000	—	0.006
A2	0.030	0.033	0.037
B	0.007	—	0.013
C	0.003	—	0.009
D	—	0.118 BSC	—
D1	0.059	—	0.076
E	—	0.193 BSC	—
E1	—	0.118 BSC	—
E2	0.055	—	0.071
e	—	0.020 BSC	—
L	0.016	0.024	0.031
L1	—	0.037 BSC	—
y	—	0.004 BSC	—
θ	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	—	1.10
A1	0.00	—	0.15
A2	0.75	0.85	0.95
B	0.17	—	0.33
C	0.08	—	0.23
D	—	3.00 BSC	—
D1	1.51	—	1.93
E	—	4.90 BSC	—
E1	—	3.00 BSC	—
E2	1.40	—	1.80
e	—	0.50 BSC	—
L	0.40	0.60	0.80
L1	—	0.95 BSC	—
y	—	0.10 BSC	—
θ	0°	—	8°