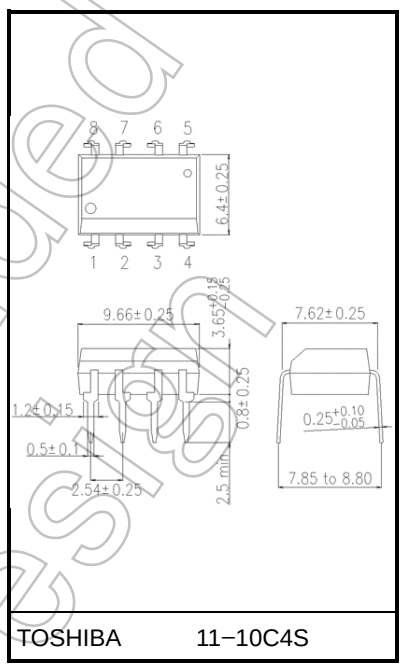
TOSHIBA Photocoupler IRED & Photo IC

6N137

Digital Logic Isolation
Tele-Communication
Analog Data Equipment Control

Unit: mm



TOSHIBA 11−10C4S

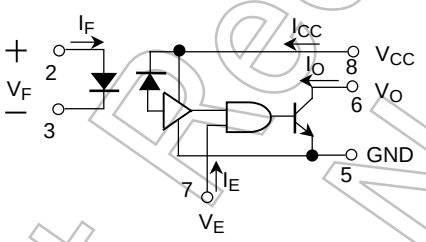
Weight: 0.54 g (typ.)

The TOSHIBA 6N137 consist of an infrared emitting diode and a one chip photo IC. This unit is 8-lead DIP package.

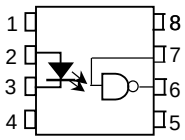
- LSTTL / TTL compatible: 5V Supply
- Ultra high speed: 10MBd
- Guaranteed performance over temperature: 0°C to 70°C
- High isolation voltage: 2500Vrms (min)
- UL-recognized: UL 1577, File No.E67349

Truth Table

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H



Pin Configurations (top view)



1 : N.C.
2 : Anode
3 : Cathode
4 : N.C.
5 : GND
6 : Output(Open collector)
7 : Enable
8 : V_{CC}

Start of commercial production
1982-11

Absolute Maximum Ratings

Characteristics			Symbol	Rating	Unit
LED	Forward current		I_F	20	mA
	Pulse forward current	(Note 1)	I_{FP}	40	mA
	Reverse voltage		V_R	5	V
	Diode power dissipation		P_D	40	mW
	Input power dissipation derating	(Ta ≥ 70 °C)	△PD/°C	-0.73	mW/°C
Detector	Output current		I_O	50	mA
	Output voltage		V_O	7	V
	Supply voltage (1 minute maximum)		V_{CC}	7	V
	Enable input voltage (not to exceed V_{CC} by more than 500mV)		V_{EH}	5.5	V
	Output collector power dissipation		P_O	85	mW
	Output power dissipation derating	(Ta ≥ 85 °C)	△Po/°C	-2.2	mW/°C
Operating temperature range			T_{opr}	0 to 70	°C
Storage temperature range			T_{stg}	−55 to 125	°C
Lead solder temperature (10 s)		(Note 2)	T_{sol}	260	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 1: 50 % duty cycle, 1ms pulse width.

Note 2: Soldering portion of lead: Up to 2mm from the body of the device.

Recommended Operating Conditions

Characteristics	Symbol	Min	Max	Unit
Input current, low level each channel	I_{FL}	0	250	μA
Input current, high level each channel	I_{FH}	7	20	mA
High level enable voltage	V_{EH}	2.0	V_{CC}	V
Low level enable voltage (output high)	V_{EL}	0	0.8	V
Supply voltage, output*	V_{CC}	4.5	5.5	V
Fan out (TTL load)	N	—	8	—
Operating temperature	Ta	0	70	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.
*This item denotes operating ranges, not meaning of recommended operating conditions.

Precaution

Please be careful of the followings.
A ceramic capacitor (0.1μF) should be connected from pin 8 to pin 5 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property. The total lead length between capacitor and coupler should not exceed 1cm.

Electrical Characteristics

Over Recommended Temperature (Ta = 0 to 70°C unless otherwise noted)

Characteristics	Symbol	Test Condition	Min	(**)Typ.	Max	Unit
High level output current	I_{OH}	V_{CC} = 5.5 V, V_O = 5.5 V I_F = 250 μA, V_E = 2.0 V	—	1	250	μA
Low level output voltage	V_{OL}	V_{CC} = 5.5 V, I_F = 5 mA V_{EH} = 2.0 V I_{OL}(sinking) = 13 mA	—	0.4	0.6	V
High level enable current	I_{EH}	V_{CC} = 5.5 V, V_E = 2.0 V	—	−1.0	—	mA
Low level enable current	I_{EL}	V_{CC} = 5.5 V, V_E = 0.5 V	—	−1.6	−2.0	mA
High level supply current	I_{CCH}	V_{CC} = 5.5 V, I_F = 0 mA, V_E = 0.5 V	—	7	15	mA
Low level supply current	I_{CCL}	V_{CC} = 5.5 V, I_F = 10 mA, V_E = 0.5 V	—	12	18	mA
Resistance (input−output) (Note 3)	R_{I-O}	V_{I-O} = 500 V, Ta = 25 °C R.H. ≤ 60 %	—	10^{12}	—	Ω
Capacitance (input−output) (Note 3)	C_{I-O}	f = 1 MHz, V = 0 V, Ta = 25 °C	—	0.6	—	pF
Input forward voltage	V_F	I_F = 10 mA, Ta = 25 °C	—	1.65	1.75	V
Input reverse breakdown voltage	BV_R	I_R = 10 μA, Ta = 25 °C	5	—	—	V
Input capacitance	C_{IN}	V_F = 0 V, f = 1 MHz	—	45	—	pF
Current transfer ratio	CTR	I_F = 5.0 mA, R_L = 100 Ω	—	1000	—	%

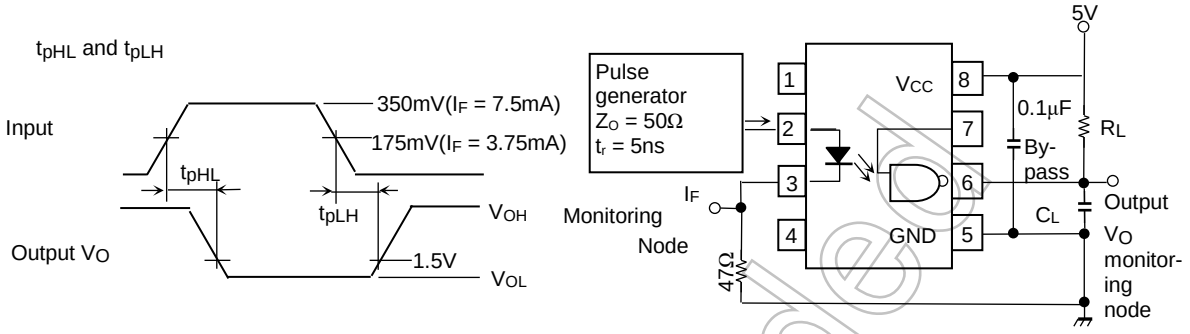
(**) All typical values are at V_{CC} = 5 V, Ta = 25 °C

Note 3: Pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together.

Switching Characteristics (Ta = 25°C, V_{CC} = 5V)

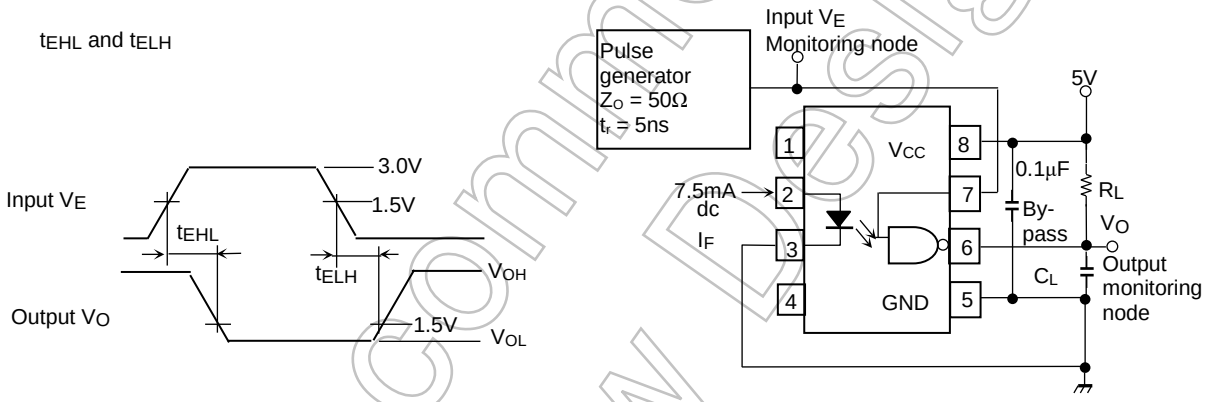
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time to high output level	t_{pLH}	1	R_L = 350 Ω, C_L = 15 pF I_F = 7.5mA	—	60	75	ns
Propagation delay time to low output level	t_{pHL}	1	R_L = 350 Ω, C_L = 15 pF I_F = 7.5 mA	—	60	75	ns
Output rise−fall time (10−90%)	t_r, t_f	—	R_L = 350 Ω, C_L = 15 pF I_F = 7.5 mA	—	30	—	ns
Propagation delay time of enable from V_{EH} to V_{EL}	t_{ELH}	2	R_L = 350 Ω, C_L = 15 pF I_F = 7.5 mA V_{EH} = 3.0 V V_{EL} = 0.5 V	—	25	—	ns
Propagation delay time of enable from V_{EL} to V_{EH}	t_{EHL}	2	R_L = 350 Ω, C_L = 15 pF I_F = 7.5 mA V_{EH} = 3.0 V V_{EL} = 0.5 V	—	25	—	ns
Common mode transient immunity at logic high output level	CM_H	3	V_{CM} = 10 V R_L = 350 Ω $V_{O(min)}$ = 2V I_F = 0 mA	—	200	—	V / μs
Common mode transient Immunity at logic low output level	CM_L	3	V_{CM} = 10 V R_L = 350 Ω $V_{O(max)}$ = 0.8 V I_F = 5 mA	—	−500	—	V / μs

Test Circuit 1.



・ C_L is approximately 15pF which includes probe and stray wiring capacitance.

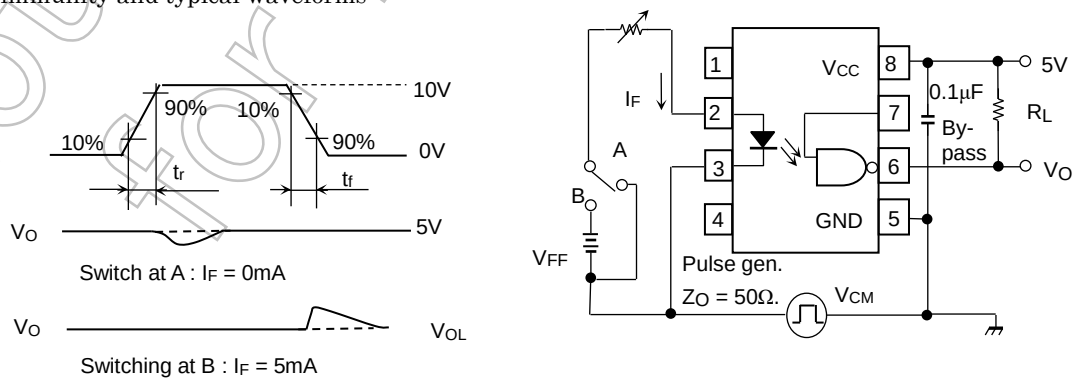
Test Circuit 2.



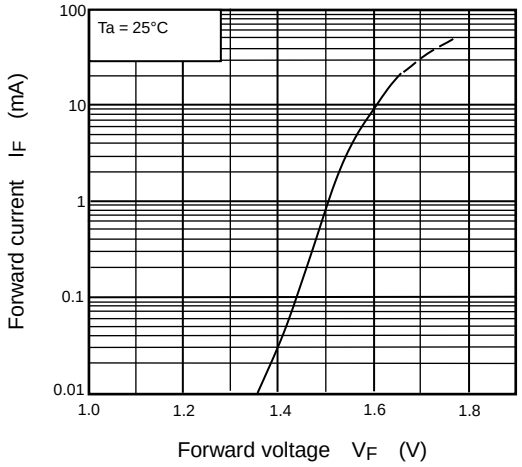
・ C_L is approximately 15pF which includes prove and stray wiring capacitance.

Test Circuit 3.

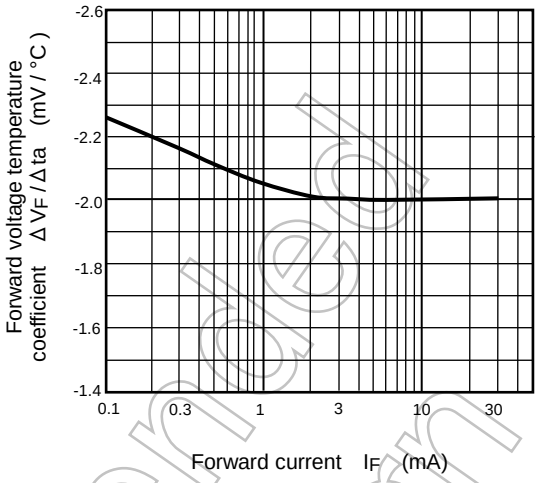
Transient immunity and typical waveforms



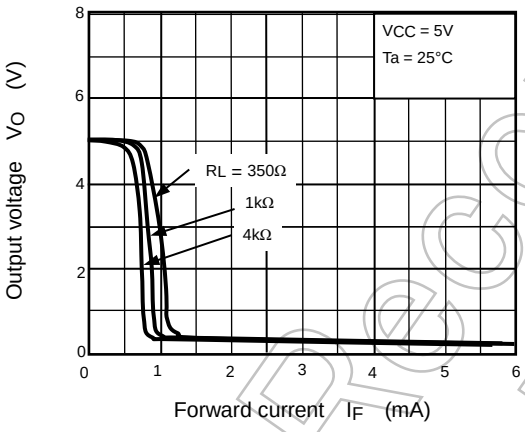
$I_F - V_F$



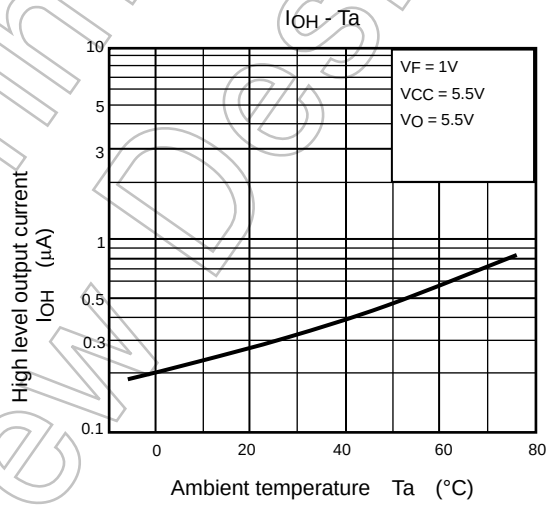
$\Delta V_F / \Delta Ta - I_F$



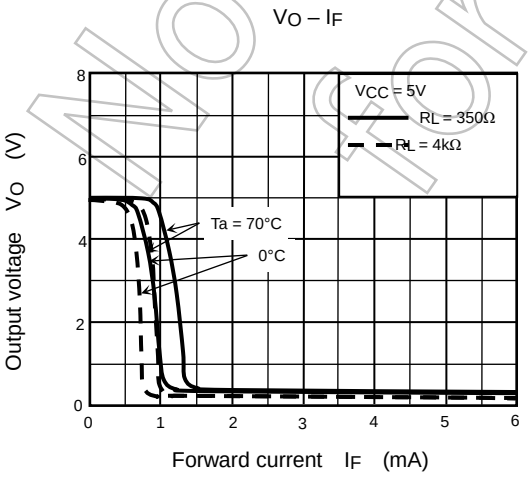
$V_O - I_F$



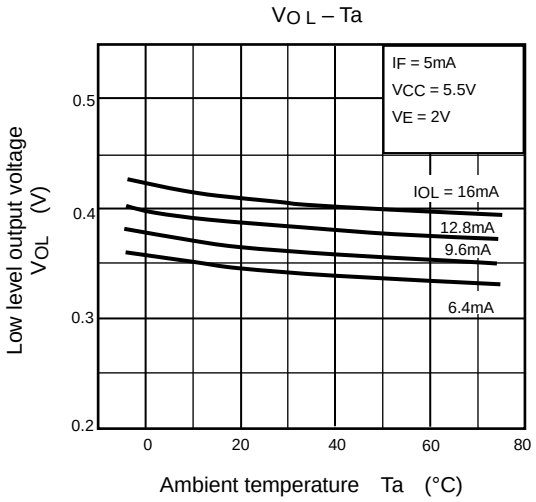
I_{OH} - Ta



$V_O - I_F$

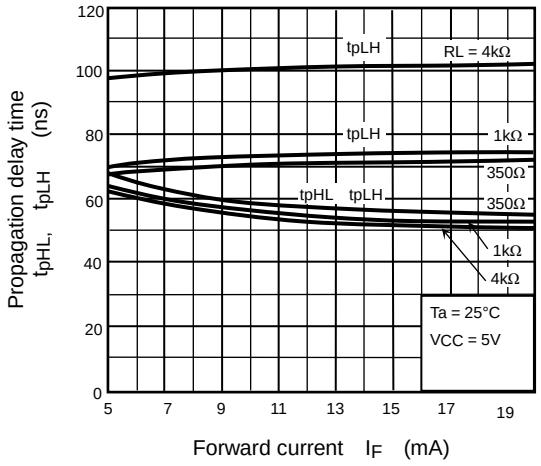


V_{OL} – Ta

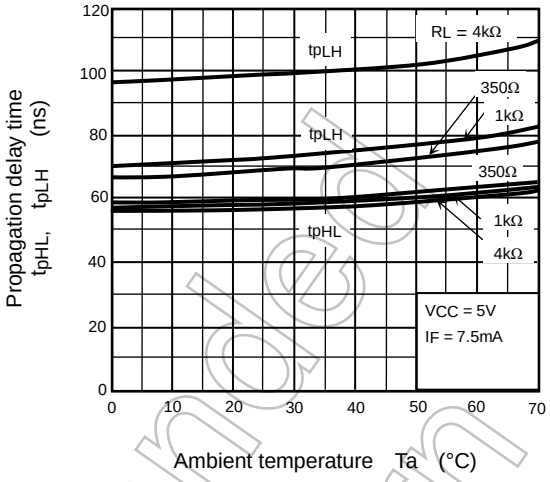


NOTE: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

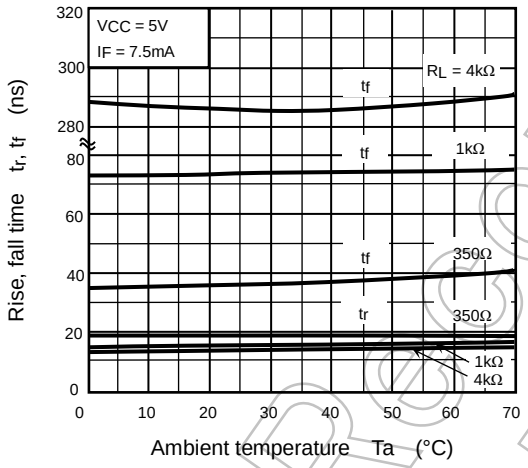
t_{pHL}, t_{pLH} - I_F



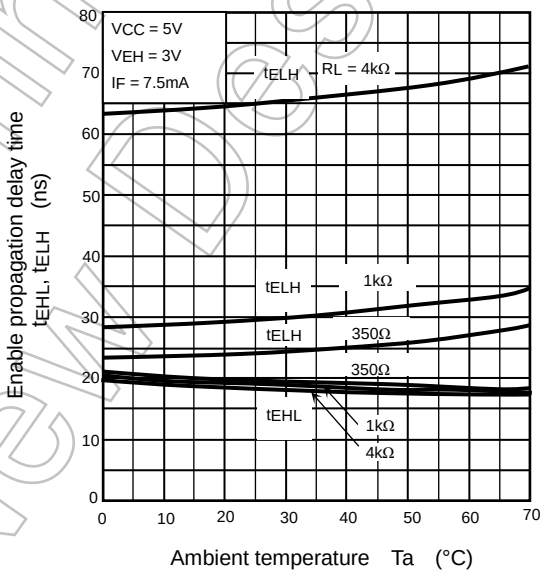
t_{pHL}, t_{pLH} - Ta



t_r, t_f – T_a



t_{EHL},t_{ELH} - T_a



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