INNODISK
Beyond your imagination

the total solution for
Industrial DRAM module

i-DIMM
INDUSTRIAL DRAM MODULE

Approval Sheet

Customer	
Product Number	M1SF-1GSCVC03-J
Module speed	**PC-3200**
Pin	**200 pin**
CAS Latency	**CL-3**
SDRAM Operating Temp	**0 ℃ ~ 70 ℃**
Date	**2nd December 2011**

Approval by Customer

P/N:

Signature:

Date:

Sales: **Sr. Technical manager: John Hsieh**

i-DIMM

1. Features

Key Parameter

Industry Nomenclature	Speed Grade	Data Rate MT/s			tRCD (ns)	tRP (ns)	tRC (ns)
		CL=2	CL=2.5	3			
PC-3200	F	266	333	400	15	15	55

- JEDEC Standard 200-pin Dual In-Line Memory Module
- Intend for 400 MHz applications
- Inputs and Outputs are SSTL-2 compatible
- VDD=VDDQ= 2.6 Volt ± 0.1 (PC-3200)
- Differential clock input
- DLL aligns DQ and DQS transition with CK transition
- Bi-Directional data strobe with one clock cycle
- Built with 512Mb DDR SDRAMs in 400 mil TSOP II packages
- Auto Refresh (CBR) and Self Refresh Modes support.
- Serial Presence Detect with EEPROM
- Auto & self refresh 7.8μs ($T_A \leq +70°C$)
- Operation Temperature
  - Commercial ($0°C \leq T_A \leq +70°C$)
- Programmable Device Operation:
  - Burst Type: Sequential or Interleave
  - Device CAS# Latency: 2,2.5 and 3
  - Burst Length: 2, 4 or 8
- RoHS Compliant *(Section 13)*

2. Environmental Requirements

iDIMM are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating Temperature (ambient)	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +150	°C	1

1. The component maximum case temperature (Tcase) shall not exceed the value specified in the DDR DRAM component specification.

3. Ordering Information

Standard Grade						
Part Number	Density	Speed	Organization	Number of DRAM	Number of rank	ECC
M1SF-1GSCVC03-J	1GB	PC-3200	64M x8	16	2	N/A

i-DIMM

4. Pin Configurations (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REF}	101	A9	26	DM1	126	V_{SS}	51	V_{SS}	151	DQ42	76	V_{SS}	176	DQ55
2	V_{REF}	102	A8	27	V_{SS}	127	DQ32	52	V_{SS}	152	DQ46	77	DQS8	177	DQ56
3	V_{SS}	103	V_{SS}	28	V_{SS}	128	DQ36	53	DQ19	153	DQ43	78	DM8	178	DQ60
4	V_{SS}	104	V_{SS}	29	DQ10	129	DQ33	54	DQ23	154	DQ47	79	CB2	179	V_{DD}
5	DQ0	105	A7	30	DQ14	130	DQ37	55	DQ24	155	V_{DD}	80	CB6	180	V_{DD}
6	DQ4	106	A6	31	DQ11	131	V_{DD}	56	DQ28	156	V_{DD}	81	V_{DD}	181	DQ57
7	DQ1	107	A5	32	DQ15	132	V_{DD}	57	V_{DD}	157	V_{DD}	82	V_{DD}	182	DQ61
8	DQ5	108	A4	33	V_{DD}	133	DQS4	58	V_{DD}	158	/CK1	83	CB3	183	DQS7
9	V_{DD}	109	A3	34	V_{DD}	134	DM4	59	DQ25	159	V_{SS}	84	CB7	184	DM7
10	V_{DD}	110	A2	35	CK0	135	DQ34	60	DQ29	160	CK1	85	DU	185	V_{SS}
11	DQS0	111	A1	36	V_{DD}	136	DQ38	61	DQS3	161	V_{SS}	86	DU/Reset	186	V_{SS}
12	DM12	112	A0	37	/CK0	137	V_{SS}	62	DM3	162	V_{SS}	87	V_{SS}	187	DQ58
13	DQ2	113	V_{DD}	38	V_{SS}	138	V_{SS}	63	V_{SS}	163	DQ48	88	V_{SS}	188	DQ62
14	DQ6	114	V_{DD}	39	V_{SS}	139	DQ35	64	V_{SS}	164	DQ52	89	CK2	189	DQ59
15	V_{SS}	115	A10/AP	40	V_{SS}	140	DQ39	65	DQ26	165	DQ49	90	V_{SS}	190	DQ63
16	V_{SS}	116	BA1	41	DQ16	141	DQ40	66	DQ30	166	DQ53	91	CK2	191	V_{DD}
17	DQ3	117	BA0	42	DQ20	142	DQ44	67	DQ27	167	V_{DD}	92	V_{DD}	192	V_{DD}
18	DQ7	118	RAS	43	DQ17	143	V_{DD}	68	DQ31	168	V_{DD}	93	V_{DD}	193	SDA
19	DQ8	119	WE	44	DQ21	144	V_{DD}	69	V_{DD}	169	DQS6	94	V_{DD}	194	SA0
20	DQ12	120	CAS	45	V_{DD}	145	DQ41	70	V_{DD}	170	DM6	95	CKE1	195	SCL
21	V_{DD}	121	/S0	46	V_{DD}	146	DQ45	71	CB0	171	DQ50	96	CKE0	196	SA1
22	V_{DD}	122	/S1	47	DQS2	147	DQS5	72	CB4	172	DQ54	97	DU	197	V_{DDSPD}
23	DQ9	123	DU (A13)	48	DM2	148	DM5	73	CB1	173	V_{SS}	98	DU	198	SA2
24	DQ13	124	DU	49	DQ18	149	V_{SS}	74	CB5	174	V_{SS}	99	A12	199	V_{DDID}
25	DQS1	125	V_{SS}	50	DQ22	150	V_{SS}	75	V_{SS}	175	DQ51	100	A11	200	DU

Pins 71, 72, 73, 74, 77, 78, 79, 80, 83, 84 are reserved for x72 variants of this module and are not used on the x64 versions.
1. Pin 86 is reserved for a registered variant of this module and is not used on the unbuffered version.
2. Pins 89, 91are reserved for x72 modules or registered modules.
3. Pin 123 reserved for higher density memories, requiring A13

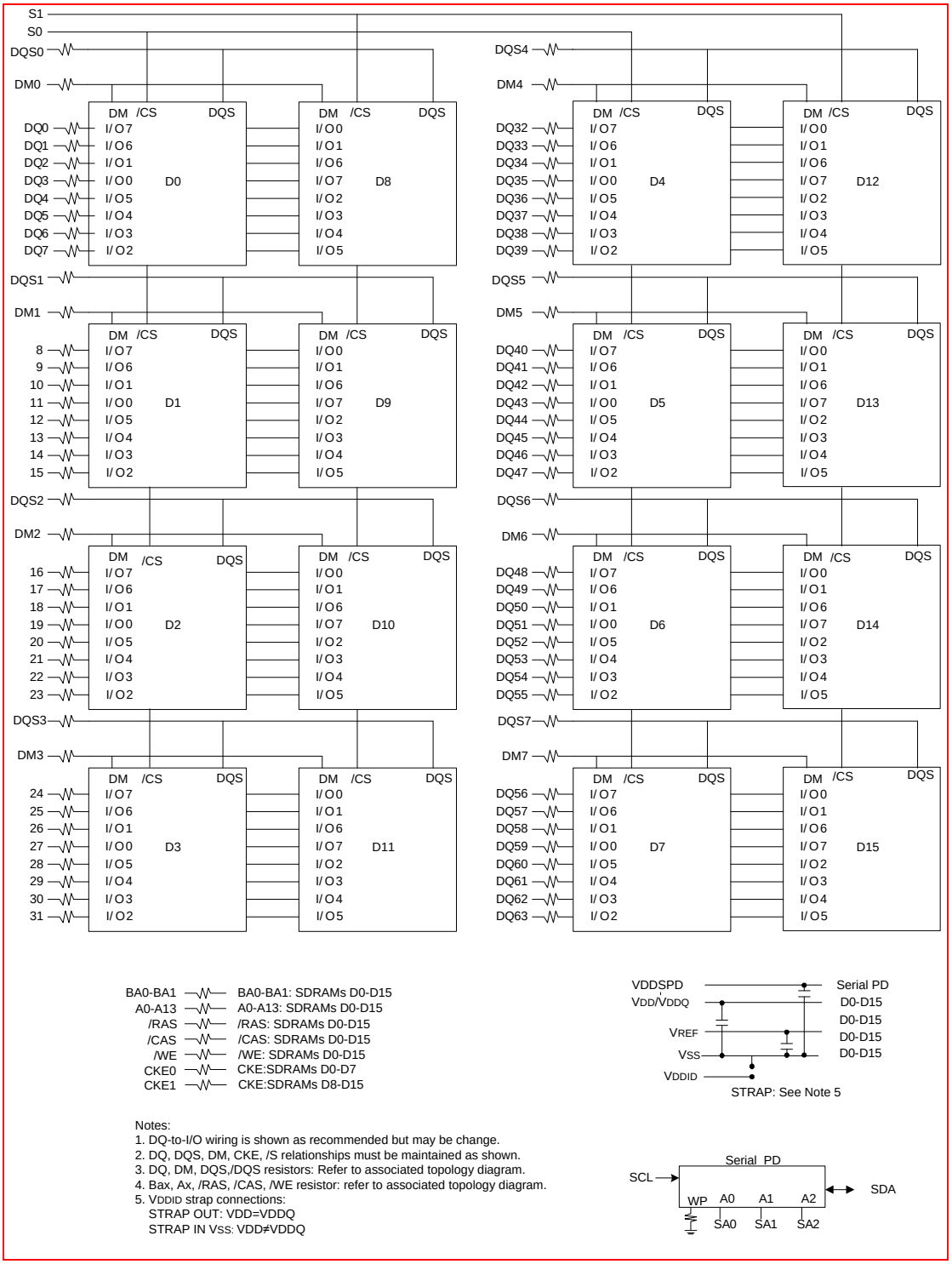
5. Architecture

Pin Definition

Pin Name	Description	Pin Name	Description
A0 - A13 (A14 or A15)	SDRAM address bus	CK0 – CK1 CK0# - CK1#	Differential SDRAM Clocks
BA0 - BA1 (or BA2)	SDRAM Bank Address Inputs	SCL	Serial Presence Detect Clock Input
RAS#	SDRAM row address strobe	SDA	Serial Presence Detect Data input/output
CAS#	SDRAM column address strobe	SA0 – SA2	Serial Presence Detect Address Inputs
WE#	SDRAM write enable	V_{DD}	Power Supply
S0# - S1#	DIMM Rank Select Lines	V_{DDID}	V_{DD} Identification Flag
CK0 – CKE1	SDRAM clock enable lines	V_{DDQ}	SDRAM I/O Driver power supply
DQ0 – DQ63	DIMM memory data bus	V_{REF}	SDRAM I/O Reference supply
CB0 – CB7	DIMM ECC check bit	V_{SS}	Ground
DQS0 – DQS17	SDRAM data strobes	V_{DDSPD}	Serial EEPROM positive power supply
DM0 – DM7	SDRAM data masks	Reset	Reset enable
NC	Spare Pin		

6. Function Block Diagram:

- (1GB, 2 Ranks, 128Mx64 DDR Unbuffered DIMM)



7. Absolute Maximum Ratings

Symbol	Parameter		Rating	Units
T_A	Operation Temperature	Standard	0 to 70	°C
T_{STG}	Storage Temperature		-55 to 150	°C
V_{INPUT}	Voltage input pins relative to Vss		-1.0 to +3.6	V
V_{IO}	Voltage on I/O pins relative to Vss		-0.5 to +3.6	V
V_{DD}	Voltage on VDD supply relative to Vss		-1.0 to +3.6	V
V_{DDQ}	Voltage on VDDQ supply relative to Vss		-1.0 to +3.6	V
I_{OS}	Output short Circuit Current		50	mA

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

8. AC & DC Operating Conditions

- AC Operating Conditions

(T_{CASE} = 0 °C ~ 70 °C; V_{SS}=0V)

Symbol	Parameter	Value		Units	Notes
		Min	Max		
V_{IH} (AC)	Input High (Logic1) Voltage	V_{REF} + 0.31	-	V	
V_{IL} (AC)	Input Low (Logic0) Voltage	-	V_{REF} + 0.31	V	
V_{ID} (AC)	Input differential Voltage: CK, /CK	0.7	V_{DDQ} + 0.6	V	1
V_{IX} (AC)	Input crossing point Voltage: CK, /CK	0.5* V_{DDQ} + 0.2	0.5* V_{DDQ} - 0.2	V	2

Note:

1. VID is the magnitude of the difference between the input level on CK and the input on /CK.
2. The value of VIX is expected to equal 0.5*V DDQ of the transmitting device and must track variations in the DC level of the same.

- DC Electrical Characteristics and Operating Conditions

(T_{CASE} = 0 °C ~ 70 °C; V_{SS} = 0V)

Symbol	Parameter	Min	Typ.	Max	Units	Notes
V_{DD}	Supply Voltage (DDR266,333)	2.3	2.5	2.7	V	
	Supply Voltage (DDR400)	2.5	2.6	2.7	V	
V_{DDQ}	Supply Voltage (DDR266,333)	2.3	2.5	2.7	V	
	Supply Voltage (DDR400)	2.5	2.6	2.7	V	
$V_{IH\ (DC)}$	Input High (Logic1) Voltage	V_{REF} + 0.15	-	V_{DDQ} + 0.3	V	1
$V_{IL\ (DC)}$	Input Low (Logic0) Voltage	-0.3	-	V_{REF} - 0.15	V	1
V_{TT}	Termination Voltage	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	3
V_{REF}	I/O Reference Voltage	0.49V_{DDQ}	0.5V_{DDQ}	0.51V_{DDQ}	V	2
$V_{IN(DC)}$	Input Voltage Level: CK, /CK	-0.3	-	V_{DDQ} + 0.3	V	
$V_{ID(DC)}$	Input Differential Voltage: CK, /CK	0.36	-	V_{DDQ} + 0.6	V	
$V_{I(RATIO)}$	V-I Matching	0.71	-	1.4	V	

Note:

1. Inputs are not recognized as valid until V_{REF} stabilizes.
2. V_{REF} is expected to be equal to 0.5 V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed 2% of the DC value.
3. V_{TT} of transmitting device must track V_{REF} of receiving device.

i-DIMM

9. Operating, Standby, and Refresh Currents

- 1GB UDIMM (2 Rank, 128Mx8 DDR SDRAMs T_{CASE} = 0 °C ~ 70 °C)

Symbol	Parameter/Condition	PC-3200	Unit
I_{DD0}	One bank; Active - Precharge; tRC=tRC(min); tCK=tCK(min); DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1520	mA
I_{DD1}	One bank; Active - Read - Precharge; Burst Length=2; tRC=tRC(min); tCK=tCK(min); address and control inputs changing once per clock cycle	1840	mA
I_{DD2P}	All banks idle; Power down mode; CKE=Low, tCK=tCK(min)	160	mA
I_{DD2F}	/CS=High, All banks idle; tCK=tCK(min); CKE= High; address and control inputs changing once per clock cycle.VIN=VREF for DQ, DQS and DM	560	mA
I_{DD3P}	One bank active ; Power down mode; CKE=Low, tCK=tCK(min)	720	mA
I_{DD3N}	/CS=HIGH; CKE=HIGH; One bank; Active-Precharge;tRC=tRAS(max); tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	960	mA
I_{DD4R}	Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); IOUT=0mA	2160	mA
I_{DD4W}	Burst=2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle	2320	mA
I_{DD5}	tRC=tRFC(min) - 8*tCK for DDR200 at 100Mhz, 10*tCK for DDR266A & DDR266B at 133Mhz; distributed refresh	2560	mA
I_{DD6}	CKE=<0.2V; External clock on; tCK=tCK(min)	80	mA
I_{DD7}	Four bank interleaving with BL=4 Refer to the following page for detailed test condition	3360	mA

10. AC Timing Specifications

(T_{CASE} = 0 °C ~ 70 °C; V_{DDQ} = V_{DD} , See AC Characteristics)

Symbol	Parameter	PC2-3200		Unit
		Min.	Max.	
tAC	DQ output access time from CK/CK#	-0.7	0.7	ns
tDQSCK	DQS output access time from CK/CK#	-0.55	0.55	ns
tCH	CK high-level width	0.45	0.55	tCK
tCL	CK low-level width	0.45	0.55	tCK
tHP	Minimum half clk period for any given cycle; defined by clk high (tCH) or clk low (tCL) time	min (tCL,tCH)	-	ns
tCK	Clock Cycle Time	5	10	ns
tDS	DQ and DM input setup time(differential data strobe)	0.4	-	ns
tDH	DQ and DM input hold time(differential data strobe)	0.4	-	ns
tIPW	Input pulse width	2.2	-	ns
tDIPW	DQ and DM input pulse width (each input)	1.75	-	ns
tHZ	Data-out high-impedance time from CK/CK	-0.7	0.7	ns
tLZ(DQS)	DQS low-impedance time from CK/CK	-0.7	0.7	ns
tLZ(DQ)	DQ low-impedance time from CK/CK	-0.7	0.7	ns
tDQSQ	DQS-DQ skew (DQS & associated DQ signals)	-	0.4	ns
tQHS	Data hold Skew Factor	-	0.5	ns
tQH	Data output hold time from DQS	tHP -tQHS	-	ns
tDQSS	Write command to 1st DQS latching transition	0.72	1.25	tCK
tDQSL,(H)	DQS input low (high) pulse width (write cycle)	0.35	-	tCK
tDSS	DQS falling edge to CK setup time (write cycle)	0.35	-	tCK
tDSH	DQS falling edge hold time from CK (write cycle)	0.4	-	tCK
tMRD	Mode register set command cycle time	2	-	tCK
tWPST	Write postamble	0.4	0.6	tCK
tWPRE	Write preamble	0.9	1.1	tCK
tIH	Address and control input hold time	0.6	-	ns

t_{IS}	Address and control input setup time	0.7	-	ns
t_{RPRE}	Read preamble	0.9	1.1	t_{CK}
t_{RPST}	Read postamble	0.4	0.6	t_{CK}
t_{RRD}	Active bank A to Active bank B command	10	-	ns
t_{REFI}	Average Periodic Refresh Interval ($85^{o}C < T_{CASE} \leq 95^{o}C$)	-	3.9	µs
	Average Periodic Refresh Interval ($0^{o}C \leq T_{CASE} \leq 85^{o}C$)	-	7.8	µs
t_{CCD}	CAS# to CAS# delay	15	-	t_{CK}
t_{WR}	Write recovery time without Auto-Precharge	15		ns
t_{DAL}	Auto precharge write recovery + precharge time	(tWR/tCK) +(tRP/tCK)	-	t_{CK}
t_{WTR}	Internal write to read command delay	2	-	ns
t_{XSNR}	Exit self refresh to a Non-read command	75	-	ns
t_{XSRD}	Exit self refresh to a Read command	200	-	t_{CK}
t_{CKE}	CKE minimum pulse width			t_{CK}

11. SPD

Serial Presence Detect –(1GB)

128Mx64 2 RANKs UNBUFFERED DDR SDRAM DIMM based on 64Mx8, 4Banks, 4K Refresh, 2.6V DDR2 SDRAMs with SPD

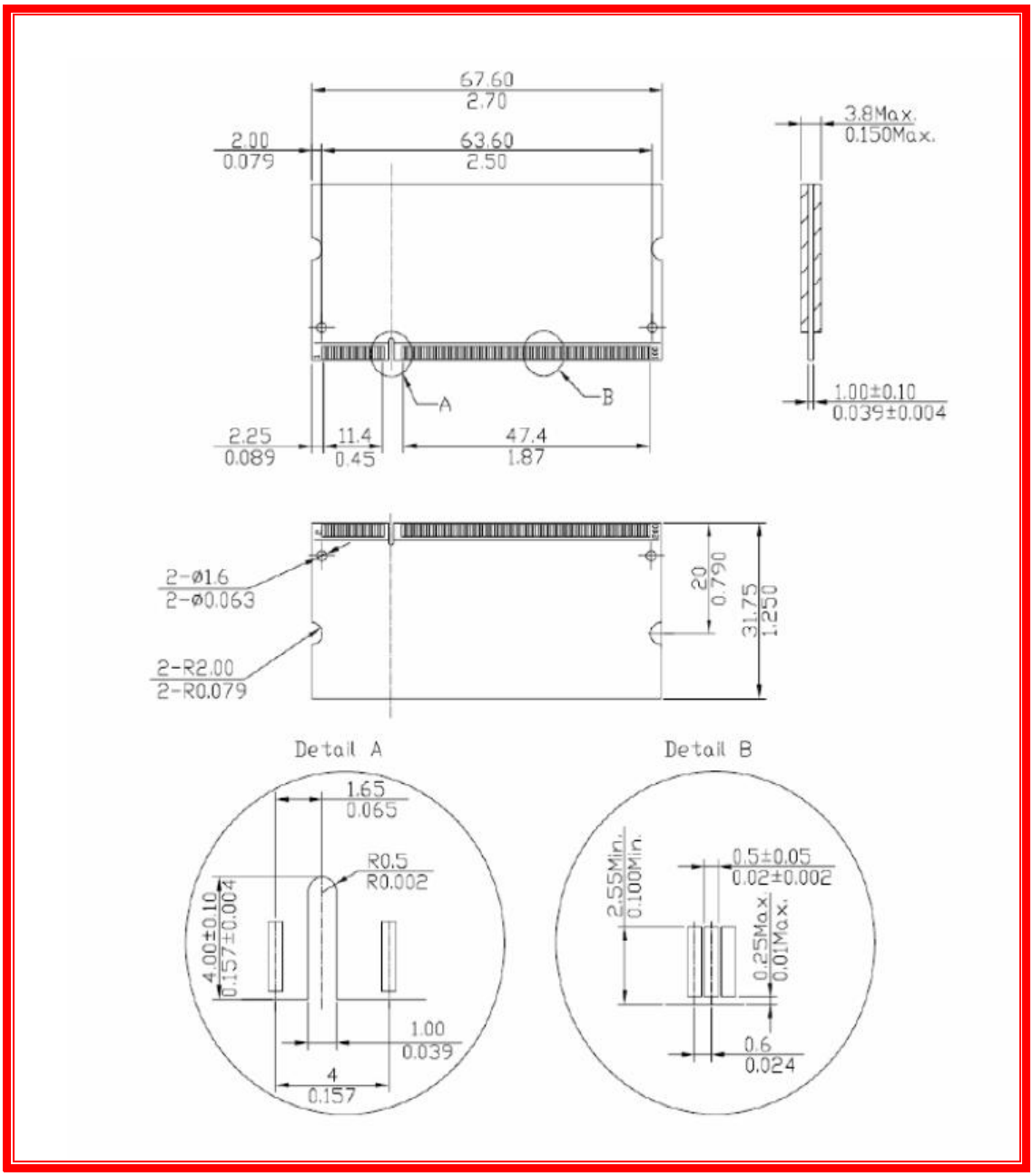
Byte	Description	Serial PD Data Entry (Hexadecimal)	Note
		M1UF1GHC2C03-E	
0	Number of Serial PD Bytes Written during Production	80	
1	Total Number of Bytes in Serial PD device	08	
2	Fundamental Memory Type	07	
3	Number of Row Addresses on Assembly	0D	
4	Number of Column Addresses on Assembly	0B	
5	Number of DIMM Bank, Package, and Height	02	
6	Data Width of this Assembly	40	
7	Reserved	00	
8	Voltage Interface Level of this Assembly	04	
9	DDR SDRAM Cycle Time at CL=5 (ns)	50	
10	DDR SDRAM Access Time from Clock at CL=5 (ns)	70	
11	DIMM Configuration Type	00	
12	Refresh Rate/Type	82	
13	Primary DDR SDRAM Width	08	
14	Error Checking DDR2 SDRAM Device Width	00	
15	Reserved	01	
16	DDR SDRAM Device Attributes: Burst Length Supported	0E	
17	DDR SDRAM Device Attributes: Number of Device Banks	04	
18	DDR SDRAM Device Attributes: /CAS Latencies Supported	1C	
19	Reserved	01	
20	DDR SDRAM DIMM Type Information	02	
21	DDR SDRAM Module Attributes:	20	
22	DDR SDRAM Device Attributes: General	C0	
23	Minimum Clock Cycle at CL=4	60	

24	Maximum Data Access Time (t_{ac}) from Clock at CL=4 (ns)	70	
25	Minimum Clock Cycle Time at CL=3 (ns)	75	
26	Maximum Data Access Time (t_{ac}) from Clock at CL=3 (ns)	75	
27	Minimum Row Precharge Time (t_{RP}) (ns)	3C	
28	Minimum Row Active to Row Active delay (t_{RRD})	28	
29	Minimum RAS to CAS delay (t_{RCD}) (ns)	3C	
30	Minimum RAS Pulse Width (t_{RAS})	28	
31	Module Bank Density	80	
32	Address and Command Setup Time Before Clock (t_{IS}) (ns)	60	
33	Address and Command Hold Time After Clock (t_{IH}) (ns)	60	
34	Data Input Setup Time Before Clock (t_{DS})	40	
35	Data Input Hold Time After Clock (t_{DH}) (ns)	40	
36	Write Recovery Time (t_{WR})	00	
37	Internal Write to Read Command delay (t_{WTR})	00	
38	Internal Read to Precharge delay (t_{RTP})	00	
39	Memory Analysis Probe Characteristics	00	
40	Extension of Byte 41 t_{RC} and Byte 42 t_{RFC}	00	
41	Minimum Core Cycle Time (t_{RC}) (ns)	37	
42	Min. Auto Refresh Command Cycle Time (t_{RFC})	46	
43	Maximum Clock Cycle Time (t_{CK})	28	
44	Max. DQS-DQ Skew Factor (t_{DQS}) (ns)	28	
45	Read Data Hold Skew Factor (t_{QHS}) (ns)	50	
46	PLL Relock Time	00	
47	Tcasemax DT4R4W Delta	00	
48	Thermal Resistance of DRAM Package from Top (Case) to Ambient (Psi-T-A DRAM)	00	
49	DRAM Case Temperature Rise from Ambient due to Activate-Precharge/Mode Bits (DT0/Mode Bits)	00	
50	DRAM Case Temperature Rise from Ambient due to Precharge/Quiet Standby (DT2N/DT2Q)	00	

51	DRAM Case Temperature Rise from Ambient due to Precharge Power-Down (DT2P)	00	
52	DRAM Case Temperature Rise from Ambient due to Active Standby (DT3N)	00	
53	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Fast PDN Exit (DT3Pfast)	00	
54	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Slow PDN Exit (DT3Pslow)	00	
55	DRAM Case Temperature Rise from Ambient due to Page Open Burst Read/DT4R4W Mode Bit (DT4R/DT4R4W Mode Bit)	00	
56	DRAM Case Temperature Rise from Ambient due to Burst Refresh (ST5B)	00	
57	DRAM Case Temperature Rise from Ambient due to Bank interleave Reads with Auto-Precharge (DT7)	00	
58	Thermal Resistance of PLL Package from Top (Case) to Ambient (Psi T-A PLL)	00	
59	Thermal Resistance of Register Package from Top (Case) to Ambient (Psi T-A Register)	00	
60	PLL Case Temperature Rise from Ambient due to PLL Active (DT PLL Active)	00	
61	Register Case Temperature Rise from Ambient due to Register Active/Mode Bit (DT Register Active/Mode Bit)	00	
62	SPD Reversion	11	
63	Checksum for byte 0-62	B9	
64-71	Manufacture's JEDEC ID Code	InnoDisk	
72	Module Manufacturing Location	Manufacturing Code	
73-91	Module Part number	Module Part Number in ASCII	
92-255	Reserved	Undefined	

12. PACKAGE DIMENSION

- (1GB, 2 Ranks, 64Mx8 DDR2 SDRAMs)



Note: Device position is only for reference.

13. RoHS Declaration

INNODISK® Beyond your imagination

Page 1/1

Declaration of Conformity

We, InnoDisk Co., Ltd, here declare the product M1SF-1GSCVC03-J complies with the requirement of RoHS directives 2002/95/EC and 2006/122/EC.

Innodisk ensures the above product meets RoHS requirements of six restricted substances. This declaration is based on vendor supplied analysis/MSDS, material certifications, and/ or 3rd party test reports of the component/ raw materials used in the manufacture of products.

Name of hazardous substance	Limited of RoHS ppm（mg/kg）
Cd	＜ 100 ppm
Pb	＜ 1000 ppm
Hg	＜ 1000 ppm
Chromium VI（Cr+6）	＜ 1000 ppm
Polybromodiphenyl ether（PBDE）	＜ 1000 ppm
Polybrominated Biphenyls（PBB）	＜ 1000 ppm

Date issued: 2012/01/19

Manufacturer: ：InnoDisk Co., Ltd.
Address：9F, No. 100, Sec.1 Xintai 5th Rd., Xizhi City, Taipei 221, Taiwan

Authorized Signature：

QA Dept. Director – Ryan Tsai

i-DIMM

Revision Log

Rev	Date	Modification
0.1	27th May 2011	Preliminary Edition
1.0	15th September 2011	Official Released.